## TPS61085A-Q1 $650-\mathrm{kHz}$ and 1.2-MHz, 18.5-V step-up DC/DC converter

## 1 Features

- AEC-Q100 qualified for automotive applications:
- Device temperature grade $2:-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$, $\mathrm{T}_{\mathrm{A}}$
- 2.3-V to 6-V input voltage range
- 18.5-V boost converter with 2-A switch current
- $650-\mathrm{kHz}$ or $1.2-\mathrm{MHz}$ selectable switching frequency
- Adjustable soft start
- Thermal shutdown
- Undervoltage lockout
- 8-pin VSSOP package


## 2 Applications

- Automotive infotainment cluster
- Instrument clusters, head units
- Radios, navigation
- Audio amplifiers
- Automotive body electronics
- Body control modules
- Gateways
- Telematics and emergency call (E-call)
- Advanced driver assistance systems (ADAS)


## 3 Description

The TPS61085A-Q1 device is a high-frequency, highefficiency, DC/DC boost converter with an integrated $2-\mathrm{A}, 0.13-\Omega$ power switch capable of providing an output voltage up to 18.5 V . The selectable frequency of 650 kHz or 1.2 MHz allows the use of small external inductors and capacitors and provides fast transient response. The external compensation allows optimizing the regulator for application conditions. A capacitor connected to the specific softstart pin minimizes inrush current at start-up.

## Device Information ${ }^{(1)}$

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
| :---: | :---: | :---: |
| TPS61085A-Q1 | VSSOP (8) | $3.00 \mathrm{~mm} \times 3.00 \mathrm{~mm}$ |

(1) For all available packages, see the orderable addendum at the end of the data sheet.


An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

Changes from Revision A (April 2018) to Revision B Page

- First public release of data sheet to the Web ..... 1
Changes from Original (September 2017) to Revision A Page
- Changed status to Production Data ..... 1


## 5 Pin Configuration and Functions



Pin Functions

| PIN |  | TYPE |  |
| :--- | :---: | :---: | :--- | :--- |
| NO. | NAME |  |  |
| 1 | COMP | I/O | Compensation pin |
| 2 | FB | I | Feedback pin |
| 3 | EN | I | Shutdown control input. Connect this pin to logic high level to enable the device. |
| 4 | PGND | - | Power ground |
| 5 | SW | I | Switch pin |
| 6 | IN | PWR | Input supply pin |
| 7 | FREQ | I | Frequency select pin. The power switch operates at 650 kHz if FREQ is connected to GND and at 1.2 MHz <br> if FREQ is connected to IN. |
| 8 | SS | O | Soft-start control pin. Connect a capacitor to this pin if soft-start required. Open = no soft start |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ${ }^{(1)}$

|  | MIN |  | MAX |
| :--- | ---: | ---: | ---: |
| UNIT |  |  |  |
| Input voltage, IN ${ }^{(2)}$ | -0.3 | 7 | V |
| Voltage on pins EN, FB, SS, FREQ, COMP | -0.3 | 7 | V |
| Voltage on pin SW | -0.3 | 20 | V |
| Continuous power dissipation | See Thermal Information |  |  |
| Lead temperature (soldering, 10 s) |  | 260 | ${ }^{\circ} \mathrm{C}$ |
| Operating junction temperature | -40 | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature, $\mathrm{T}_{\text {stg }}$ | -65 | 150 | ${ }^{\circ} \mathrm{C}$ |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to network ground terminal.

### 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {(ESD) }}$ | Electrostatic discharge | Human-body model (HBM), Classification Level 2 per AEC Q100-002 ${ }^{(1)}$ | $\pm 2000$ | V |
|  |  | Charged-device model (CDM), Classification Level C4A per AEC Q100-011 | $\pm 500$ |  |
|  |  | Machine model (MM) | $\pm 200$ |  |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

|  |  | MIN | MAX |
| :--- | :--- | ---: | :---: |
| $\mathrm{V}_{\mathrm{IN}}$ | UNPut voltage | 2.3 | 6 |
| $\mathrm{~V}_{S}$ | Uoost output voltage | $\mathrm{V}_{\text {IN }}+0.5$ | 18.5 |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating free-air temperature | -40 | 105 |
| $\mathrm{~T}_{J}$ | Operating junction temperature | -40 | 125 |

### 6.4 Thermal Information

| THERMAL METRIC ${ }^{(1)}$ |  | $\begin{gathered} \text { TPS61085A-Q1 } \\ \hline \text { DGK (VSSOP) } \\ \hline \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
|  |  | 8 PINS |  |
| $\mathrm{R}_{\text {өJA }}$ | Junction-to-ambient thermal resistance | 189.7 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {өJC(top) }}$ | Junction-to-case (top) thermal resistance | 75.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {日JB }}$ | Junction-to-board thermal resistance | 110 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| \%JT | Junction-to-top characterization parameter | 13.7 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\psi_{\text {JB }}$ | Junction-to-board characterization parameter | 108.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

(1) For more information about traditional and new thermal metrics, see the application report, Semiconductor and IC Package Thermal Metrics.

### 6.5 Electrical Characteristics

$\mathrm{V}_{\mathrm{IN}}=3.3 \mathrm{~V}, \mathrm{EN}=\mathrm{IN}, \mathrm{V}_{\mathrm{S}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$, typical values are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SUPPLY |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IN }}$ | Input voltage |  | 2.3 |  | 6 | V |
| $\mathrm{I}_{\mathrm{Q}}$ | Operating quiescent current into IN | Device not switching, $\mathrm{V}_{\mathrm{FB}}=1.3 \mathrm{~V}$ |  | 70 | 100 | $\mu \mathrm{A}$ |
| ISDVIN | Shutdown current into IN | EN = GND |  |  | 1 | $\mu \mathrm{A}$ |
| UVLO | Undervoltage lockout threshold | $\mathrm{V}_{\text {IN }}$ falling |  |  | 2.2 | V |
|  |  | $\mathrm{V}_{\text {IN }}$ rising |  |  | 2.3 |  |
| $\mathrm{T}_{\text {SD }}$ | Thermal shutdown | Temperature rising, $\mathrm{T}_{J}$ |  | 150 |  | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {SD(HYS) }}$ | Thermal shutdown hysteresis |  |  | 14 |  | ${ }^{\circ} \mathrm{C}$ |
| LOGIC SIGNALS EN, FREQ |  |  |  |  |  |  |
| $\mathrm{V}_{1 H}$ | High level input voltage | $\mathrm{V}_{\mathbb{I}}=2.3 \mathrm{~V}$ to 6 V | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low level input voltage | $\mathrm{V}_{\mathrm{IN}}=2.3 \mathrm{~V}$ to 6 V |  |  | 0.5 | V |
| $\mathrm{l}_{1 \mathrm{~kg}}$ | Input leakage current | $\mathrm{EN}=\mathrm{FREQ}=\mathrm{GND}$ |  |  | 0.1 | $\mu \mathrm{A}$ |
| BOOST CONVERTER |  |  |  |  |  |  |
| $\mathrm{V}_{\text {S }}$ | Boost output voltage |  | $\mathrm{V}_{\mathrm{IN}}+0.5$ |  | 18.5 | V |
| $\mathrm{V}_{\text {FB }}$ | Feedback regulation voltage |  | 1.230 | 1.238 | 1.246 | V |
| gm | Transconductance error amplifier |  |  | 107 |  | $\mu \mathrm{A} / \mathrm{V}$ |
| $\mathrm{I}_{\text {FB }}$ | Feedback input bias current | $\mathrm{V}_{\text {FB }}=1.238 \mathrm{~V}$ |  |  | 0.1 | $\mu \mathrm{A}$ |
| $\mathrm{R}_{\mathrm{DS} \text { (on) }}$ | N-channel MOSFET ON-resistance | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}, \mathrm{I}_{\text {SW }}=$ current limit |  | 0.13 | 0.2 | $\Omega$ |
|  |  | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\mathrm{GS}}=3.3 \mathrm{~V}, \mathrm{I}_{\text {SW }}=$ current limit |  | 0.15 | 0.24 |  |
| $\mathrm{l}_{\text {kg }}$ | SW leakage current | $\mathrm{EN}=\mathrm{GND}, \mathrm{V}_{\text {SW }}=6 \mathrm{~V}$ |  |  | 2 | $\mu \mathrm{A}$ |
| ILIM | N-channel MOSFET current limit |  | 2 | 2.6 | 3.2 | A |
| Iss | Soft-start current | $\mathrm{V}_{\text {SS }}=1.238 \mathrm{~V}$ | 7 | 10 | 13 | $\mu \mathrm{A}$ |
| $\mathrm{f}_{\text {osc }}$ | Oscillator frequency | FREQ $=$ high | 0.9 | 1.2 | 1.5 | MHz |
|  |  | FREQ = low | 480 | 650 | 820 | kHz |
|  | Line regulation | $\mathrm{V}_{\text {IN }}=2.3 \mathrm{~V}$ to 6 V , $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ |  | 0.0002 |  | \%/V |
|  | Load regulation | $\mathrm{V}_{\text {IN }}=3.3 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=1 \mathrm{~mA}$ to 400 mA |  | 0.11 |  | \%/A |

### 6.6 Typical Characteristics

The typical characteristics are measured with the $3.3-\mu \mathrm{H}$ inductor for high-frequency (part number-7447789003) or $6.8-\mu \mathrm{H}$ inductor for low frequency (part number-B82464G4) and the rectifier diode with part number SL22.

Table 1. Table of Graphs

|  |  |  | FIGURE |
| :---: | :---: | :---: | :---: |
|  | Maximum load current | vs Input voltage at high frequency (1.2 MHz) | Figure 1 |
| IOUT(max) | Maximum load current | vs Input voltage at low frequency ( 650 kHz ) | Figure 2 |
|  | Efficiency | vs Load current, $\mathrm{V}_{\mathrm{S}}=12 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=3.3 \mathrm{~V}$ | Figure 3 |
| $\eta$ | Efriency | vs Load current, $\mathrm{V}_{\mathrm{S}}=9 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=3.3 \mathrm{~V}$ | Figure 4 |
|  | Supply current | vs Supply voltage | Figure 5 |
|  | Frequency | vs Load current | Figure 6 |
|  | Frequency | vs Supply voltage | Figure 7 |



Figure 1. Maximum Load Current vs Input Voltage


Figure 3. Efficiency vs Load Current, $\mathrm{V}_{\mathrm{S}}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=3.3 \mathrm{~V}$


Figure 2. Maximum Load Current vs Input Voltage


Figure 4. Efficiency vs Load Current, $\mathrm{V}_{\mathrm{S}}=9 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=3.3 \mathrm{~V}$

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Figure 5. Supply Current vs Supply Voltage


Figure 6. Frequency vs Load Current


Figure 7. Frequency vs Supply Voltage

## 7 Detailed Description

### 7.1 Overview

The TPS61085A-Q1 boost converter is designed for output voltages up to 18.5 V with a switch-peak current limit of 2 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable between 650 kHz or 1.2 MHz and the minimum input voltage is 2.3 V . To control the inrush current at start-up, a soft-start pin is available.

The novel topology of the TPS61085A-Q1 boost converteruses adaptive OFF-time to provide superior load and line transient responses. The device also operates over a wider range of applications than conventional converters.
The selectable switching frequency offers the possibility to optimize the design either for the use of small sized components ( 1.2 MHz ) or for higher system efficiency ( 650 kHz ). However, the frequency changes slightly because the voltage drop across the $R_{\text {DS(on) }}$ has some influence on the current and voltage measurement and thus on the ON-time (the OFF-time remains constant).
Depending on the load current, the converter operates in continuous conduction mode (CCM), discontinuous conduction mode (DCM), or pulse skip mode to maintain the output voltage.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

### 7.3.1 Soft Start

The boost converter has an adjustable soft start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor connected to the soft-start pin SS is used to slowly ramp up the internal current limit of the boost converter when charged with a constant current. When the EN pin is pulled high, the soft-start capacitor $\left(\mathrm{C}_{\mathrm{Ss}}\right)$ is immediately charged to 0.3 V . The capacitor is then charged at a constant current of $10 \mu \mathrm{~A}$ typically until the output of the boost converter $\mathrm{V}_{\mathrm{S}}$ has reached its power good threshold ( $90 \%$ of $\mathrm{V}_{\mathrm{S}}$ nominal value). During this time, the SS voltage directly controls the peak inductor current, starting with 0 A at $\mathrm{V}_{\mathrm{SS}}=0.3 \mathrm{~V}$ up to the full current limit at $\mathrm{V}_{S S} \approx 800 \mathrm{mV}$. The maximum load current is available after the soft start is completed. The larger the capacitor the slower the ramp of the current limit and the longer the soft-start time. A $100-\mathrm{nF}$ capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.

### 7.3.2 Frequency Select Pin (FREQ)

The frequency select pin FREQ allows to set the switching frequency of the device to 650 kHz (FREQ = low) or 1.2 MHz (FREQ = high). Higher switching frequency improves load transient response but reduces slightly the efficiency. The other benefits of higher switching frequency are a lower output ripple voltage and smaller inductor size. Usually, TI recommends using $1.2-\mathrm{MHz}$ switching frequency unless light-load efficiency is a major concern.

### 7.3.3 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.2 V .

### 7.3.4 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown threshold is at $\mathrm{T}_{J}=150^{\circ} \mathrm{C}$. When the thermal shutdown is triggered the device stops switching until the temperature falls below typically $\mathrm{T}_{J}=136^{\circ} \mathrm{C}$. Then the device starts switching again.

### 7.3.5 Overvoltage Prevention

If overvoltage is detected on the FB pin (typically $3 \%$ above the nominal value of 1.238 V ) the part stops switching immediately until the voltage on this pin drops to its nominal value. This prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

### 7.4 Device Functional Modes

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor. For lower load currents it switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

## 8 Application and Implementation

## NOTE

Information in the following applications sections is not part of the Tl component specification, and TI does not warrant its accuracy or completeness. Tl's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

With the TPS61085A-Q1 device, a boost regulator with an output voltage of up to 18.5 V can be designed with input voltage ranging from 2.3 V to 6 V . The TPS61085A-Q1 device has a peak switch current limit of 2 A minimum. The device, which operates in a current mode scheme and uses simple external compensation scheme for maximum flexibility and stability. Selectable switching frequency allows the regulator to be optimized either for smaller size ( 1.2 MHz ) or for higher system efficiency ( 650 KHz ). A dedicated soft-start (SS) pin allows the designer to control the inrush current at start-up.
The following section provides a step-by-step design approach for configuring the TPS61085A-Q1 as a voltage regulating boost converter.

### 8.2 Typical Application



Figure 8. Typical Application, 3.3 V to $12 \mathrm{~V}\left(\mathrm{f}_{\mathrm{sw}}=1.2 \mathrm{MHz}\right)$

### 8.2.1 Design Requirements

Table 2 lists the design parameters for this application example.
Table 2. TPS61085A-Q1 Output Design Requirements

| PARAMETER | VALUE |
| :---: | :---: |
| Input voltage | $3.3 \mathrm{~V} \pm 20 \%$ |
| Output voltage | 12 V |
| Output current | 600 mA |
| Switching frequency | 1.2 MHz |

### 8.2.2 Detailed Design Procedure

The first step in the design procedure is to verify that the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst-case assumption for the expected efficiency, for example, $90 \%$.

1. Duty cycle:

$$
\begin{equation*}
D=1-\frac{V_{I N} \times \eta}{V_{S}} \tag{1}
\end{equation*}
$$

2. Maximum output current:

$$
\begin{equation*}
\text { Iout }=\left(I_{\text {swpeak }}-\frac{\Delta I_{L}}{2}\right) \times(1-D) \tag{2}
\end{equation*}
$$

3. Peak switch current:

$$
I_{\text {swpeak }}=\frac{\Delta I_{L}}{2}+\frac{I_{\text {out }}}{1-D}
$$

where

$$
\Delta I_{L}=\frac{V_{I N} \times D}{f_{S} \times L}
$$

- $\mathrm{I}_{\text {swpeak }}=$ converter switch current (minimum switch current limit $=2 \mathrm{~A}$ )
- fs = Converter switching frequency (typically 1.2 MHz )
- $\mathrm{L}=$ Selected inductor value
- $\eta=$ Estimated converter efficiency (please use the number from the efficiency plots or $90 \%$ as an estimation)
- $\Delta \mathrm{L}_{\mathrm{L}}=$ Inductor peak-to-peak ripple current

The peak switch current is the steady-state peak switch current that the integrated switch, inductor, and external Schottky diode must be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

### 8.2.2.1 Inductor Selection

The TPS61085A-Q1 is designed to work with a wide range of inductors. The main parameter for the inductor selection is the saturation current of the inductor which must be higher than the peak switch current as calculated in Detailed Design Procedure with additional margin to cover for heavy load transients. An alternative, more conservative option is to choose an inductor with a saturation current at least as high as the maximum switch current limit of 3.2 A. The other important parameter is the inductor DC resistance. Usually, the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. At high switching frequencies of $1.2-\mathrm{MHz}$ inductor core losses, proximity effects and skin effects become more important. Usually, an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between $2 \%$ to $10 \%$. For the TPS61085A-Q1, inductor values between $3 \mu \mathrm{H}$ and $6 \mu \mathrm{H}$ are a good choice with a switching frequency of 1.2 MHz , typically $3.3 \mu \mathrm{H}$. At 650 kHz , TI recommends inductors between $6 \mu \mathrm{H}$ and 13 $\mu \mathrm{H}$, typically $6.8 \mu \mathrm{H}$. Table 3 shows a few inductors. Customers must verify and validate these components for suitability with their application before using them.
Typically, TI recommends the inductor current ripple is below $20 \%$ of the average inductor current. Calculate the inductor value using Equation 4.

$$
\mathrm{L}=\left(\frac{\mathrm{VIN}}{\mathrm{Vs}}\right)^{2} \times\left(\frac{\mathrm{Vs}^{2}-\mathrm{VIN}_{\text {I }}}{\text { Iout_max } \times \mathrm{f}}\right) \times\left(\frac{\eta}{0.35}\right)
$$

where

- $L$ is the inductor value
- $\mathrm{V}_{\text {IN }}$ is input voltage
- $\mathrm{V}_{\mathrm{S}}$ is boost output voltage
- $\eta$ is efficiency
- $\mathrm{I}_{\text {out_max }}$ is the maximum output current
- $f$ is frequency

Table 3. Inductor Selection

| $\mathbf{L}$ <br> $(\boldsymbol{\mu H})$ | SUPPLIER ${ }^{(1)}$ | COMPONENT <br> CODE | SIZE <br> $(\mathbf{L} \times \mathbf{W} \times \mathbf{H} \mathbf{~ m m})$ | DCR TYP <br> $(\mathbf{m \Omega} \boldsymbol{\Omega})$ | Isat (A) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{1 . 2 ~ M H z ~}$ |  |  |  |  |  |
| 3.3 | Sumida | CDH38D09 | $4 \times 4 \times 1$ | 240 | 1.25 |
| 4.7 | Sumida | CDPH36D13 | $5 \times 5 \times 1.5$ | 155 | 1.36 |
| 3.3 | Sumida | CDPH4D19F | $5.2 \times 5.2 \times 2$ | 33 | 1.5 |
| 3.3 | Sumida | CDRH6D12 | $6.7 \times 6.7 \times 1.5$ | 62 | 2.2 |
| 4.7 | Würth Elektronik | 7447785004 | $5.9 \times 6.2 \times 3.3$ | 60 | 2.5 |
| 5 | Coilcraft | MSS7341 | $7.3 \times 7.3 \times 4.1$ | 24 | 2.9 |
|  |  |  |  |  |  |
| 6.8 | Sumida | CDP14D19 | $5.2 \times 5.2 \times 2$ | 50 | 1 |
| 10 | Coilcraft | LPS4414 | $4.3 \times 4.3 \times 1.4$ | 380 | 1.2 |
| 6.8 | Sumida | CDRH6D12/LD | $6.7 \times 6.7 \times 1.5$ | 95 | 1.25 |
| 10 | Sumida | CDR6D23 | $5 \times 5 \times 2.4$ | 133 | 1.75 |
| 10 | Würth Elektronik | 744778910 | $7.3 \times 7.3 \times 3.2$ | 51 | 2.2 |
| 6.8 | Sumida | CDRH6D26HP | $7 \times 7 \times 2.8$ | 52 | 2.9 |

(1) See Third-party Products Disclaimer

### 8.2.2.2 Rectifier Diode Selection

To achieve high efficiency, a Schottky type must be used for the rectifier diode. The reverse voltage rating must be higher than the maximum output voltage of the converter. The averaged rectified forward current $\mathrm{l}_{\text {avg }}$, the Schottky diode requirement is rated for, is equal to the output current $\mathrm{l}_{\text {out }}$ :

$$
\begin{equation*}
I_{\text {avg }}=I_{\text {out }} \tag{5}
\end{equation*}
$$

Usually a Schottky diode with 2-A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current $\mathrm{I}_{\text {out }}$ but must be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

$$
\begin{equation*}
P_{D}=I_{\text {avg }} \times V_{\text {forward }} \tag{6}
\end{equation*}
$$

Typically the diode must be able to dissipate around 500 mW depending on the load current and forward voltage. See Table 4 for few diode options. Customers must verify and validate these components for suitability with their application before using them.

Table 4. Rectifier Diode Selection

| CURRENT <br> RATING (lavg) | $\mathbf{V r}$ | $\mathbf{V}_{\text {forward } / \text { lavg }}$ | SUPPLIER $^{(1)}$ | COMPONENT <br> CODE | PACKAGE <br> TYPE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 750 mA | 20 V | $0.425 \mathrm{~V} /$ <br> 750 mA | Fairchild Semiconductor | FYV0704S | SOT-23 |
| 1 A | 20 V | $0.39 \mathrm{~V} / 1 \mathrm{~A}$ | NXP | PMEG2010AEH | SOD-123 |
| 1 A | 20 V | $0.52 \mathrm{~V} / 1 \mathrm{~A}$ | Vishay Semiconductor | B120 | SMA |
| 1 A | 20 V | $0.5 \mathrm{~V} / 1 \mathrm{~A}$ | Vishay Semiconductor | SS12 | SMA |
| 1 A | 20 V | $0.44 \mathrm{~V} / 1 \mathrm{~A}$ | Vishay Semiconductor | MSS1P2L | $\mu-$ SMP <br> (Low Profile) |

(1) See Third-party Products Disclaimer

### 8.2.2.3 Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of $50 \mu \mathrm{~A}$ flowing through the feedback divider gives good accuracy and noise covering. A standard low-side resistor of $18 \mathrm{k} \Omega$ is typically selected. The resistors are then calculated as:

$$
\begin{equation*}
R 2=\frac{V r e f}{70 \mu A} \approx 18 k \Omega \quad R 1=R 2 \times\left(\frac{V S}{V r e f}-1\right) \tag{7}
\end{equation*}
$$

### 8.2.2.4 Compensation (COMP)

The regulator loop must be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. Standard values of $R_{\text {COMP }}=13 \mathrm{k} \Omega$ and $\mathrm{C}_{\text {COMP }}=3.3 \mathrm{nF}$ works for the majority of the applications.
See Table 5 for dedicated compensation networks giving an improved load transient response. Equation 8 can be used to calculate $\mathrm{R}_{\text {Сомр }}$ and $\mathrm{C}_{\text {сомр }}$ :

$$
\begin{equation*}
R_{\text {COMP }}=\frac{110 \cdot V_{I N} \cdot V_{S} \cdot C_{\text {OUT }}}{L \cdot I_{\text {OUT }}} \quad C_{\text {COMP }}=\frac{V_{S} \cdot C_{\text {OUT }}}{7.5 \cdot I_{\text {OUT }} \cdot R_{\text {COMP }}} \tag{8}
\end{equation*}
$$

Table 5. Recommended Compensation Network Values at High/Low Frequency

| FREQUENCY | L | $\mathrm{V}_{\text {S }}$ | $\mathrm{V}_{\text {IN }} \pm 20 \%$ | $\mathbf{R}_{\text {COMP }}$ | $\mathrm{C}_{\text {COMP }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High (1.2 MHz) | $3.3 \mu \mathrm{H}$ | 15 V | 5 V | $82 \mathrm{k} \Omega$ | 1.1 nF |
|  |  |  | 3.3 V | $75 \mathrm{k} \Omega$ | 1.6 nF |
|  |  | 12 V | 5 V | $51 \mathrm{k} \Omega$ | 1.1 nF |
|  |  |  | 3.3 V | $47 \mathrm{k} \Omega$ | 1.6 nF |
|  |  | 9 V | 5 V | $30 \mathrm{k} \Omega$ | 1.1 nF |
|  |  |  | 3.3 V | $27 \mathrm{k} \Omega$ | 1.6 nF |
| Low (650 kHz) | $6.8 \mu \mathrm{H}$ | 15 V | 5 V | $43 \mathrm{k} \Omega$ | 2.2 nF |
|  |  |  | 3.3 V | $39 \mathrm{k} \Omega$ | 3.3 nF |
|  |  | 12 V | 5 V | $27 \mathrm{k} \Omega$ | 2.2 nF |
|  |  |  | 3.3 V | $24 \mathrm{k} \Omega$ | 3.3 nF |
|  |  | 9 V | 5 V | $15 \mathrm{k} \Omega$ | 2.2 nF |
|  |  |  | 3.3 V | $13 \mathrm{k} \Omega$ | 3.3 nF |

Table 5 gives conservatives $\mathrm{R}_{\text {СомP }}$ and $\mathrm{C}_{\text {COMP }}$ values for certain inductors, input and output voltages providing a very stable system. For a faster response time, a higher $\mathrm{R}_{\text {сомр }}$ value can be used to enlarge the bandwidth, as well as a slightly lower value of $\mathrm{C}_{\text {comp }}$ to keep enough phase margin. These adjustments must be performed in parallel with the load transient response monitoring of TPS61085A-Q1.

### 8.2.2.5 Input Capacitor Selection

For good input voltage filtering, TI recommends low-ESR ceramic capacitors. TPS61085A-Q1 has an analog input (IN). Therefore, TI highly recommends placing a $1-\mathrm{uF}$ bypass capacitor as close as possible to the IC from IN to GND.
One $10-\mu \mathrm{F}$ ceramic input capacitor is sufficient for most of the applications. For better input voltage, filtering this value can be increased. Refer to Table 6 and typical applications for input capacitor recommendations. Customers must verify and validate these components for suitability with their application before using them.

### 8.2.2.6 Output Capacitor Selection

For best output voltage filtering, TI recommends a low ESR output capacitor like ceramic capacitor. Two $10-\mu \mathrm{F}$ ceramic output capacitors (or one $22-\mu \mathrm{F}$ ) work for most of the applications. Higher capacitor values can be used to improve the load transient response.
Pay attention to the derating of capacitor value with the DC voltage.
Table 6. Rectifier Input and Output Capacitor Selection

|  | CAPACITOR | VOLTAGE RATING | SUPPLIER $^{\left({ }^{(1)}\right.}$ | COMPONENT CODE |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\mathrm{IN}}$ | $10 \mu \mathrm{~F} / 1206$ | 16 V | Taiyo Yuden | EMK212 BJ 106KG |
| $\mathrm{IN}_{\mathrm{N}}$ bypass | $1 \mu \mathrm{~F} / 0603$ | 16 V | Taiyo Yuden | EMK107 BJ 105KA |
| $\mathrm{C}_{\text {Out }}$ | $10 \mu \mathrm{~F} / 1206$ | 25 V | Taiyo Yuden | TMK316 BJ 106KL |

(1) See Third-party Products Disclaimer

### 8.2.3 Application Curves



### 8.3 System Examples

Figure 14 to Figure 21 show application circuit examples using the TPS61085A-Q1 device. These circuits must be fully validated and tested by customers before using these circuits in their designs. TI does not warrant the accuracy or completeness of these circuits, nor does TI accept any responsibility for them.


Figure 14. Typical Application, 3.3 V to 12 V ( $\mathrm{f}_{\mathrm{sw}}=650 \mathrm{kHz}$ )


Figure 15. Typical Application, 3.3 V to $9 \mathrm{~V}\left(\mathrm{f}_{\mathrm{sw}}=1.2 \mathrm{MHz}\right)$

TPS61085A-Q1
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## System Examples (continued)



Figure 16. Typical Application, 3.3 V to $9 \mathrm{~V}\left(\mathrm{f}_{\mathrm{sw}}=650 \mathrm{kHz}\right)$


Figure 17. Typical Application With External Load Disconnect Switch

## System Examples (continued)



Figure 18. Typical Application 3.3 V to $9 \mathrm{~V}\left(\mathrm{f}_{\mathrm{sw}}=1.2 \mathrm{MHz}\right.$ ) For TFT LCD With External Charge Pumps (VGH, VGL)


Figure 19. Simple Application (5-V Input, $\mathrm{f}_{\mathrm{sw}}=650 \mathrm{kHz}$ ) For wLED Supply (3S3P) (With Optional Clamping Zener Diode)

## System Examples (continued)



Figure 20. Simple Application (3.3-V Input, $\mathrm{f}_{\mathrm{sw}}=\mathbf{6 5 0} \mathbf{k H z}$ ) For wLED Supply (3S3P) With Adjustable Brightness Control

Using a PWM Signal on the Enable Pin
(With Optional Clamping Zener Diode)


Figure 21. Simple Application (3.3-V Input, $\mathrm{f}_{\text {sw }}=650 \mathrm{kHz}$ ) For wLED Supply (3S3P) With Adjustable Brightness Control Using an Analog Signal on the Feedback Pin
(With Optional Clamping Zener Diode)

## 9 Power Supply Recommendations

The TPS61085A-Q1 is designed to operate from an input voltage supply range from 2.3 V to 6 V . The required power supply for the TPS61085A-Q1 must have a current rating according to the output voltage and output current of the TPS61085A-Q1.

## 10 Layout

### 10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.
Layout Example provides an example of layout design with the TPS61085A-Q1 device.

- Use wide and short traces for the main current path and for the power ground tracks.
- The input capacitor, output capacitor, and the inductor must be placed as close as possible to the IC.
- Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at the GND terminal of the IC.
- The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces must be placed on the same board layer as the IC and as close as possible between the SW pin and the GND terminal of the IC.


### 10.2 Layout Example



Figure 22. TPS61085A-Q1 Layout Example

## 11 Device and Documentation Support

### 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to Tl community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute Tl specifications and do not necessarily reflect Tl's views; see Tl's Terms of Use.

TI E2E ${ }^{\text {TM }}$ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.
Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.
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### 11.5 Electrostatic Discharge Caution <br> $\xrightarrow{\Delta}$ <br> These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

SLYZ022 - TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status <br> (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <br> (2) | Lead finish/ Ball material (6) | MSL Peak Temp <br> (3) | Op Temp ( ${ }^{\circ} \mathrm{C}$ ) | Device Marking <br> (4/5) | Samples |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TPS61085ATDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2000 | RoHS \& Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | 1EGV | Samples |
| TPS61085ATDGKTQ1 | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS \& Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | 1EGV | Samples |

${ }^{(1)}$ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
${ }^{(2)}$ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed $0.1 \%$ by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as " Pb -Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the $<=1000 \mathrm{ppm}$ threshold requirement.
${ }^{(3)}$ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
${ }^{(4)}$ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
${ }^{(5)}$ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a " $\sim$ " will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
${ }^{(6)}$ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel <br> Width <br> W1 (mm) | $\begin{gathered} \mathrm{AO} \\ (\mathrm{~mm}) \end{gathered}$ | $\begin{gathered} \mathrm{BO} \\ (\mathrm{~mm}) \end{gathered}$ | $\begin{gathered} \text { K0 } \\ (\mathrm{mm}) \end{gathered}$ | $\begin{gathered} \text { P1 } \\ (\mathrm{mm}) \end{gathered}$ | $\begin{gathered} \mathrm{W} \\ (\mathrm{~mm}) \end{gathered}$ | Pin1 Quadrant |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TPS61085ATDGKRQ1 | VSSOP | DGK | 8 | 2000 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS61085ATDGKTQ1 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TPS61085ATDGKRQ1 | VSSOP | DGK | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TPS61085ATDGKTQ1 | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

## DGK (S-PDSO-G8)

## PLAStic SmALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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