

3.3-V/5-V Input, 6-A, D-CAP+™ Mode Synchronous Step-Down Integrated FETs Converter

Check for Samples: [TPS51317](#)

FEATURES

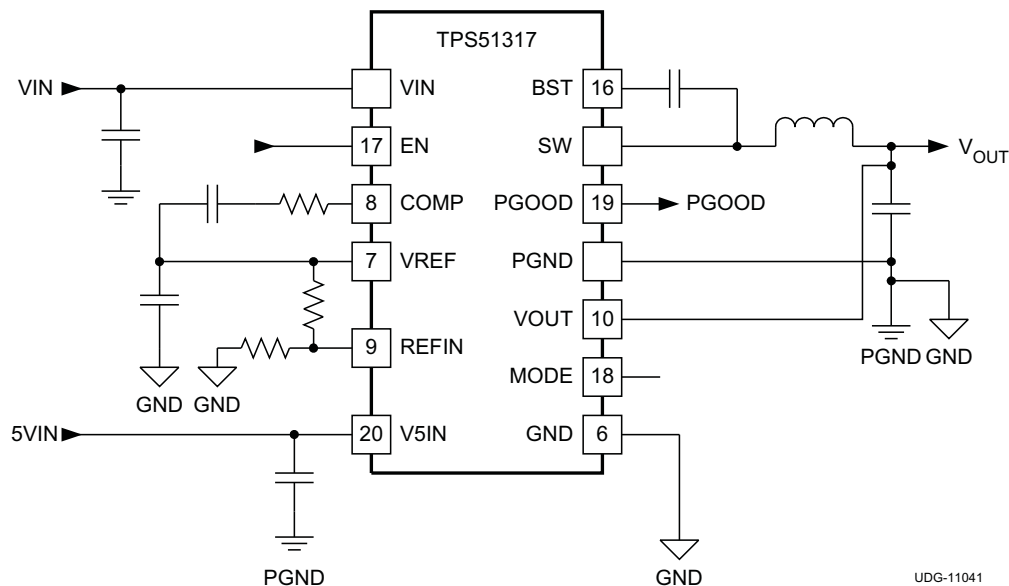
- **Integrated FETs Converter w/TI Proprietary D-CAP+™ Mode Architecture**
- **Minimum External Components Count**
- **Support all MLCC Output Capacitor and SP/POSCAP**
- **Auto-Skip Mode and Ripple Reduction Mode**
- **Optimized Efficiency at Light and Heavy Loads**
- **Selectable 800-kHz, 1-MHz, 1.2-MHz and 1.5-MHz Frequency**
- **Up to 6.0-V Conversion Voltage Range**
- **Adjustable Output Voltage Range From 0.6 V to 2 V**
- **Small 3.5 mm × 4 mm, 20-Pin QFN Package**

DESCRIPTION

The TPS51317 is a fully integrated synchronous buck regulator employing D-CAP+™ mode architecture. It is used for 3.3-V and 5-V step-down systems where space is a consideration, high-performance and optimized component count are required. The TPS51317 features four switching frequency settings (up to 1.5 MHz), synchronous operation in SKIP, droop support, external tracking support, pre-bias startup, output soft discharge, integrated bootstrap switch, power good function, enable function and complete protection functions, and both output ceramic and SP/POS capacitor support. It supports supply and conversion voltages up to 6.0 V, and output voltages adjustable from 0.6 V to 2.0V. The TPS51317 is available in the 3.5 mm × 4 mm 20-pin QFN package (Green RoHS compliant and Pb free) and is specified from -40°C to 85°C.

APPLICATIONS

- **Low-Voltage Applications Stepping Down from 5-V or 3.3-V Rail**



UDG-11041



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP+ is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | ORDERING NUMBER | PINS | OUTPUT SUPPLY | MINIMUM QUANTITY | ECO PLAN |
|----------------|------------------------|-----------------|------|---------------|------------------|---------------------------|
| -40°C to 85°C | Plastic QFN (RGB) | TPS51317RGBR | 20 | Tape and reel | 3000 | Green (RoHS and no Pb/Br) |
| | | TPS51317RGBT | 20 | Mini reel | 250 | |

- (1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | TPS51317 | UNITS |
|-------------------------------|---|----------|-------|
| | | RGB | |
| | | 20 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 35.5 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 39.6 | |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 12.4 | |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 0.5 | |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 12.5 | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | 3.7 | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | | UNIT | |
|--|-------------------------------------|-------|------|------|----|
| | | MIN | MAX | | |
| Input voltage range | VIN, V5IN, BST (with respect to SW) | -0.3 | 7.0 | V | |
| | BST | -0.3 | 14.0 | | |
| | SW | -2 | 7 | | |
| | EN | -0.3 | 7 | | |
| | MODE, REFIN | -0.3 | 3.6 | | |
| | VOUT | -1 | 3.6 | | |
| Output voltage range | COMP, VREF | -0.3 | 3.6 | V | |
| | PGOOD | -0.3 | 7.0 | | |
| | PGND | -0.3 | 0.3 | | |
| Junction temperature | T _J | -40 | 150 | | |
| Storage temperature | T _{stg} | -55 | 150 | °C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | | | 300 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | VALUE | | | UNIT |
|---|-------------------|-------|-----|------|------|
| | | MIN | TYP | MAX | |
| Input voltage range | VIN | -0.1 | | 6.5 | V |
| | V5IN | 4.5 | | 6.5 | |
| | BST | -0.1 | | 13.5 | |
| | SW | -1.0 | | 6.5 | |
| | EN | -0.7 | | 6.5 | |
| | VOUT, MODE, REFIN | -0.1 | | 3.5 | |
| Output voltage range | COMP, VREF | -0.1 | | 3.5 | V |
| | PGOOD | -0.1 | | 5.5 | |
| | PGND | -0.1 | | 0.1 | |
| Operating temperature range, T _A | | -40 | | 85 | °C |

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, $V_{V5IN} = 5.0\text{ V}$, PGND = GND (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|-------|-------|-------|------------------|
| SUPPLY: VOLTAGE, CURRENTS AND 5 V UVLO | | | | | | |
| I_{VINSD} | VIN shutdown current | EN = 'LO' | | 0.02 | 5 | μA |
| V_{5VIN} | 5VIN supply voltage | V5IN voltage range | 4.5 | 5.0 | 6.5 | V |
| I_{5VIN} | 5VIN supply current | EN = 'HI', V5IN supply current | | 1.1 | 2 | mA |
| I_{5VINSD} | 5VIN shutdown current | EN = 'LO', V5IN shutdown current | | 0.2 | 7.0 | μA |
| V_{V5UVLO} | V5IN UVLO | Ramp up; EN = 'HI' | 4.20 | 4.37 | 4.50 | V |
| $V_{V5UVHYS}$ | V5IN UVLO hysteresis | Falling hysteresis | | 440 | | mV |
| $V_{VREFUVLO}$ | REF UVLO ⁽¹⁾ | Rising edge of VREF, EN = 'HI' | | 1.8 | | V |
| $V_{VREFUVHYS}$ | REF UVLO hysteresis ⁽¹⁾ | | | 100 | | mV |
| $V_{POR5VFILT}$ | Reset | OVP latch is reset by V5IN falling below the reset threshold | 1.5 | 2.3 | 3.1 | V |
| VOLTAGE FEEDBACK LOOP: VREF, VOUT, AND VOLTAGE GM AMPLIFIER | | | | | | |
| V_{OUTTOL} | VOUT accuracy | $V_{REFIN} = 1\text{ V}$, No droop | -1% | 0% | 1% | |
| V_{VREF} | VREF | $I_{VREF} = 0\ \mu\text{A}$ | 1.98 | 2.00 | 2.02 | V |
| | | $I_{VREF} = 50\ \mu\text{A}$ | 1.975 | 2.000 | 2.025 | |
| I_{REFSNK} | VREF sink current | $V_{VREF} = 2.05\text{ V}$ | | 2.5 | | mA |
| G_M | Transconductance | | | 1.00 | | mS |
| V_{CM} | Common mode input voltage range ⁽¹⁾ | | 0 | | 2 | V |
| V_{DM} | Differential mode input voltage | | 0 | | 80 | mV |
| $I_{COMPSNK}$ | COMP pin maximum sinking current | $V_{COMP} = 2\text{ V}$, $(V_{REFIN} - V_{OUT}) = 80\text{ mV}$ | | 80 | | μA |
| $I_{COMPSRC}$ | COMP pin maximum sourcing current | $V_{COMP} = 2\text{ V}$ | | -80 | | μA |
| V_{OFFSET} | Input offset voltage | $T_A = 25^\circ\text{C}$ | | 0 | | mV |
| R_{DSCH} | Output voltage discharge resistance | | | 42 | | Ω |
| f_{-3dBVL} | -3dB Frequency ⁽¹⁾ | | 4.5 | 6.0 | 7.5 | MHz |
| CURRENT SENSE: CURRENT SENSE AMPLIFIER, OVERCURRENT AND ZERO CROSSING | | | | | | |
| A_{CSINT} | Internal current sense gain | Gain from the current of the low-side FET to PWM comparator when PWM = "OFF" | 43 | 53 | 57 | mV/A |
| I_{OCL} | Positive overcurrent limit (valley) | | | 7.6 | | A |
| $I_{OCL(neg)}$ | Negative overcurrent limit (valley) | | | -9.3 | | A |
| V_{ZXOFF} | Zero crossing comp internal offset | | | 0 | | mV |
| DRIVERS: BOOT STRAP SWITCH | | | | | | |
| $R_{DSONBST}$ | Internal BST switch on-resistance | $I_{BST} = 10\text{ mA}$, $T_A = 25^\circ\text{C}$ | | | 10 | Ω |
| I_{BSTLK} | Internal BST switch leakage current | $V_{BST} = 14\text{ V}$, $V_{SW} = 7\text{ V}$ | | | 1 | μA |
| PROTECTION: OVP, UVP, PGOOD, and THERMAL SHUTDOWN | | | | | | |
| V_{PGDLL} | PGOOD deassert to lower (PGOOD \rightarrow Low) | Measured at the VOUT pin wrt/ V_{REFIN} | | 84% | | |
| V_{PGHSHL} | PGOOD high hysteresis | | | 8% | | |
| V_{PGDLH} | PGOOD de-assert to higher (PGOOD \rightarrow Low) | Measured at the VOUT pin wrt/ V_{REFIN} | | 116% | | |
| V_{PGHSHH} | PGOOD high hysteresis | | | -8% | | |
| $V_{INMINPG}$ | Minimum VIN voltage for valid PGOOD | Measured at the VIN pin with a 2-mA sink current on PGOOD pin | 0.9 | 1.3 | 1.5 | V |
| V_{OVP} | OVP threshold | Measured at the VOUT pin wrt/ V_{REFIN} | 117% | 120% | 123% | |
| V_{UVP} | UVP threshold | Measured at the VOUT pin wrt/ V_{REFIN} , device latches OFF, begins soft-stop | 65% | 68% | 71% | |
| TH_{SD} | Thermal shutdown ⁽¹⁾ | Latch off controller, attempt soft-stop. | | 145 | | $^\circ\text{C}$ |
| $TH_{SD(hys)}$ | Thermal Shutdown hysteresis ⁽¹⁾ | Controller re-starts after temperature has dropped | | 10 | | $^\circ\text{C}$ |

(1) Ensured by design, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, $V_{V5IN} = 5.0\text{ V}$, $PGND = GND$ (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---------------------------------------|--|------|------|------|------|
| TIMERS: ON-TIME, MINIMUM OFF-TIME, SS, AND I/O TIMINGS | | | | | | |
| $t_{ONESHOTC}$ | PWM one-shot ⁽²⁾ | $V_{VIN} = 5\text{ V}$, $V_{VOUT} = 1.05\text{ V}$, $f_{SW} = 860\text{ KHz}$ | | 240 | | ns |
| | | $V_{VIN} = 5\text{ V}$, $V_{VOUT} = 1.05\text{ V}$, $f_{SW} = 1\text{ MHz}$ | | 210 | | |
| | | $V_{VIN} = 5\text{ V}$, $V_{VOUT} = 1.05\text{ V}$, $f_{SW} = 1.2\text{ MHz}$ | | 175 | | |
| | | $V_{VIN} = 5\text{ V}$, $V_{VOUT} = 1.05\text{ V}$, $f_{SW} = 1.5\text{ MHz}$ | | 140 | | |
| $t_{MIN(off)}$ | Minimum OFF time | $V_{VIN} = 5\text{ V}$, $V_{VOUT} = 1.05\text{ V}$, $f_{SW} = 1\text{ MHz}$, DRVL on, SW = PGND, $V_{VOUT} < V_{REFIN}$ | | 360 | | ns |
| $t_{INT(SS)}$ | Soft-start time | From EN = HI to VOUT =95%, default setting | | 1.6 | | ms |
| $t_{INT(SSDLY)}$ | Internal soft-start delay time | From EN = HI to VOUT ramp starts | | 260 | | µs |
| t_{PGDDL} | PGOOD startup delay time | External tracking | | 8 | | ms |
| $t_{PGDPDLYH}$ | PGOOD high propagation delay time | 50 mV over drive, rising edge | 0.8 | 1 | 1.2 | ms |
| $t_{PGDPDLYL}$ | PGOOD low propagation delay time | 50 mV over drive, falling edge | | 10 | | µs |
| t_{OVPDLY} | OVP delay time | Time from the VOUT pin out of +20% of REFIN to OVP fault | | 10 | | µs |
| $t_{UVLDYEN}$ | Undervoltage fault enable delay | Time from EN_INT going high to undervoltage fault is ready | | 2 | | ms |
| | | External tracking from VOUT ramp starts | | 8 | | |
| t_{UVPDLY} | UVP delay time | Time from the VOUT pin out of -30% of REFIN to UVP fault | | 256 | | µs |
| LOGIC PINS: I/O VOLTAGE AND CURRENT | | | | | | |
| V_{PGDPD} | PGOOD pull-down voltage | PGOOD low impedance, $I_{SINK} = 4\text{ mA}$, $V_{V5IN} = 4.5\text{ V}$ | | | 0.3 | V |
| I_{PGDLKG} | PGOOD leakage current | PGOOD high impedance, forced to 5.5 V | -1 | 0 | 1 | µA |
| V_{ENH} | EN logic high | EN, VCCP logic | 2 | | | V |
| V_{ENL} | EN logic low | EN, VCCP logic | | | 0.5 | V |
| I_{EN} | EN input current | | | | 1 | µA |
| V_{MODETH} | MODE threshold voltage ⁽³⁾ | Threshold 1 | 80 | 130 | 180 | mV |
| | | Threshold 2 | 200 | 250 | 300 | |
| | | Threshold 3 | 370 | 420 | 470 | |
| | | Threshold 4 | 1.77 | 1.80 | 1.85 | |
| I_{MODE} | MODE current | | | 15 | | µA |

(2) Ensured by design, not production tested.

(3) See [Table 4](#) for descriptions of MODE parameters.

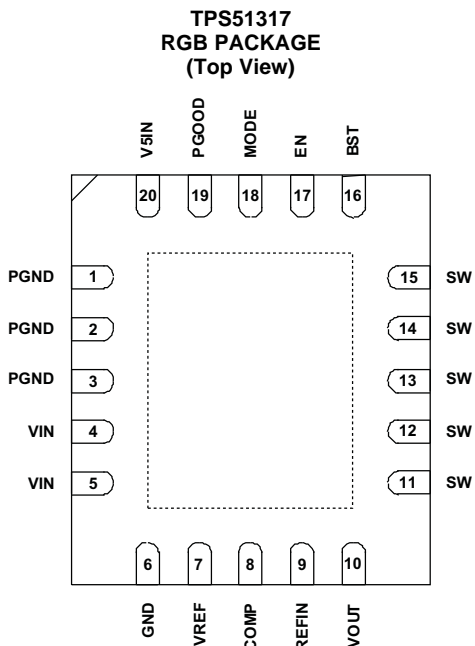
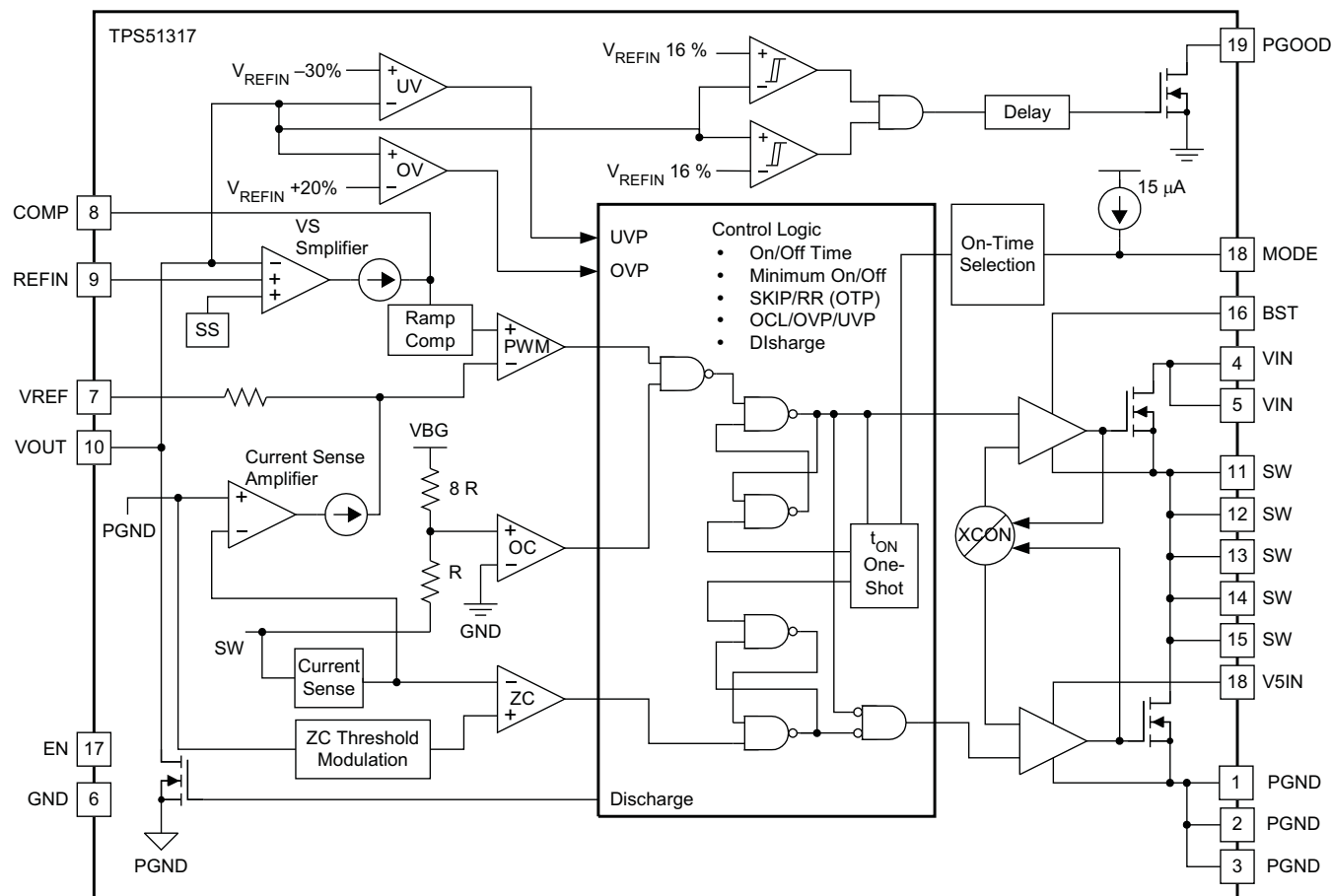


Table 2. PIN FUNCTIONS

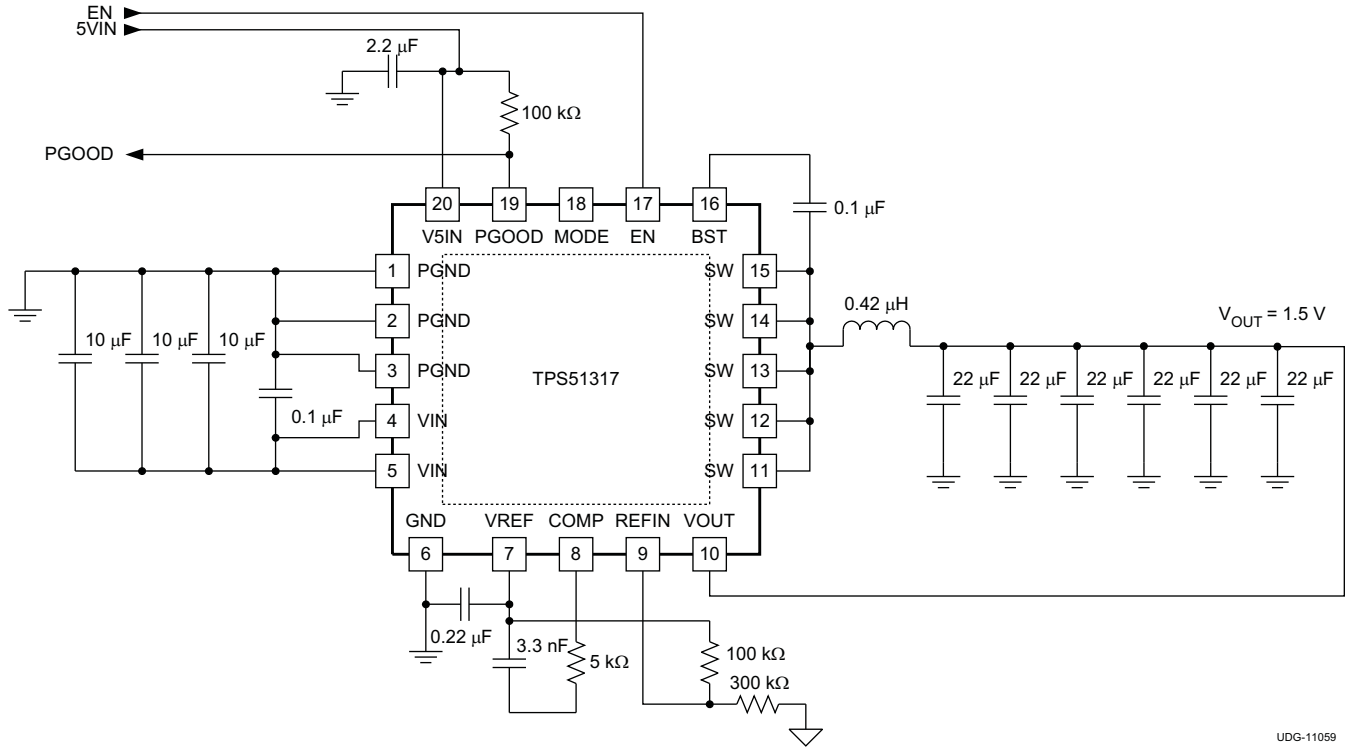
| PIN | | I/O | DESCRIPTION |
|-----|-------|-----|--|
| NO. | NAME | | |
| 16 | BST | I | Power supply for internal high-side gate driver. Connect a 0.1- μ F bootstrap capacitor between this pin and the SW pin. |
| 8 | COMP | O | Connect series R-C filter between this pin and VREF for loop compensation. |
| 17 | EN | I | Enable of the SMPS (3.3-V logic compatible). |
| 6 | GND | – | Signal ground. |
| 18 | MODE | I | Allows selection of switching frequencies light-load modes. (See Table 4) |
| 1 | PGND | I | Power ground. Source terminal of the rectifying low-side power FET. Positive input for current sensing. |
| 2 | | | |
| 3 | | | |
| 19 | PGOOD | O | Power good output. Connect pull-up resistor. |
| 9 | REFIN | | Target output voltageinput pin. Apply voltage between 0.6 V to 2.0 V. |
| 11 | SW | I/O | Switching node output. Connect to the external inductor. Also serve as current-sensing negative input. |
| 12 | | | |
| 13 | | | |
| 14 | | | |
| 15 | | | |
| 20 | V5IN | I | 5-V power supply for analog circuits and gate drive. |
| 4 | VIN | I | Power supply input pin. Drain terminal of the switching high-side power FET. |
| 5 | | | |
| 10 | VOUT | I | Output voltage monitor input pin. |
| 7 | VREF | O | 2.0-V reference output. Connect a 0.22- μ F ceramic capacitor to GND. |

BLOCK DIAGRAM



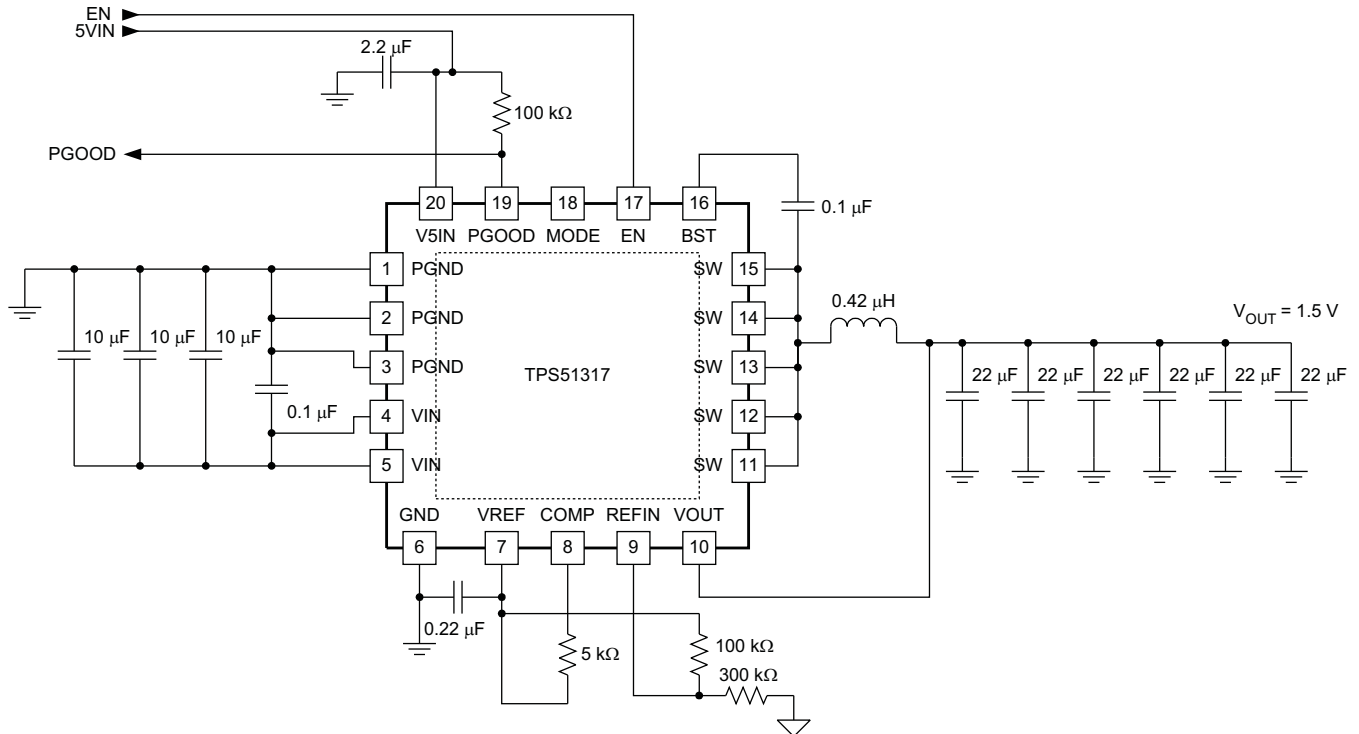
UDG-11058

APPLICATION SCHEMATIC WITH TPS51317



UDG-11059

Figure 1. Application Using Non-Droop Configuration



UDG-11060

Figure 2. Application Using Droop Configuration

Application Circuit List of Materials

Recommended parts for key external components for the circuits in [Figure 1](#) and [Figure 2](#) are listed in [Table 3](#).

**Table 3. Key External Component Recommendations
([Figure 1](#) and [Figure 2](#))**

| FUNCTION | MANUFACTURER | PART NUMBER |
|---------------------------|--------------|--------------------|
| Output Inductor | Nec-Tokin | MPCG0740LR42C |
| Ceramic Output Capacitors | Panasonic | ECJ2FB0J226M |
| | Murata | GRM21BR60J226ME39L |

APPLICATION INFORMATION

Functional Overview

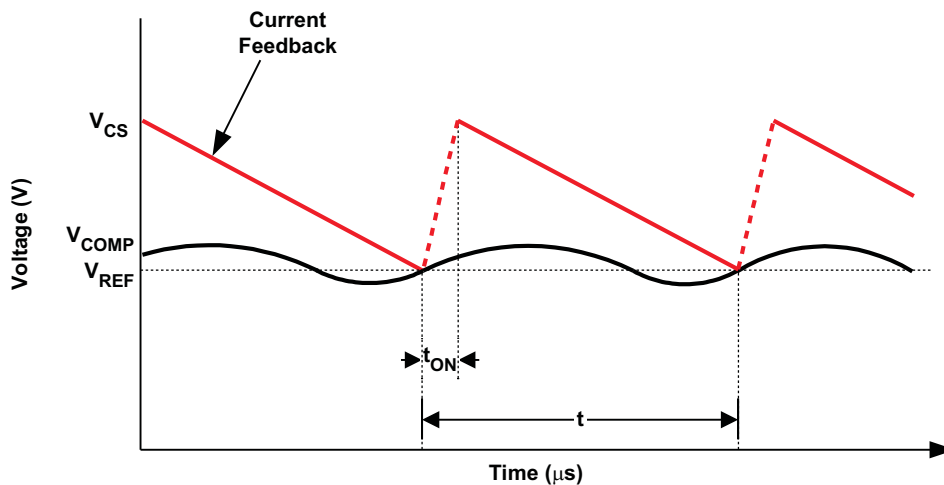
The TPS51317 is a D-CAP+™ mode adaptive on-time converter. Integrated high-side and low-side FET supports output current to a maximum of 6-ADC. The converter automatically runs in discontinuous conduction mode (DCM) to optimize light-load efficiency. Multiple switching frequencies are provided to enable optimization of the power chain for the cost, size and efficiency requirements of the design (see [Table 4](#)).

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS51317, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the reference voltage and the feedback voltage.

PWM Operation

Referring to [Figure 3](#), in steady state, continuous conduction mode, the converter operates in the following way.

Starting with the condition that the top FET is off and the bottom FET is on, the current feedback (V_{CS}) is higher than the error amplifier output (V_{COMP}). V_{CS} falls until it hits V_{COMP} , which contains a component of the output ripple voltage. V_{CS} is not directly accessible by measuring signals on pins of TPS51317. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.



UDG-10187

Figure 3. D-CAP+™ Mode Basic Waveforms

The current feedback is an amplified and filtered version of the voltage between PGND and SW during low-side FET on-time. The TPS51317 also provides a single-ended differential voltage (V_{OUT}) feedback to increase the system accuracy and reduce the dependence of circuit performance on layout.

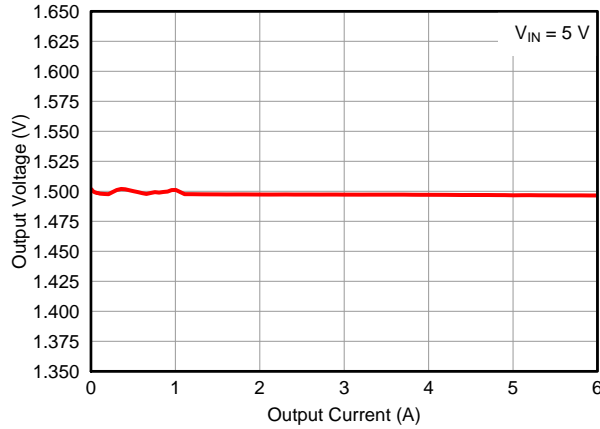


Figure 5. 1.5-V Load Regulation ($V_{IN} = 5\text{ V}$) Non-Droop Configuration

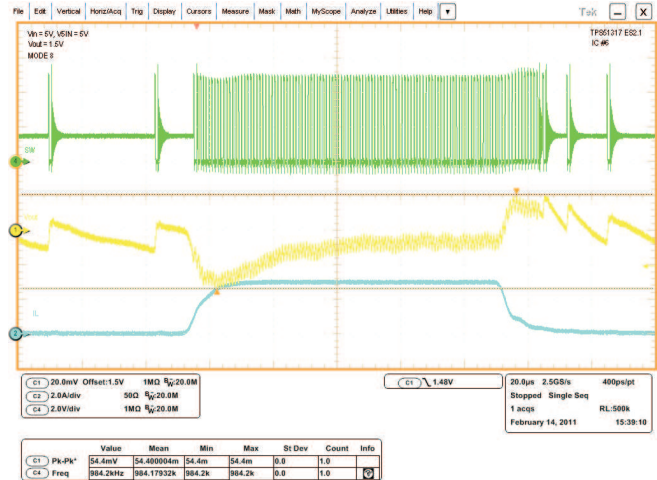


Figure 6. Non-Droop Configuration Transient Response

Droop Configuration

The terminology for droop is the same as *load line* or *voltage positioning* as defined in the Intel CPU V_{CORE} specification. Based on the actual tolerance requirement of the application, load-line set points can be defined to maximize either cost savings (by reducing output capacitors) or power reduction benefits.

Accurate droop voltage response is provided by the finite gain of the droop amplifier. The equation for droop voltage is shown in Equation 2.

$$V_{DROOP} = \frac{A_{CSINT} \times I(L)}{R_{DROOP} \times G_M}$$

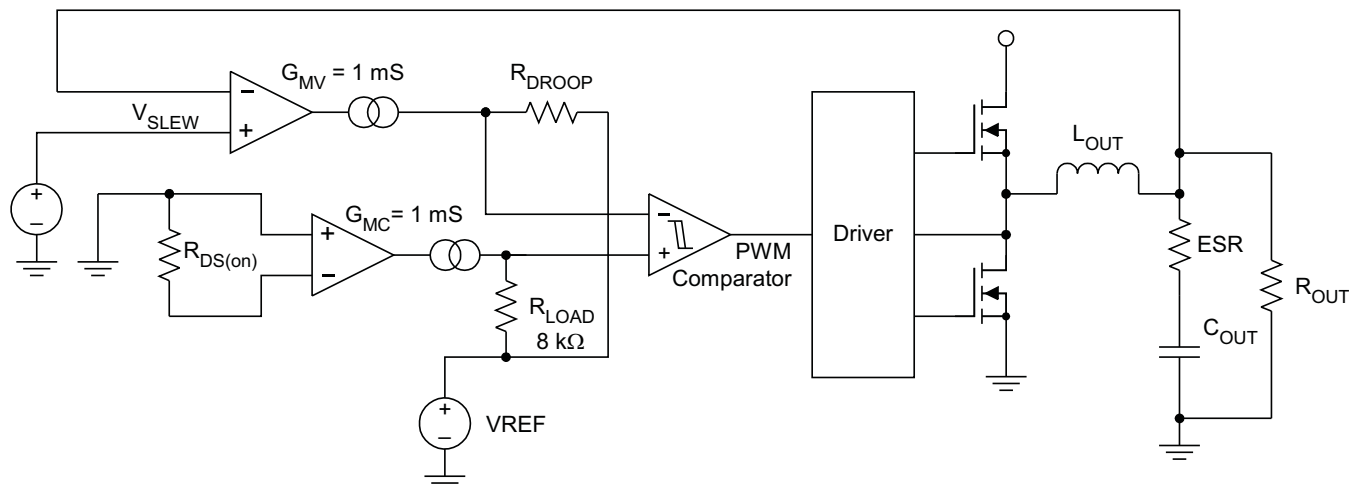
where

- low-side on-resistance is used as the current sensing element
- A_{CSINT} is a constant, which nominally is 53 mV/A.
- $I(L)$ is the DC current of the inductor, or the load current
- R_{DROOP} is the value of resistor from the COMP pin to the VREF pin
- G_M is the transconductance of the droop amplifier with nominal value of 1 mS

Equation 3 can be used to easily derive R_{DROOP} for any load line slope/droop design target.

$$R_{LOAD_LINE} = \frac{V_{DROOP}}{I(L)} = \frac{A_{CSINT}}{R_{DROOP} \times G_M} \therefore R_{DROOP} = \frac{A_{CSINT}}{R_{LOAD_LINE} \times G_M}$$

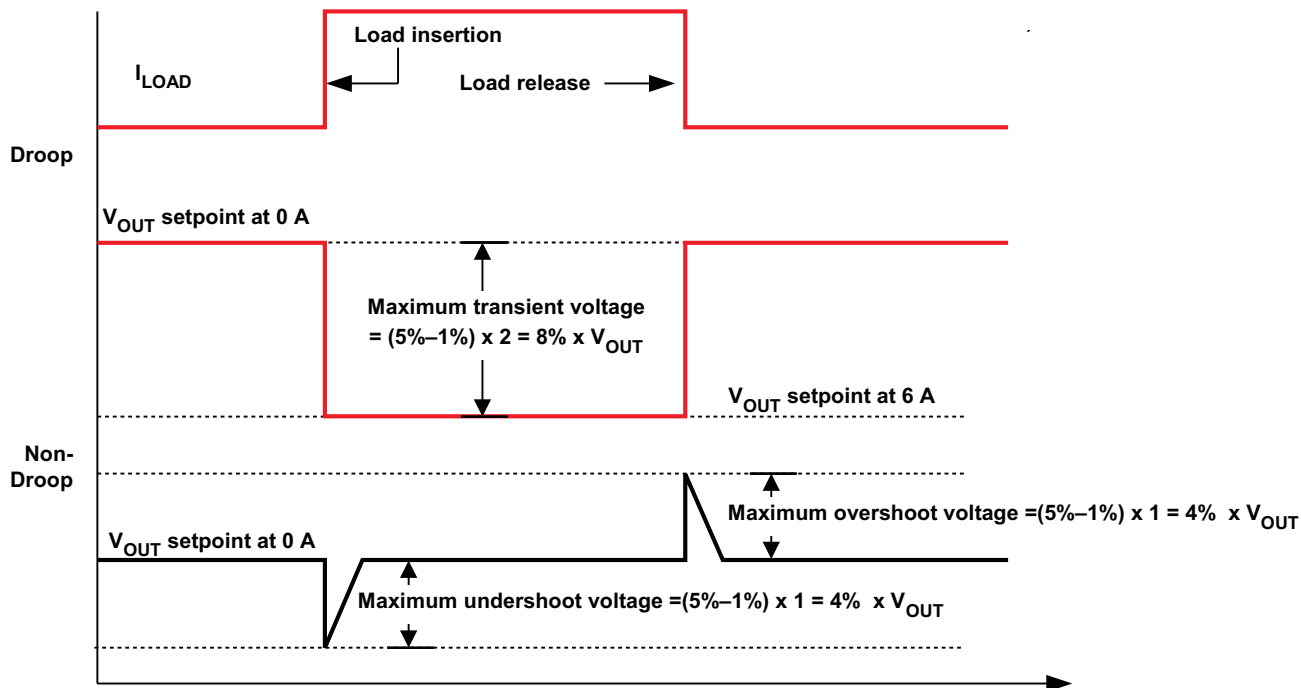
Figure 7 shows the basic implementation of the droop mode using the TPS51317.



UDG-10188

Figure 7. DROOP Mode Basic Implementation

The droop (voltage positioning) method was originally recommended to reduce the number of external output capacitors required. The effective transient voltage range is increased because of the active voltage positioning (see Figure 8).



UDG-11080

Figure 8. DROOP vs Non-DROOP in Transient Voltage Window

In applications where the DC and the AC tolerances are not separated, which means there is not a strict DC tolerance requirement, the droop method can be used.

Table 4. Mode Definitions

| MODE | MODE RESISTANCE (kΩ) | LIGHT-LOAD POWER SAVING MODE | SWITCHING FREQUENCY (f _{sw}) (MHz) |
|------|----------------------|------------------------------|--|
| 1 | 0 | SKIP | 0.86 |
| 2 | 12 | SKIP | 1.2 |
| 3 | 22 | SKIP | 1.5 |
| 4 | 33 | RR ⁽¹⁾ | 1.0 |
| 5 | 47 | RR ⁽¹⁾ | 0.86 |
| 6 | 68 | PWM | 1.2 |
| 7 | 100 | PWM | 1.5 |
| 8 | OPEN | SKIP | 1.0 |

(1) Ripple reduction is a special light-load power saving feature. See [\(Light-Load Power Saving Features\)](#)

Figure 9 shows the load regulation of the 1.5-V rail using an R_{DRROP} value of 5 kΩ.

Figure 10 shows the transient response of the TPS51317 using droop configuration and C_{OUT} = 6 × 22 μF. The applied step load is from 0 A to 3 A.

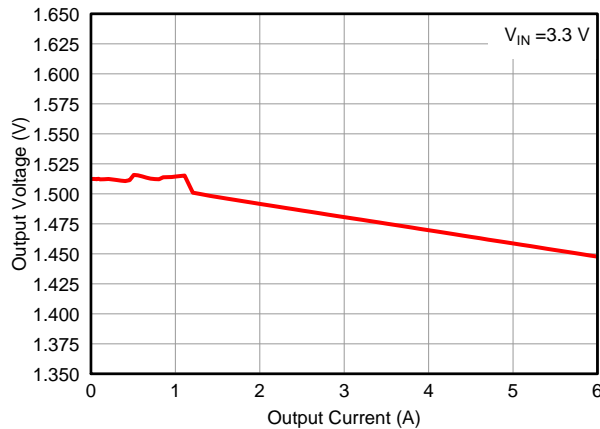


Figure 9. 1.5-V Load Regulation (V_{IN} = 5 V)

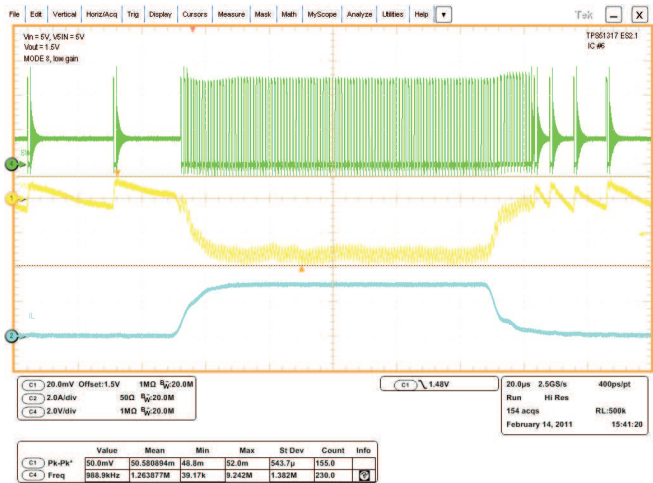


Figure 10. Droop Configuration Transient Response, C_{OUT} = 6 x 22 μF and 0 A to 3 A

Light-Load Power Saving Features

The TPS51317 has an automatic pulse-skipping mode to provide excellent efficiency over a wide load range. The converter senses inductor current and prevents negative flow by shutting off the low-side gate driver. This saves power by eliminating re-circulation of the inductor current. Further, when the bottom FET shuts off, the converter enters discontinuous mode, and the switching frequency decreases, thus reducing switching losses as well.

TPS51317 also provides a special light-load power saving feature, called ripple reduction. Essentially, it reduces the on-time in SKIP mode to effectively reduce the output voltage ripple associated with using an all MLCC capacitor output power stage design.

Power Sequences

Non-Tracking Startup

The TPS51317 can be configured for non-tracking application. When non-tracking is configured, output voltage is regulated to the REFIN voltage which taps off the voltage dividers from the 2VREF. Either the EN pin or the V5IN pin can be used to start up the device. The TPS51317 uses internal voltage servo DAC to provide a precise 1.6-ms soft-start time during soft-start initialization. (See [Figure 11](#))

Tracking Startup

TPS51317 can also be configured for tracking application. When tracking configuration is desired, output voltage is also regulated to the REFIN voltage which comes from external power source. In order for TPS51317 to differentiate between a non-tracking configuration or a tracking configuration, there is a minimum delay time of 260 μ s required between the time when the EN pin or the V5IN pin is validated to the time when the REFIN pin voltage can be applied, in order for the TPS51317 to track properly (see [Figure 12](#)). The valid REFIN voltage range is between 0.6 V to 2 V.

Protection Features

The TPS51317 offers many features to protect the converter power chain as well as the system electronics.

5-V Undervoltage Protection (UVLO)

The TPS51317 continuously monitors the voltage on the V5IN pin to ensure that the voltage level is high enough to bias the device properly and to provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.3 V and has a nominal of 440 mV of hysteresis. If the 5-V UVLO limit is reached, the converter transitions the phase node into a off function. And the converter remains in the off state until the device is reset by cycling 5 V until the 5-V POR is reached (2.3-V nominal). The power input does not have an UVLO function

Power Good Signals

The TPS51317 has one open-drain *power good* (PGOOD) pin. During startup, there is a 1-ms power good high propagation delay. The PGOOD pin de-asserts as soon as the EN pin is pulled low or an undervoltage condition on V5IN or any other faults that require latch off action is detected.

Output Overvoltage Protection (OVP)

In addition to the power good function described above, the TPS51317 has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when the output voltage is approximately $120\% \times V_{REFIN}$. In this case, the converter de-asserts the PGOOD signals and performs the overvoltage protection function. The converter remains in this state until the device is reset by cycling 5 V until the 5-V POR threshold (2.3 V nominal) is reached.

Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the [Overcurrent Protection](#) and [Overcurrent Limit](#) sections. If the output voltage drops below 70% of V_{REFIN} , after an 8- μ s delay, the device latches OFF. Undervoltage protection can be reset only by EN or a 5-V POR.

Overcurrent Protection

Both positive and negative overcurrent protection are provided in the TPS51317:

- Overcurrent Limit (OCL)
- Negative OCL (level same as positive OCL)

Overcurrent Limit

If the sensed current value is above the OCL setting, the converter delays the next ON pulse until the current drops below the OCL limit. Current limiting occurs on a pulse-by-pulse basis. The TPS51317 uses a valley current limiting scheme where the DC OCL trip point is the OCL limit plus half of the inductor ripple current. The minimum valley OCL is 6 A over process and temperature.

During the overcurrent protection event, the output voltage likely droops until the UVP limit is reached. Then, the converter de-asserts the PGOOD pin, and then latches OFF after an 8- μ s delay. The converter remains in this state until the device is reset.

$$I_{\text{OCL(dc)}} = I_{\text{OCL(valley)}} + \frac{1}{2} \times I_{\text{P-P}} \quad (4)$$

Negative OCL

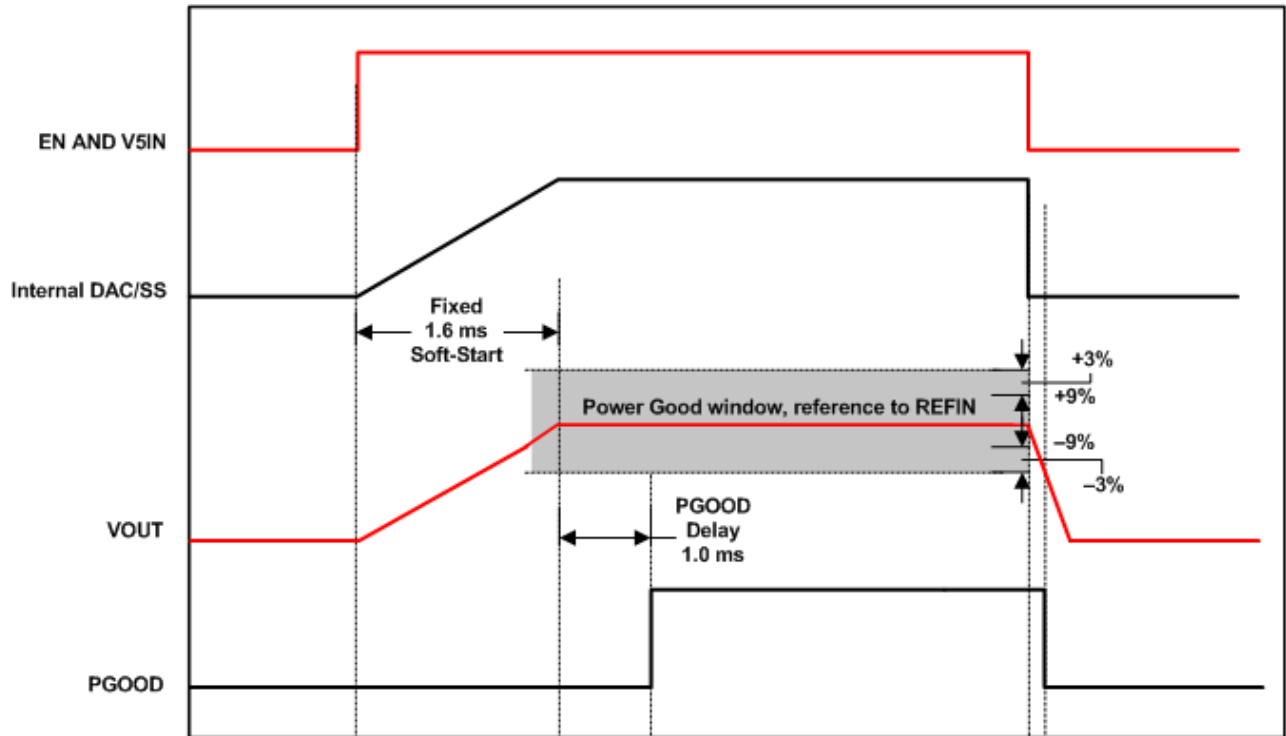
The negative OCL circuit acts when the converter is sinking current from the output capacitor(s). The converter continues to act in a *valley* mode, the absolute value of the negative OCL set point is typically -6.5 A.

Thermal Protection

Thermal Shutdown

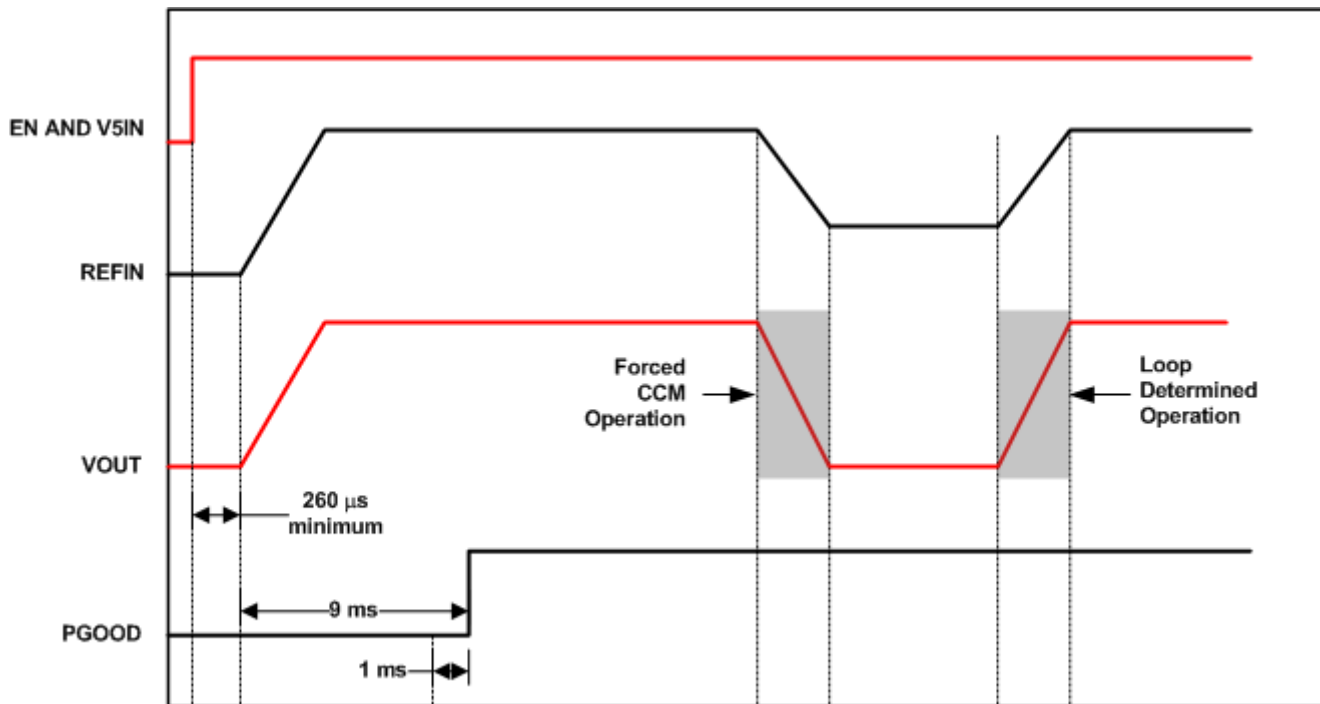
The TPS51317 has an internal temperature sensor. When the temperature reaches a nominal 145°C, the device shuts down until the temperature cools by approximately 10°C. Then the converter restarts.

Startup Timing Diagrams



UDG-11061

Figure 11. Non-Tracking Start-Up



UDG-11079

Figure 12. Tracking Start-Up

TYPICAL CHARACTERISTICS

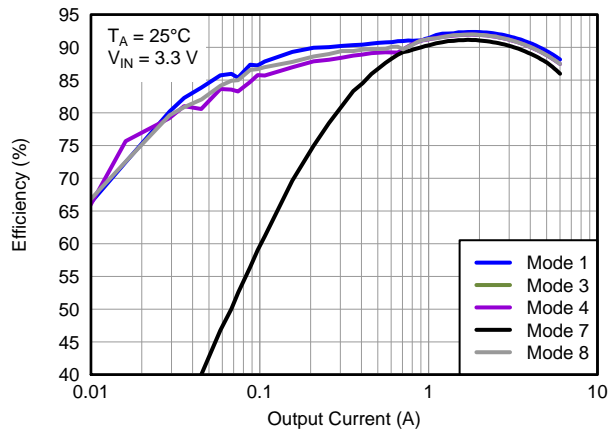


Figure 13. Efficiency vs Output Current

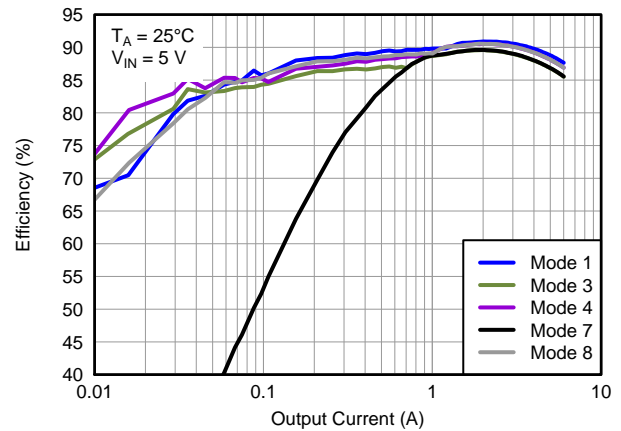


Figure 14. Efficiency vs Output Current

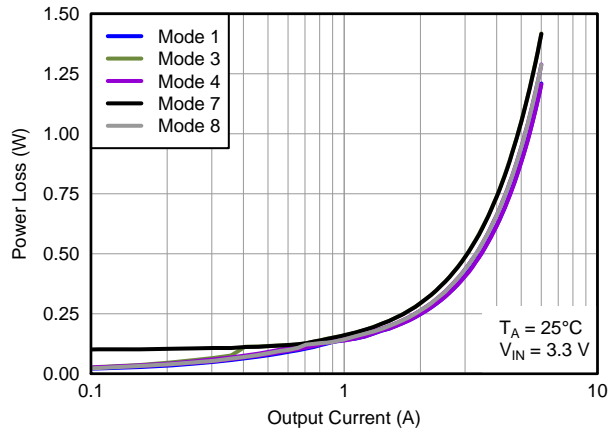


Figure 15. Power Loss

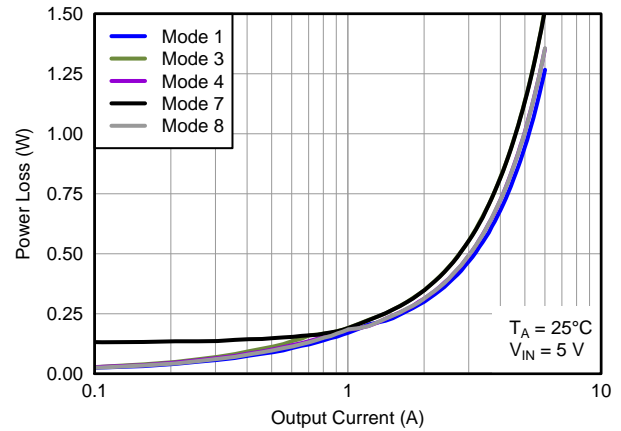


Figure 16. Power Loss

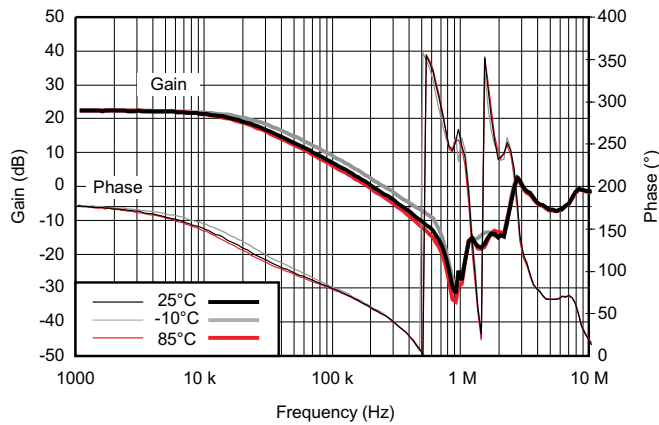


Figure 17. Bode Plot (Non-Droop Mode) $V_{IN} = 5 V$, $V_{OUT} = 0.8 V$, $I_{LOAD} = 5 A$

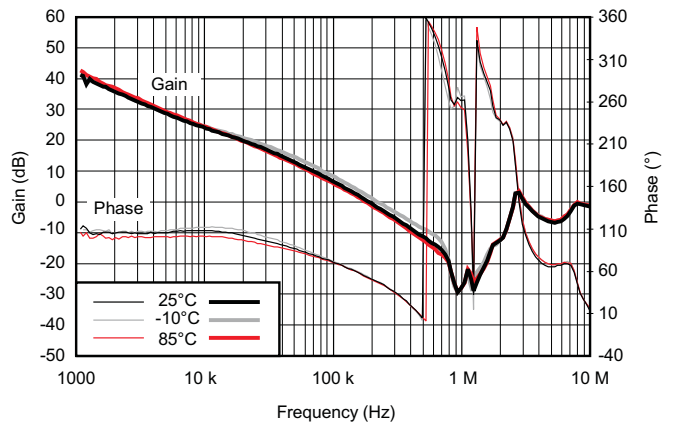


Figure 18. Bode Plot (Droop Mode), $V_{IN} = 5 V$, $V_{OUT} = 0.8 V$, $I_{LOAD} = 5 A$

DESIGN PROCEDURE

The simplified design procedure is done for a non-droop application using the TPS51317 converter.

Step One

Determine the specifications.

The Rail requirements provide the following key parameters:

1. $V_{OUT} = 1.5\text{ V}$
2. $I_{CC(max)} = 6\text{ A}$
3. $I_{DYN(max)} = 3\text{ A}$
4. $I_{CC(tdc)} = 3\text{ A}$

Step Two

Determine system parameters.

The input voltage range and operating frequency are of primary interest. For example:

1. $V_{IN} = 5\text{ V}$
2. $f_{SW} = 1\text{ MHz}$

Step Three

Determine inductor value and choose inductor.

Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. In this case, use 40%:

$$I_{P-P} = 6\text{ A} \times 0.4 = 2.4\text{ A} \quad (5)$$

At $f_{SW} = 1\text{ MHz}$, with a 5-V input and a 1.5-V output:

$$L = \frac{V \times dT}{I_{P-P}} = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{(f_{SW} \times V_{IN})} \right)}{I_{P-P}} = \frac{(5 - 1.5) \times \left(\frac{1.5}{(1 \times 5)} \right)}{1.5\text{ A}} = 0.43\text{ }\mu\text{H} \quad (6)$$

For this application, a 0.42- μH , 1.55-m Ω inductor from NEC-TOKIN with part number MPCG0740LR42C is chosen.

Step Four

Set the output voltage.

$$V_{OUT} = \frac{V_{VREF}}{R_{UPPER} + R_{LOWER}} \times R_{LOWER} \quad (7)$$

The output voltage is determined by the 2-V reference (V_{REF}) and the resistor dividers (R_{UPPER} and R_{LOWER}). The output voltage is regulated to the REF_{IN} pin. Because the 2-V reference current capability is limited to less than 50 μA , care should be taken when selecting the resistor dividers. For the current reference design of 1.5 V (see application schematics shown in [Figure 1](#) and [Figure 2](#), $R_{UPPER} = 100\text{ k}\Omega$, $R_{LOWER} = 300\text{ k}\Omega$).

Step Five

Calculate OCL.

The DC OCL level of TPS51317 design is determined by [Equation 8](#),

$$I_{OCL(dc)} = I_{OCL(valley)} + \frac{1}{2} \times I_{P-P} = 6\text{ A} + \frac{1}{2} \times 1.5\text{ A} = 6.75\text{ A} \quad (8)$$

The minimum valley OCL is 6 A over process and temperature, and $I_{p,p} = 1.5$ A, the minimum DC OCL is calculated to be 6.75A.

Step Six

Determine the output capacitance.

To determine C_{OUT} based on transient and stability requirement, first calculate the the minimum output capacitance for a given transient.

Equation 10 and Equation 9 can be used to estimate the amount of capacitance needed for a given dynamic load step/release. Please note that there are other factors that may impact the amount of output capacitance for a specific design, such as ripple and stability. Equation 10 and Equation 9 are used only to estimate the transient requirement, the result should be used in conjunction with other factors of the design to determine the necessary output capacitance for the application.

$$C_{OUT(\min_under)} = \frac{L \times \Delta I_{LOAD(max)}^2 \times \left(\frac{V_{VOUT} \times t_{SW}}{V_{IN(min)}} + t_{MIN(off)} \right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{VOUT}}{V_{IN(min)}} \right) \times t_{SW} - t_{MIN(off)} \right) \times V_{VOUT}} \quad (9)$$

$$C_{OUT(\min_over)} = \frac{L_{OUT} \times (\Delta I_{LOAD(max)})^2}{2 \times \Delta V_{LOAD(release)} \times V_{VOUT}} \quad (10)$$

Equation 9 and Equation 10 calculate the minimum C_{OUT} for meeting the transient requirement, which is 84 μ F assuming the following:

- $\pm 3\%$ voltage allowance for load step and release
- MLCC capacitance derating of 60% due to DC and AC bias effect

In this reference design, 6, 22- μ F capacitors are used in order to provide this amount of capacitance.

Step Seven

Determine the stability based on the output capacitance C_{OUT} .

In order to achieve stable operation. The 0-dB frequency, f_0 should be kept less than 1/5 of the switching frequency (1 MHz). (See Figure 4)

$$f_0 = \frac{1}{2\pi} \times \frac{G_M}{C_{OUT}} \times \frac{R_C}{R_S} = 190 \text{ kHz}$$

where

$$\bullet \quad R_S = R_{DS(on)} \times G_{MC} \times R_{LOAD} \quad (11)$$

$$R_C = \frac{f_0 \times R_S \times 2\pi \times C_{OUT}}{G_M} = \frac{190 \text{ kHz} \times 53 \text{ m}\Omega \times 2\pi \times 80 \mu\text{F}}{1 \text{ mS}} \approx 5 \text{ k}\Omega \quad (12)$$

Using 6, 22- μ F capacitors, the compensation resistance, R_C can be calculated to be approximately 5 k Ω .

The purpose of the comparator capacitor (C_C) is to reduce the DC component to obtain high DC feedback gain. However, as it causes phase delay, another zero to cancel this effect at f_0 is needed. This zero can be determined by values of C_C and the compensation resistor, R_C .

$$f_z = \frac{1}{2\pi \times R_C \times C_C} = \frac{f_0}{10} \quad (13)$$

And since R_C has previously been derived, the value of C_C is calculated to be 2.2 nF. In order to further boost phase margin, a value of 3.3-nF is chosen for this reference design.

Step Eight

Select decoupling and peripheral components.

For TPS51317 peripheral capacitors use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

- V5IN decoupling $\geq 22 \mu\text{F}$, $\geq 10 \text{ V}$
- VREF decoupling $0.22 \mu\text{F}$ to $1 \mu\text{F}$, $\geq 4 \text{ V}$
- Bootstrap capacitors $\geq 0.1 \mu\text{F}$, $\geq 10 \text{ V}$
- Pull-up resistors on PGOOD, $100 \text{ k}\Omega$

Layout Considerations

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout.

- Connect PGND pins (or at least one of the pins) to the thermal PAD underneath the device. Also connect GND pin to the thermal PAD underneath the device. Use four vias to connect the thermal pad to internal ground planes.
- Place VIN, V5IN and 2VREF decoupling capacitors as close to the device as possible.
- Use wide traces for the VIN, VOUT, PGND and SW pins. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep COMP analog signal away from noisy signals (SW, BST).

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS51317RGBR | ACTIVE | VQFN | RGB | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 51317 | Samples |
| TPS51317RGBT | ACTIVE | VQFN | RGB | 20 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 51317 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS51317RGBR | VQFN | RGB | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| TPS51317RGBR | VQFN | RGB | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| TPS51317RGBT | VQFN | RGB | 20 | 250 | 180.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| TPS51317RGBT | VQFN | RGB | 20 | 250 | 180.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

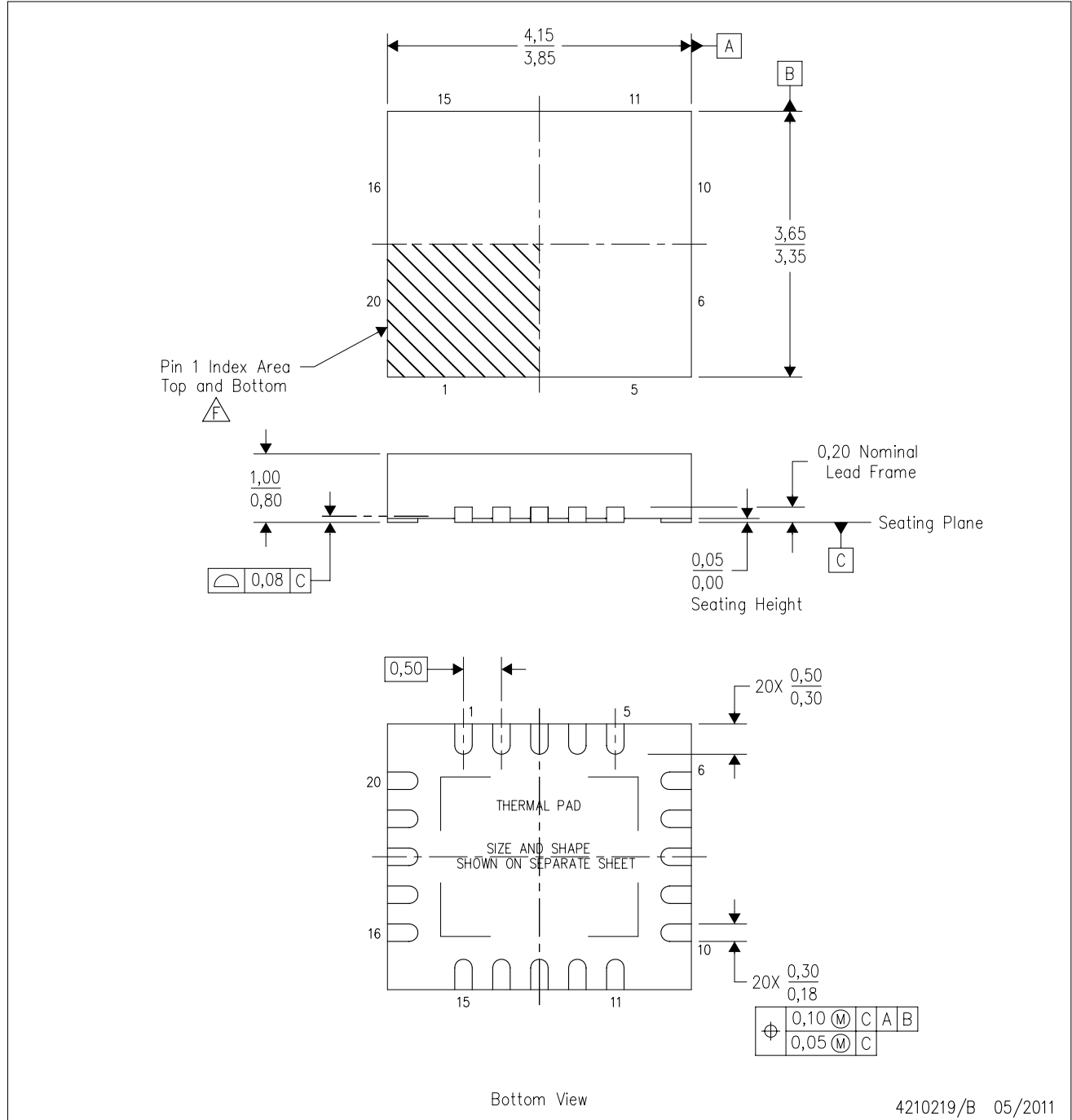
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS51317RGBR | VQFN | RGB | 20 | 3000 | 356.0 | 356.0 | 35.0 |
| TPS51317RGBR | VQFN | RGB | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS51317RGBT | VQFN | RGB | 20 | 250 | 210.0 | 185.0 | 35.0 |
| TPS51317RGBT | VQFN | RGB | 20 | 250 | 210.0 | 185.0 | 35.0 |

RGB (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

THERMAL PAD MECHANICAL DATA

RGB (R-PVQFN-N20)

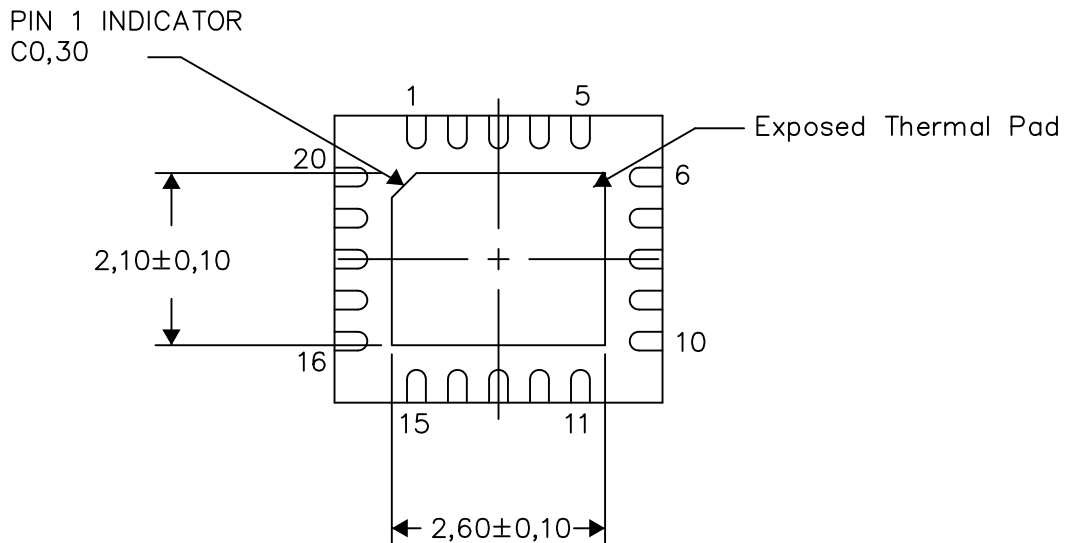
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

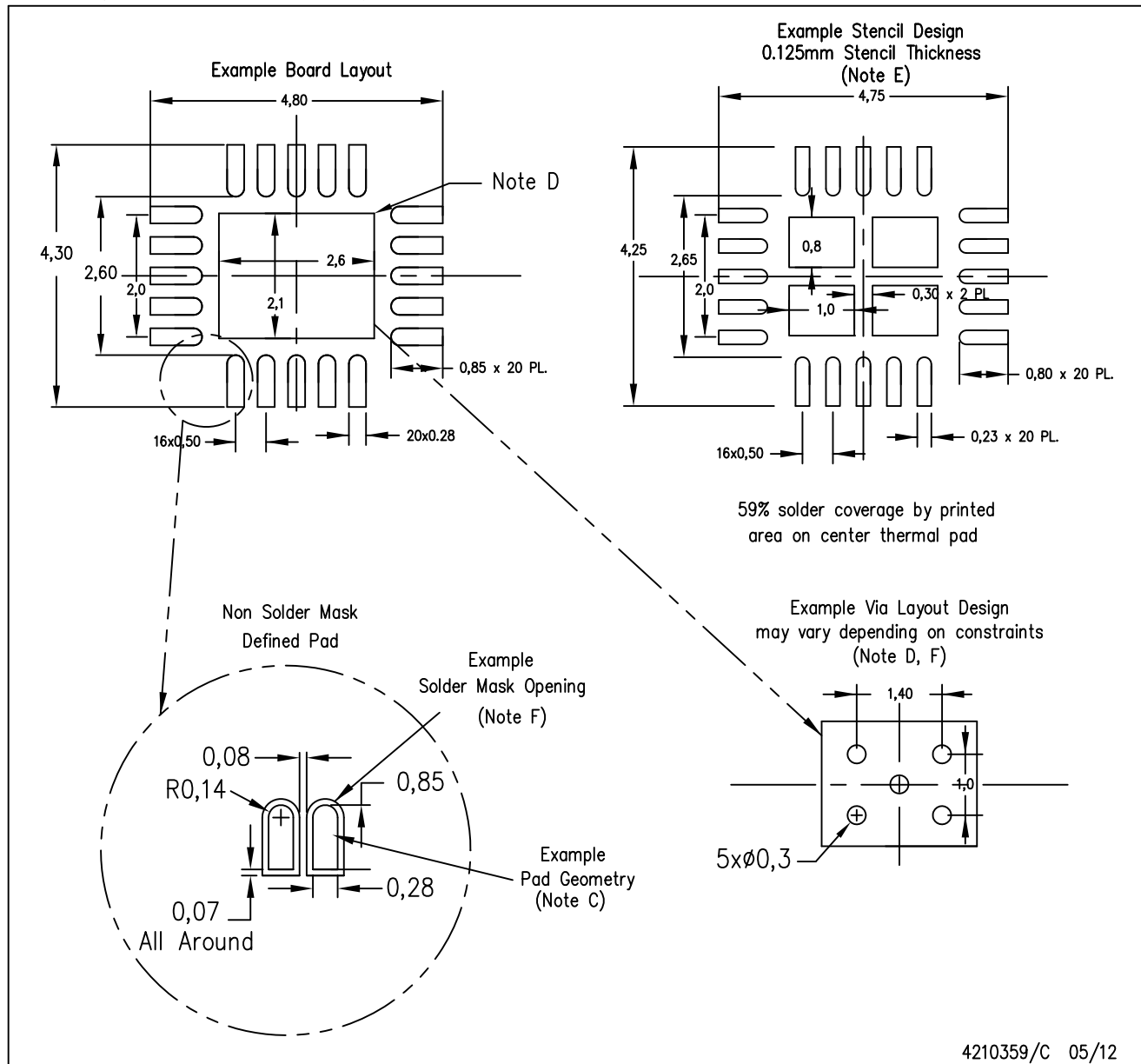
Exposed Thermal Pad Dimensions

4210242/C 05/12

NOTE: All linear dimensions are in millimeters

RGB (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated