LMR62421 SIMPLE SWITCHER® 24Vout, 2.1A Step-Up Voltage Regulator in SOT-23

Check for Samples: LMR62421

FEATURES

- **Input Voltage Range of 2.7V to 5.5V**
- **Output Voltage up to 24V**
- **Switch Current up to 2.1A**
- **1.6 MHz Switching Frequency**
- **Low Shutdown Iq, 80 nA**
- **Cycle-by-Cycle Current Limiting**
- **Internally Compensated**
- **Internal Soft-Start**
- **5-Pin SOT-23 (2.92 x 2.84 x 1mm) and 6-Pin WSON (3 x 3 x 0.8 mm) Packaging**
- **Fully Enabled for WEBENCH® Power Designer**

PERFORMANCE BENEFITS

- **Extremely Easy to Use**
- **Tiny Overall Solution Reduces System Cost**

APPLICATIONS

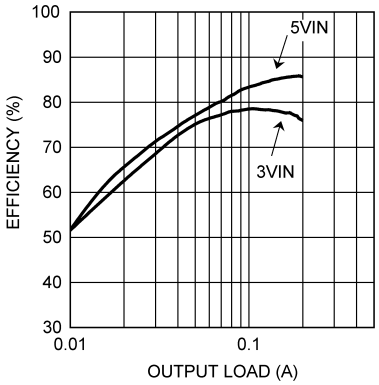
- **Boost / SEPIC Conversions from 3.3V, 5V Rails**
- **Space Constrained Applications**
- **Embedded Systems**
- **LCD Displays**
- **LED Applications**

DESCRIPTION

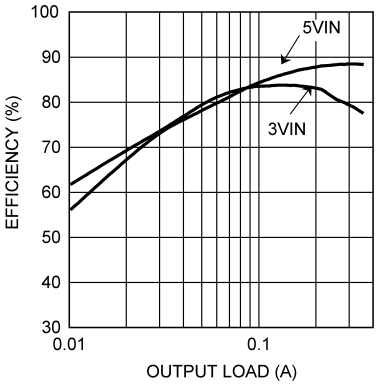
The LMR62421 is an easy-to-use, space-efficient 2.1A low-side switch regulator ideal for Boost and SEPIC DC-DC regulation. It provides all the active functions to provide local DC/DC conversion with fast-transient response and accurate regulation in the smallest PCB area. Switching frequency is internally set to 1.6 MHz, allowing the use of extremely small surface mount inductor and chip capacitors while providing efficiencies near 90%. Current-mode control and internal compensation provide ease-of-use, minimal component count, and high-performance regulation over a wide range of operating conditions. External shutdown features an ultra-low standby current of 80 nA ideal for portable applications. Tiny 5-pin SOT-23 and 6-pin WSON packages provide space-savings. Additional features include internal soft-start, circuitry to reduce inrush current, pulse-by-pulse current limit, and thermal shutdown.

System Performance

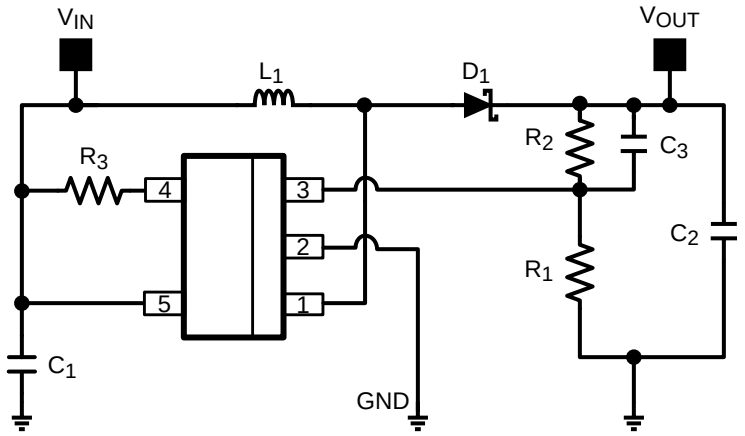
Efficiency vs Load Current
V_{OUT} = 20V



Efficiency vs Load Current
V_{OUT} = 12V



Typical Application



Connection Diagrams

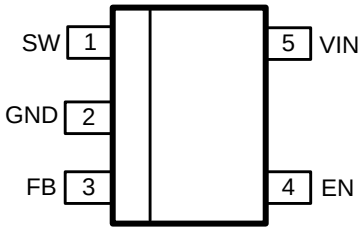


Figure 1. 5-Pin SOT-23 (Top View)
See DBV Package

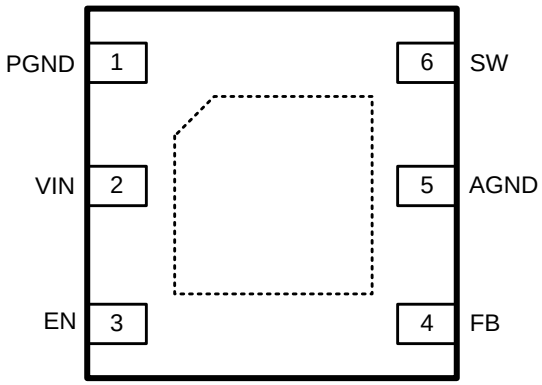


Figure 2. 6-Pin WSON (Top View)
See NGG0006A Package

PIN DESCRIPTIONS - 5-Pin SOT-23

Pin	Name	Function
1	SW	Switch node. Connect to the inductor, output diode.
2	GND	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
3	FB	Feedback pin. Connect FB to external resistor divider to set output voltage.
4	EN	Shutdown control input. Logic high enables operation. Do not allow this pin to float or be greater than VIN + 0.3V.
5	VIN	Supply voltage for power stage, and input supply voltage.

PIN DESCRIPTIONS - 6-Pin WSON

Pin	Name	Function
1	PGND	Power ground pin. Place PGND and output capacitor GND close together.
2	VIN	Supply voltage for power stage, and input supply voltage.
3	EN	Shutdown control input. Logic high enables operation. Do not allow this pin to float or be greater than VIN + 0.3V.
4	FB	Feedback pin. Connect FB to external resistor divider to set output voltage.
5	AGND	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to this pin & pin 4.
6	SW	Switch node. Connect to the inductor, output diode.
DAP	GND	Signal & Power ground. Connect to pin 1 & pin 5 on top layer. Place 4-6 vias from DAP to bottom layer GND plane.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{IN}	-0.5V to 7V
SW Voltage	-0.5V to 26.5V
FB Voltage	-0.5V to 3.0V
EN Voltage	-0.5V to VIN + 0.3V
ESD Susceptibility(3)	2kV
Junction Temperature(4)	150°C
Storage Temp. Range	-65°C to 150°C
For soldering specifications: SNOA549	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specified specifications and the test conditions, see Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
(4) Thermal shutdown will occur if the junction temperature exceeds the maximum junction temperature of the device.

Operating Ratings(1)

V_{IN}	2.7V to 5.5V
V_{EN}(2)	0V to V_{IN}
Junction Temperature Range	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specified specifications and the test conditions, see Electrical Characteristics.
(2) Do not allow this pin to float or be greater than V_{IN} +0.3V.

Electrical Characteristics[1][2]

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature range of (T_J = -40°C to 125°C). Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 5V unless otherwise indicated under the Conditions column.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	−40°C ≤ to T_J ≤ +125°C (SOT-23)	**1.230**	1.255	**1.280**	V
		0°C ≤ to T_J ≤ +125°C (SOT-23)	**1.236**	1.255	**1.274**	
		−40°C ≤ to T_J ≤ +125°C (WSON)	**1.225**	1.255	**1.285**	
		−0°C ≤ to T_J ≤ +125°C (WSON)	**1.229**	1.255	**1.281**	
$\Delta V_{FB}/V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 2.7V to 5.5V		0.06		%/V
I_{FB}	Feedback Input Bias Current			0.1	**1**	µA
F_{SW}	Switching Frequency		**1200**	1600	**2000**	kHz
D_{MAX}	Maximum Duty Cycle		**88**	96		%
D_{MIN}	Minimum Duty Cycle			5		%
$R_{DS(ON)}$	Switch On Resistance	SOT-23		170	**330**	mΩ
		WSON		190	**350**	
I_{CL}	Switch Current Limit		**2.1**	3		A
SS	Soft Start			4		ms
I_Q	Quiescent Current (switching)			7.0	**11**	mA
	Quiescent Current (shutdown)	V_{EN} = 0V		80		nA
UVLO	Undervoltage Lockout	VIN Rising		2.3	**2.65**	V
		VIN Falling	**1.7**	1.9		
V_{EN_TH}	Shutdown Threshold Voltage	See [3]			**0.4**	V
	Enable Threshold Voltage	See [3]	**1.8**			
I_{-SW}	Switch Leakage	V_{SW} = 24V		1.0		µA
I_{-EN}	Enable Pin Current	Sink/Source		100		nA
θ_{JA}	Junction to Ambient 0 LFPM Air Flow[4]	WSON		80		°C/W
		SOT-23		118		
θ_{JC}	Junction to Case	WSON		18		°C/W
		SOT-23		60		
T_{SD}	Thermal Shutdown Temperature[5]			160		°C
	Thermal Shutdown Hysteresis			10		

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Do not allow this pin to float or be greater than V_{IN} +0.3V.
(4) Applies for packages soldered directly onto a 3" x 3" PC board with 2oz. copper on 4 layers in still air.
(5) Thermal shutdown will occur if the junction temperature exceeds the maximum junction temperature of the device.

Typical Performance Characteristics

Current Limit vs Temperature

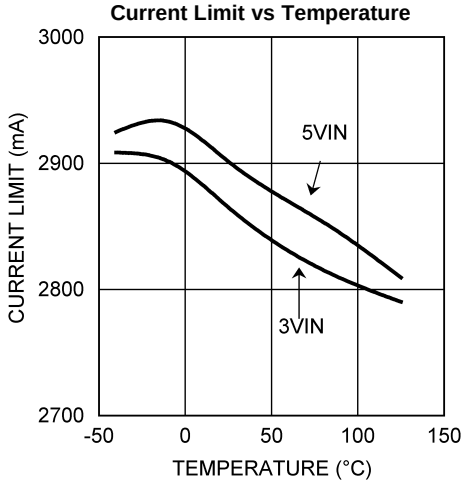


Figure 3.

FB Pin Voltage vs Temperature

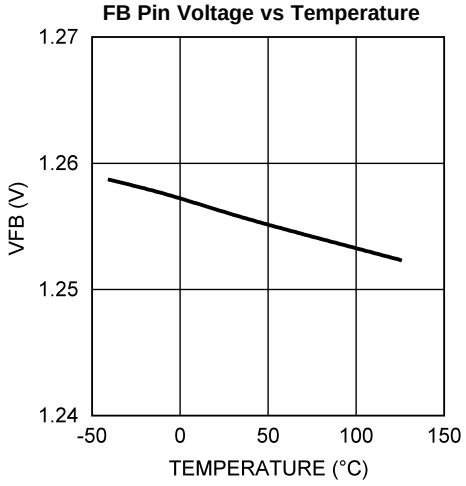


Figure 4.

Oscillator Frequency vs Temperature

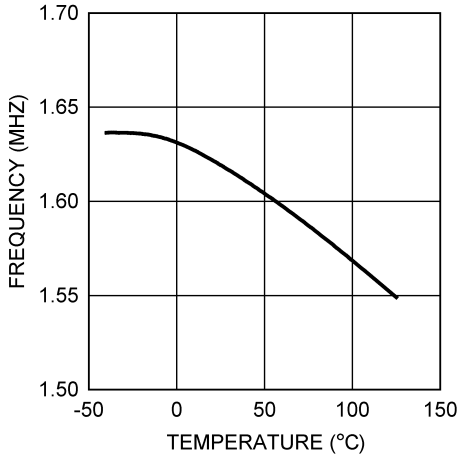


Figure 5.

Typical Maximum Output Current vs V_{IN}

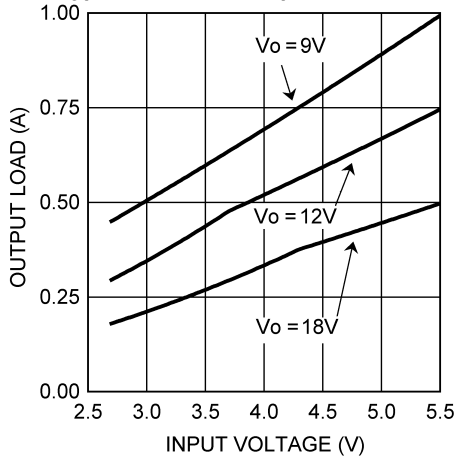


Figure 6.

R_{DSON} vs Temperature

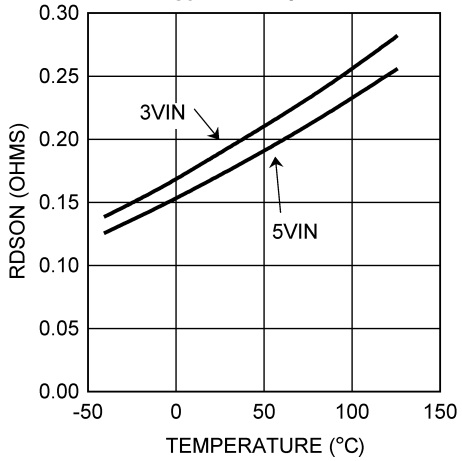


Figure 7.

Efficiency vs Load Current, Vo = 20V

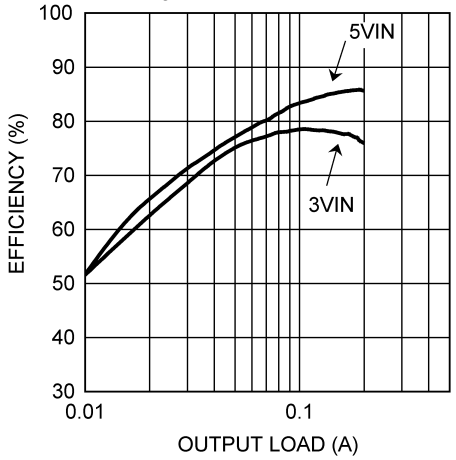


Figure 8.

Typical Performance Characteristics (continued)

Efficiency vs Load Current, Vo = 12V

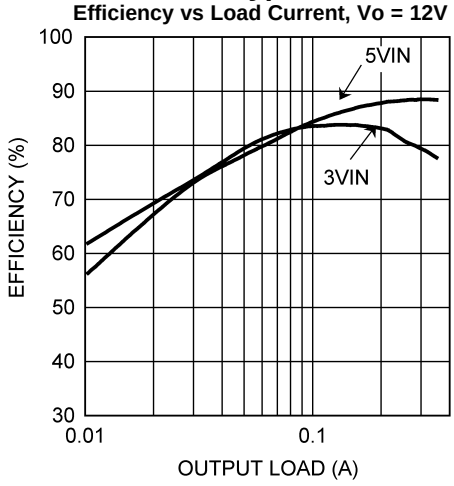


Figure 9.

Output Voltage Load Regulation

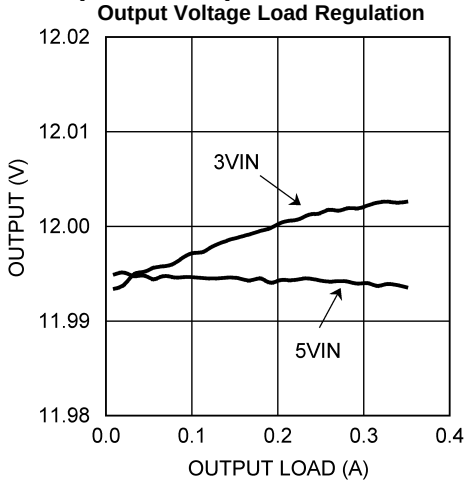


Figure 10.

Output Voltage Line Regulation

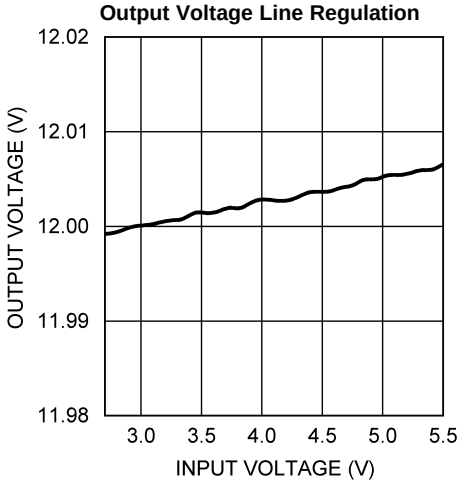


Figure 11.

Simplified Internal Block Diagram

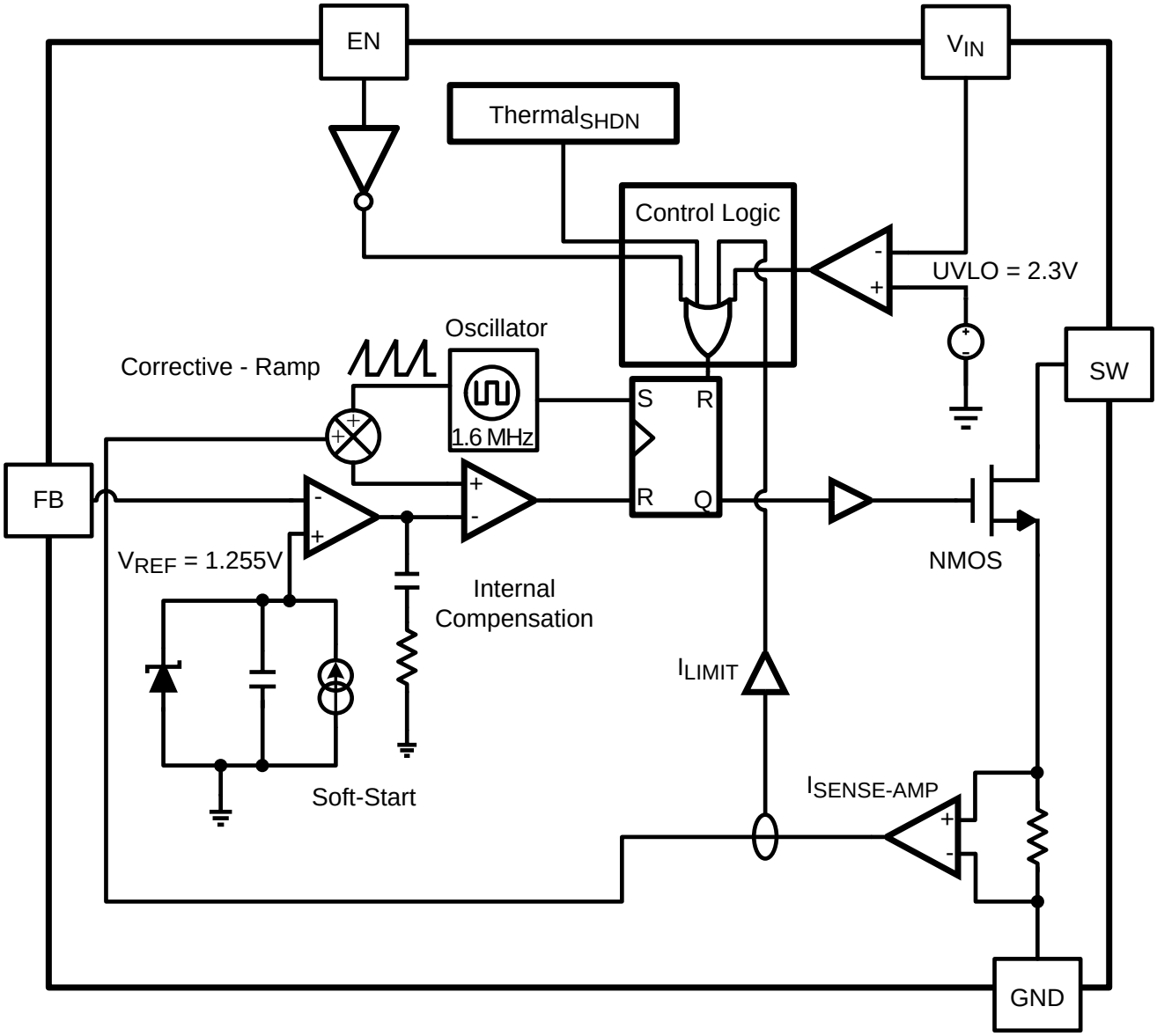


Figure 12. Simplified Block Diagram

APPLICATION INFORMATION

THEORY OF OPERATION

The following operating description of the LMR62421 will refer to the Simplified Block Diagram (Figure 12) the simplified schematic (Figure 13), and its associated waveforms (Figure 14). The LMR62421 supplies a regulated output voltage by switching the internal NMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this on-time, the SW pin voltage (V_{SW}) decreases to approximately GND, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sensed signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through diode D1, which forces the SW pin to swing to the output voltage plus the forward voltage (V_D) of the diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage .

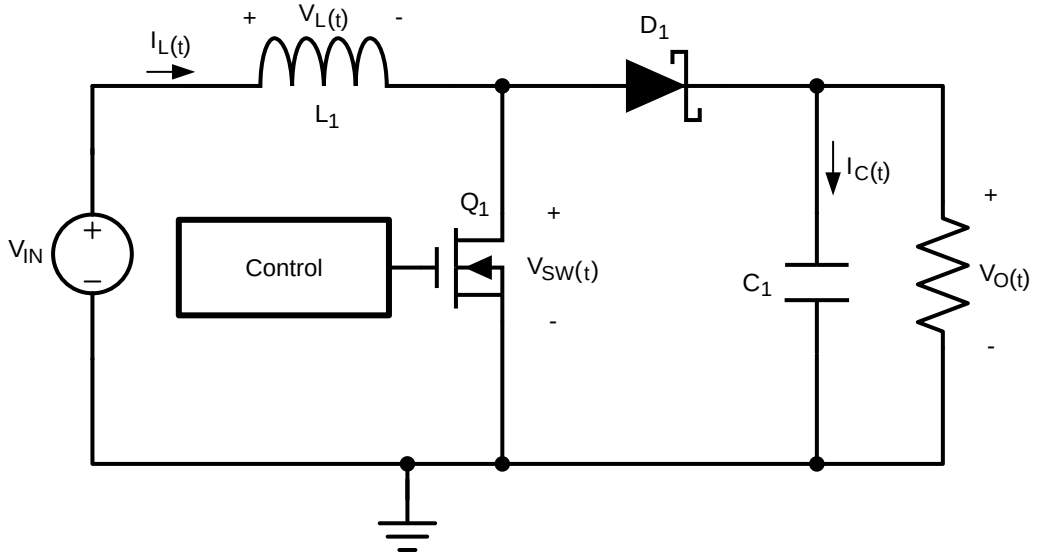


Figure 13. Simplified Schematic

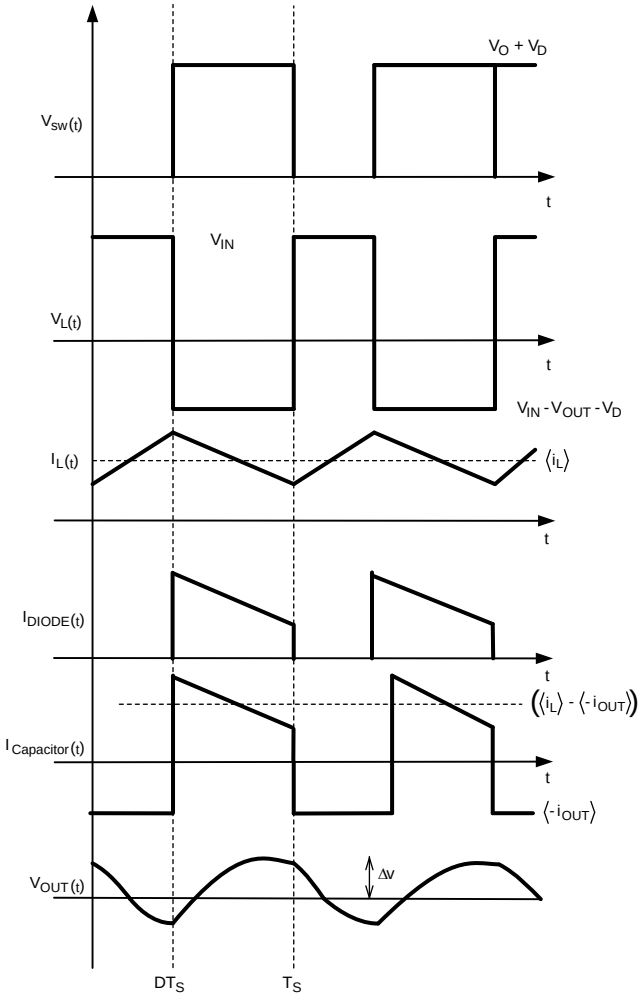


Figure 14. Typical Waveforms

CURRENT LIMIT

The LMR62421 uses cycle-by-cycle current limiting to protect the internal NMOS switch. It is important to note that this current limit will not protect the output from excessive current during an output short circuit. The input supply is connected to the output by the series connection of an inductor and a diode. If a short circuit is placed on the output, excessive current can damage both the inductor and diode.

Design Guide

ENABLE PIN / SHUTDOWN MODE

The LMR62421 has a shutdown mode that is controlled by the Enable pin (EN). When a logic low voltage is applied to EN, the part is in shutdown mode and its quiescent current drops to typically 80 nA. Switch leakage adds up to another 1 µA from the input supply. The voltage at this pin should never exceed V_{IN} + 0.3V.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 160°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

SOFT-START

This function forces V_{OUT} to increase at a controlled rate during start up. During soft-start, the error amplifier's reference voltage ramps to its nominal value of 1.255V in approximately 4.0ms. This forces the regulator output to ramp up in a more linear and controlled fashion, which helps reduce inrush current.

INDUCTOR SELECTION

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}):

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{1}{1-D}\right) = \frac{1}{D'} \tag{1}$$

Therefore:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{2}$$

Power losses due to the diode (D1) forward voltage drop, the voltage drop across the internal NMOS switch, the voltage drop across the inductor resistance (R_{DCR}) and switching losses must be included to calculate a more accurate duty cycle (See Calculating Efficiency and Junction Temperature for a detailed explanation). A more accurate formula for calculating the conversion ratio is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\eta}{D'} \tag{3}$$

where

- η equals the efficiency of the LMR62421 application.

The inductor value determines the input ripple current. Lower inductor values decrease the size of the inductor, but increase the input ripple current. An increase in the inductor value will decrease the input ripple current.

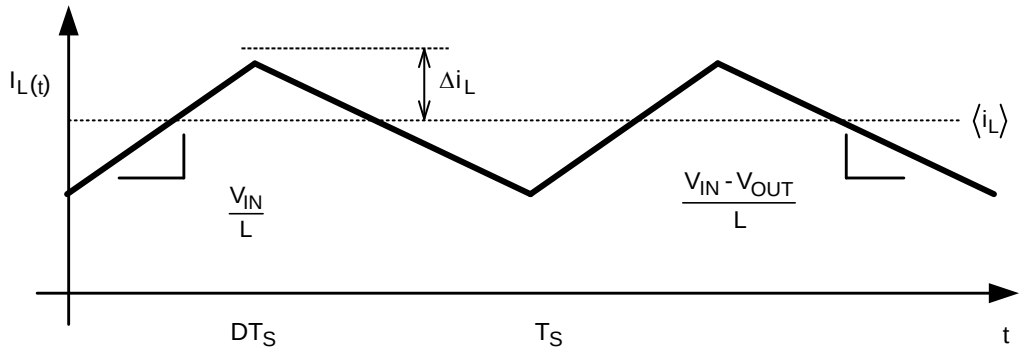


Figure 15. Inductor Current

$$\frac{2\Delta i_L}{DT_S} = \left(\frac{V_{IN}}{L}\right)$$

$$\Delta i_L = \left(\frac{V_{IN}}{2L}\right) x\, DT_S \tag{4}$$

A good design practice is to design the inductor to produce 10% to 30% ripple of maximum load. From the previous equations, the inductor value is then obtained.

$$L = \left(\frac{V_{IN}}{2 \times \Delta i_L}\right) x\, DT_S$$

where

- $1/T_S = F_{SW}$ = switching frequency (5)

One must also ensure that the minimum current limit (2.1A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$IL_{pk} = I_{IN} + \Delta I_L \tag{6}$$

or

$$IL_{pk} = I_{OUT} / D' + \Delta I_L \tag{7}$$

When selecting an inductor, make sure that it is capable of supporting the peak input current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum input current. For example, if the designed maximum input current is 1.5A and the peak current is 1.75A, then the inductor should be specified with a saturation current limit of >1.75A. There is no need to specify the saturation or peak current of the inductor at the 3A typical switch current limit.

Because of the operating frequency of the LMR62421, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (DCR) will provide better operating efficiency. For recommended inductors see Example Circuits.

INPUT CAPACITOR

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and ESL (Equivalent Series Inductance). The recommended input capacitance is 10 µF to 44 µF depending on the application. The capacitor manufacturer specifically states the input voltage rating. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. At the operating frequencies of the LMR62421, certain capacitors may have an ESL so large that the resulting impedance (2πfL) will be higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended. Multilayer ceramic capacitors (MLCC) are good choices for both input and output capacitors and have very low ESL. For MLCCs it is recommended to use X7R or X5R dielectrics. Consult capacitor manufacturer datasheet to see how rated capacitance varies over operating conditions.

OUTPUT CAPACITOR

The LMR62421 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output impedance will therefore determine the maximum voltage perturbation. The output ripple of the converter is a function of the capacitor's reactance and its equivalent series resistance (ESR):

$$\Delta V_{OUT} = \Delta I_L \times R_{ESR} + \left(\frac{V_{OUT} \times D}{2 \times F_{SW} \times R_{Load} \times C_{OUT}} \right) \quad (8)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action .

Given the availability and quality of MLCCs and the expected output voltage of designs using the LMR62421, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum at 4.7 µF of output capacitance. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R. Again, verify actual capacitance at the desired operating voltage and temperature.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the following equation where R1 is connected between the FB pin and GND, and R2 is connected between V_{OUT} and the FB pin.

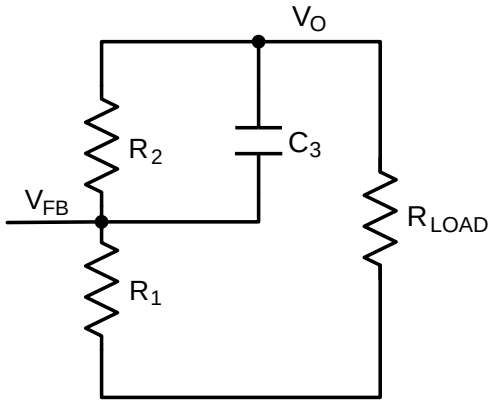


Figure 16. Setting Vout

A good value for R1 is 10kΩ.

$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_1 \quad (9)$$

COMPENSATION

The LMR62421 uses constant frequency peak current mode control. This mode of control allows for a simple external compensation scheme that can be optimized for each application. A complicated mathematical analysis can be completed to fully explain the LMR62421's internal & external compensation, but for simplicity, a graphical approach with simple equations will be used. Below is a Gain & Phase plot of a LMR62421 that produces a 12V output from a 5V input voltage. The Bode plot shows the total loop Gain & Phase without external compensation.

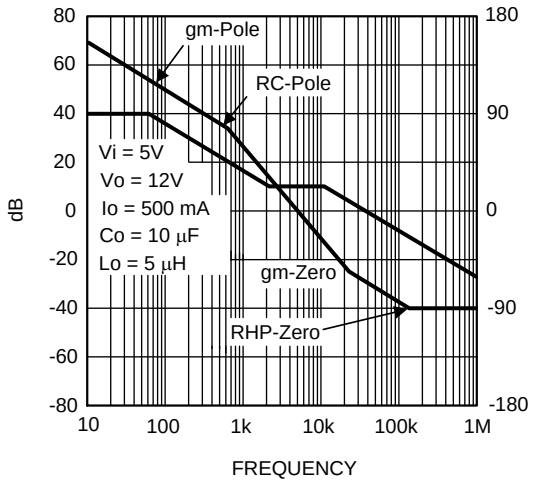


Figure 17. LMR62421 Without External Compensation

One can see that the Crossover frequency is fine, but the phase margin at 0dB is very low (22°). A zero can be placed just above the crossover frequency so that the phase margin will be bumped up to a minimum of 45°. Below is the same application with a zero added at 8 kHz.

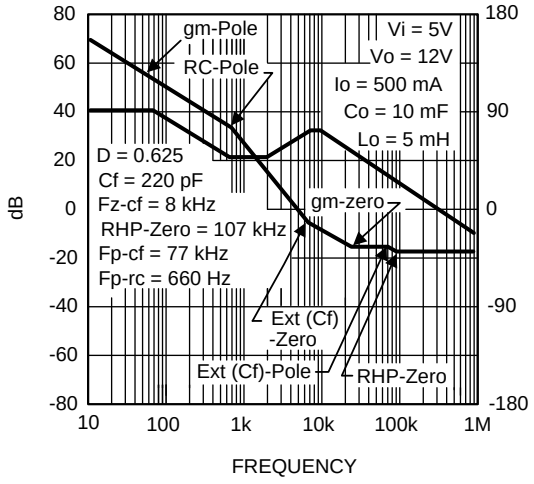


Figure 18. LMR62421 With External Compensation

The simplest method to determine the compensation component value is as follows.

Set the output voltage with the following equation.

$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) x\, R_1$$

where

- R1 is the bottom resistor

and

- R2 is the resistor tied to the output voltage. (10)

The next step is to calculate the value of C3. The internal compensation has been designed so that when a zero is added between 5 kHz & 10 kHz the converter will have good transient response with plenty of phase margin for all input & output voltage combinations.

$$F_{ZERO-CF} = \frac{1}{2\pi(R_2 x C_f)} = 5\ kHz \rightarrow 10\ kHz \quad (11)$$

Lower output voltages will have the zero set closer to 10 kHz, and higher output voltages will usually have the zero set closer to 5 kHz. It is always recommended to obtain a Gain/Phase plot for your actual application. One could refer to the Typical Appplication section to obtain examples of working applications and the associated component values.

Pole @ origin due to internal gm amplifier:

$$F_{P-ORIGIN} \quad (12)$$

Pole due to output load and capacitor:

$$F_{P-RC} = \frac{1}{2\pi(R_{Load} C_{OUT})} \quad (13)$$

This equation only determines the frequency of the pole for perfect current mode control (CMC). Therefore, it doesn't take into account the additional internal artificial ramp that is added to the current signal for stability reasons. By adding artificial ramp, you begin to move away from CMC to voltage mode control (VMC). The artifact is that the pole due to the output load and output capacitor will actually be slightly higher in frequency than calculated. In this example it is calculated at 650 Hz, but in reality it is around 1 kHz.

The zero created with capacitor C3 & resistor R2:

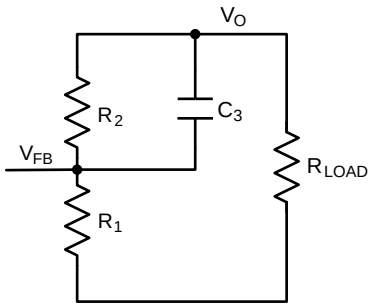


Figure 19. Setting External Pole-Zero

$$F_{ZERO-CF} = \frac{1}{2\pi(R_2 \times C_3)} \quad (14)$$

There is an associated pole with the zero that was created in the above equation.

$$F_{POLE-CF} = \frac{1}{2\pi((R_1 \| R_2) \times C_3)} \quad (15)$$

It is always higher in frequency than the zero.

A right-half plane zero (RHPZ) is inherent to all boost converters. One must remember that the gain associated with a right-half plane zero increases at 20dB per decade, but the phase decreases by 45° per decade. For most applications there is little concern with the RHPZ due to the fact that the frequency at which it shows up is well beyond crossover, and has little to no effect on loop stability. One must be concerned with this condition for large inductor values and high output currents.

$$RHP_{ZERO} = \frac{(D')^2 R_{Load}}{2\pi \times L} \quad (16)$$

There are miscellaneous poles and zeros associated with parasitics internal to the LMR62421, external components, and the PCB. They are located well over the crossover frequency, and for simplicity are not discussed.

PCB Layout Considerations

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration when completing a Boost Converter layout is the close coupling of the GND connections of the C_{OUT} capacitor and the LMR62421 PGND pin. The GND ends should be close to one another and be connected to the GND plane with at least two through-holes. There should be a continuous ground plane on the bottom layer of a two-layer board. The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the AGND of R1 placed as close as possible to the GND (pin 5 for the WSON) of the IC. The V_{OUT} trace to R2 should be routed away from the inductor and any other traces that are switching. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor. The remaining components should also be placed as close as possible to the IC. Please see Application Note AN-1229 SNVA054 for further considerations and the LMR62421 demo board as an example of a good layout.

SEPIC Converter

The LMR62421 can easily be converted into a SEPIC converter. A SEPIC converter has the ability to regulate an output voltage that is either larger or smaller in magnitude than the input voltage. Other converters have this ability as well (CUK and Buck-Boost), but usually create an output voltage that is opposite in polarity to the input voltage. This topology is a perfect fit for Lithium Ion battery applications where the input voltage for a single cell Li-Ion battery will vary between 3V & 4.5V and the output voltage is somewhere in between. Most of the analysis of the LMR62421 Boost Converter is applicable to the LMR62421 SEPIC Converter.

SEPIC Design Guide:

SEPIC Conversion ratio without loss elements:

$$\frac{V_o}{V_{IN}} = \frac{D}{D'} \quad (17)$$

Therefore:

$$D = \frac{V_O}{V_O + V_{IN}} \quad (18)$$

Small ripple approximation:

In a well-designed SEPIC converter, the output voltage, and input voltage ripple, the inductor ripple and is small in comparison to the DC magnitude. Therefore it is a safe approximation to assume a DC value for these components. The main objective of the Steady State Analysis is to determine the steady state duty-cycle, voltage and current stresses on all components, and proper values for all components.

In a steady-state converter, the net volt-seconds across an inductor after one cycle will equal zero. Also, the charge into a capacitor will equal the charge out of a capacitor in one cycle.

Therefore:

$$I_{L2} = \left(\frac{D}{D'}\right) \times I_{L1}$$

and

$$I_{L1} = \left(\frac{D}{D'}\right) X \left(\frac{V_O}{R}\right) \quad (19)$$

Substituting I_{L1} into I_{L2}

$$I_{L2} = \frac{V_O}{R} \quad (20)$$

The average inductor current of L2 is the average output load.

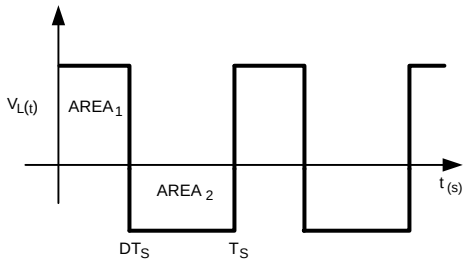


Figure 20. Inductor Volt-Sec Balance Waveform

Applying Charge balance on C1:

$$V_{C1} = \frac{D'(V_0)}{D} \quad (21)$$

Since there are no DC voltages across either inductor, and capacitor C6 is connected to Vin through L1 at one end, or to ground through L2 on the other end, we can say that

$$V_{C1} = V_{IN} \quad (22)$$

Therefore:

$$V_{IN} = \frac{D'(V_0)}{D} \quad (23)$$

This verifies the original conversion ratio equation.

It is important to remember that the internal switch current is equal to I_{L1} and I_{L2}. During the D interval. Design the converter so that the minimum ensured peak switch current limit (2.1A) is not exceeded.

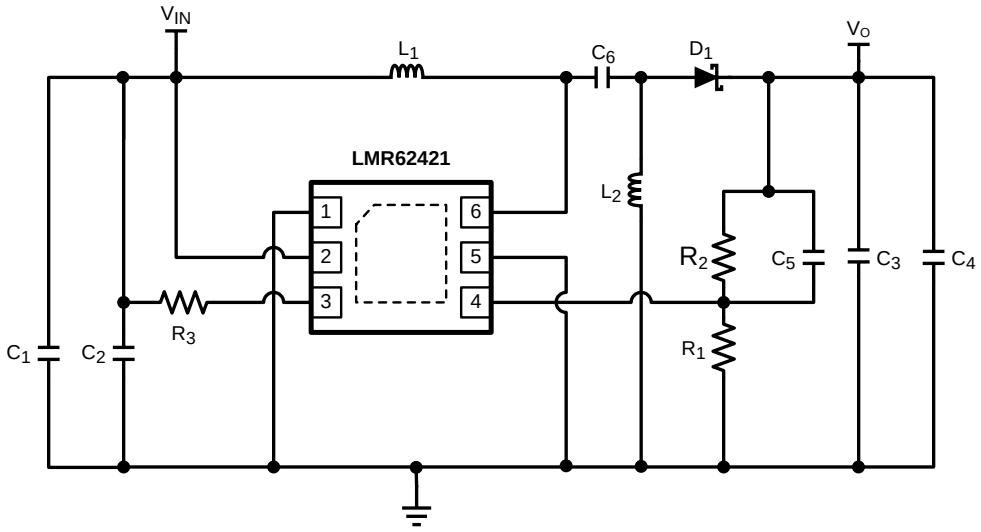
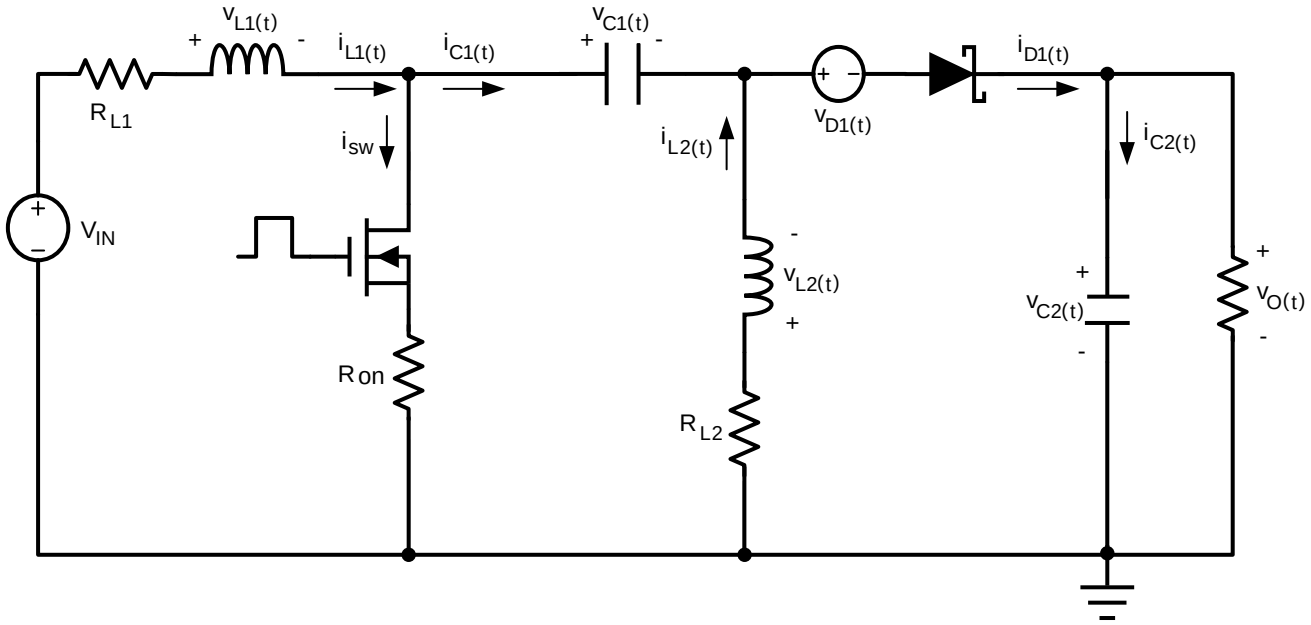


Figure 21. SEPIC CONVERTER Schematic

Steady State Analysis with Loss Elements



Using inductor volt-second balance & capacitor charge balance, the following equations are derived:

$$I_{L2} = \left(\frac{V_O}{R}\right)$$

and

$$I_{L1} = \left(\frac{V_O}{R}\right) x \left(\frac{D}{D'}\right) \quad (24)$$

$$\frac{V_0}{V_{IN}} = \left(\frac{D}{D'}\right)\left(\frac{1}{\left(1+\frac{V_D}{V_O}+\frac{R_{L2}}{R}\right)+\left(\frac{D}{D'^2}\right)\left(\frac{R_{ON}}{R}\right)+\left(\frac{D^2}{D'^2}\right)\left(\frac{R_{L1}}{R}\right)}\right) \quad (25)$$

Therefore:

$$\eta = \left(\frac{1}{\left(1+\frac{V_D}{V_O}+\frac{R_{L2}}{R}\right)+\left(\frac{D}{D'^2}\right)\left(\frac{R_{ON}}{R}\right)+\left(\frac{D^2}{D'^2}\right)\left(\frac{R_{L1}}{R}\right)}\right) \quad (26)$$

One can see that all variables are known except for the duty cycle (D). A quadratic equation is needed to solve for D. A less accurate method of determining the duty cycle is to assume efficiency, and calculate the duty cycle.

$$\frac{V_O}{V_{IN}} = \left(\frac{D}{1 - D}\right) x \, \eta \quad (27)$$

$$D = \left(\frac{V_O}{(V_{IN} x \, \eta) + V_O}\right) \quad (28)$$

Table 1. Efficiencies for Typical SEPIC Application

Vin	2.7V	Vin	3.3V	Vin	5V
Vo	3.1V	Vo	3.1V	Vo	3.1V
Iin	770 mA	Iin	600mA	Iin	375 mA
Io	500 mA	Io	500mA	Io	500 mA
η	75%	η	80%	η	83%

SEPIC Converter PCB Layout

The layout guidelines described for the LMR62421 Boost-Converter are applicable to the SEPIC Converter. Below is a proper PCB layout for a SEPIC Converter.

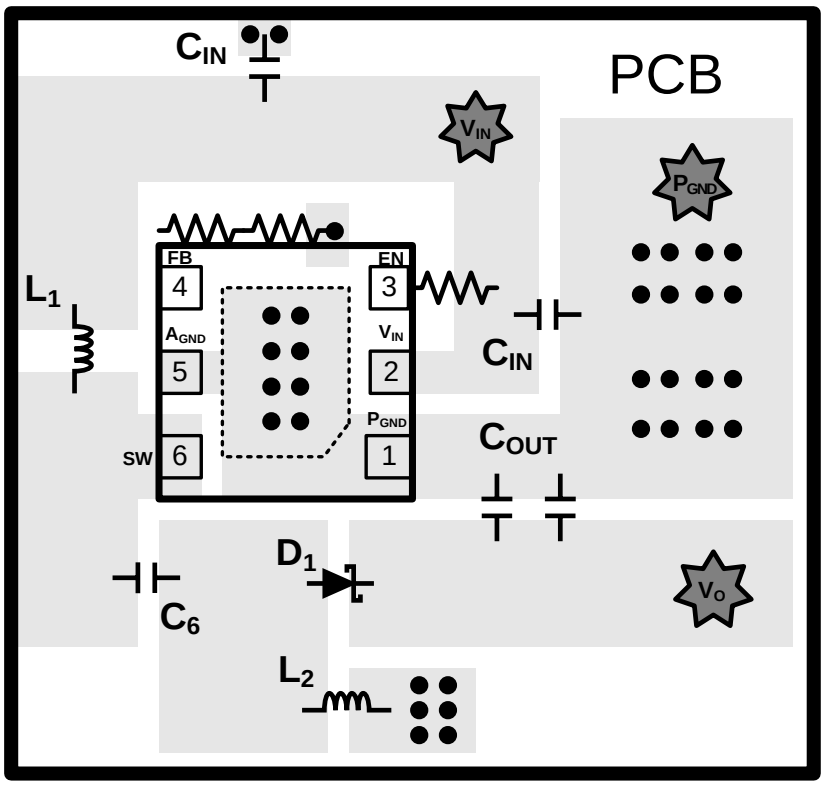


Figure 22. SEPIC PCB Layout

WSON Package

The LMR62421 packaged in the 6–pin WSON:

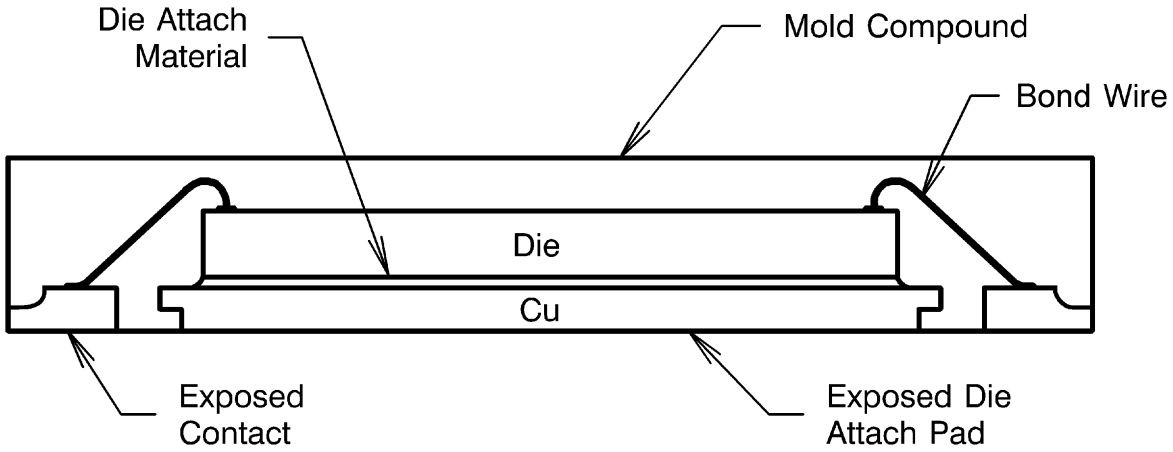


Figure 23. Internal WSON Connection

For certain high power applications, the PCB land may be modified to a "dog bone" shape (see Figure 24). Increasing the size of ground plane, and adding thermal vias can reduce the $R_{\theta JA}$ for the application.

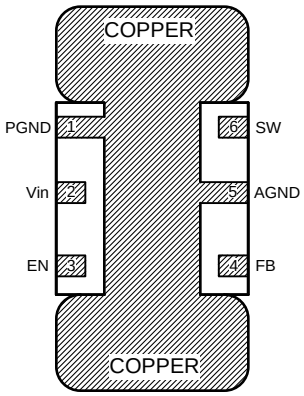


Figure 24. PCB Dog Bone Layout

LMR62421 Design Example 1

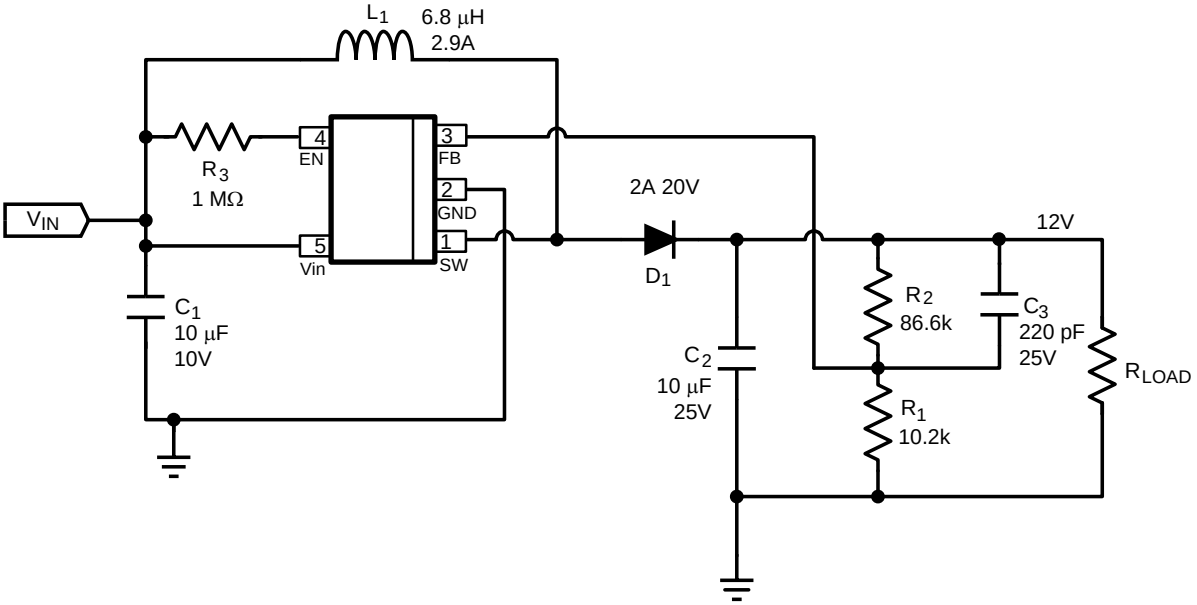


Figure 25. Vin = 3V - 5V, Vout = 12V @ 500 mA

LMR62421 Design Example 2

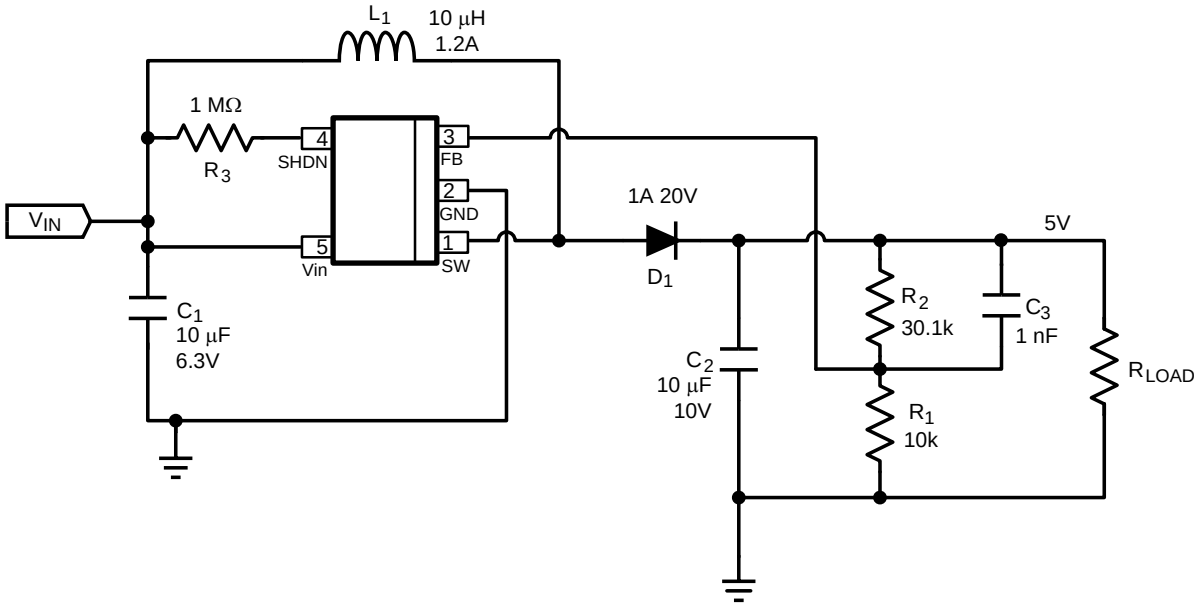


Figure 26. Vin = 3V, Vout = 5V @ 500 mA

LMR62421 Design Example 3

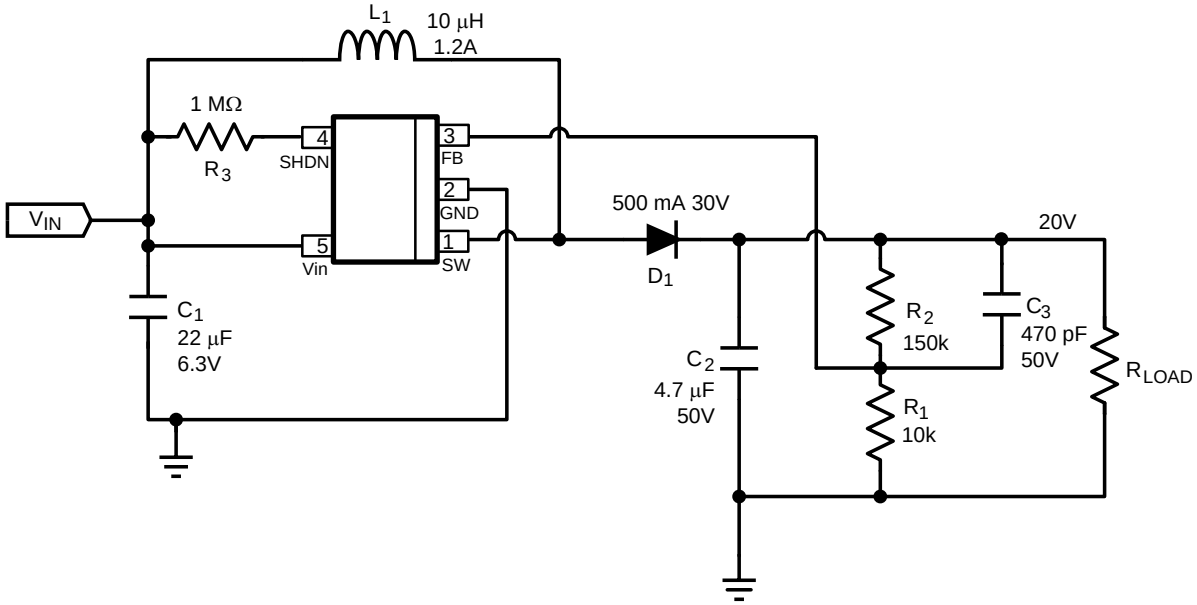


Figure 27. Vin = 3.3V, Vout = 20V @ 100 mA

LMR62421 SEPIC Design Example 4

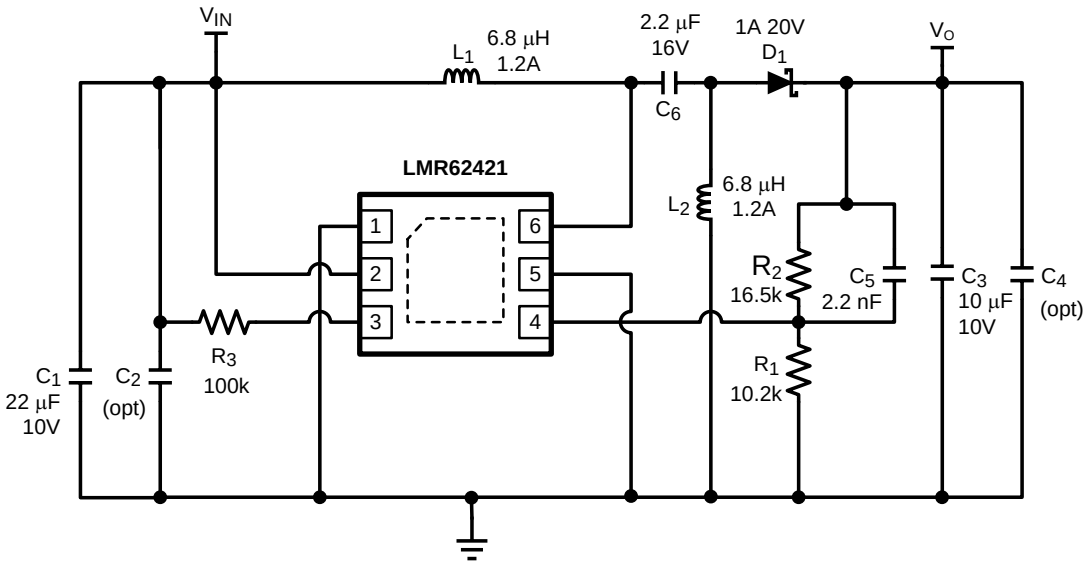


Figure 28. Vin = 2.7V - 5V, Vout = 3.3V @ 500mA

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR62421XMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SH8B	Samples
LMR62421XMFE/NOPB	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SH8B	Samples
LMR62421XMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SH8B	Samples
LMR62421XSD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L270B	Samples
LMR62421XSDE/NOPB	ACTIVE	WSON	NGG	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L270B	Samples
LMR62421XSDX/NOPB	ACTIVE	WSON	NGG	6	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L270B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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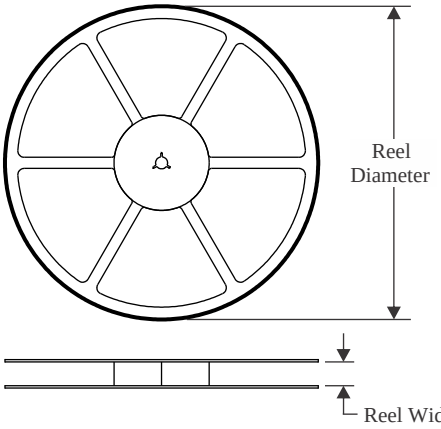
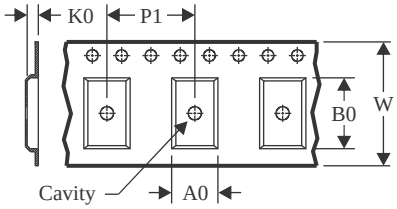
TAPE AND REEL INFORMATION

REEL DIMENSIONS

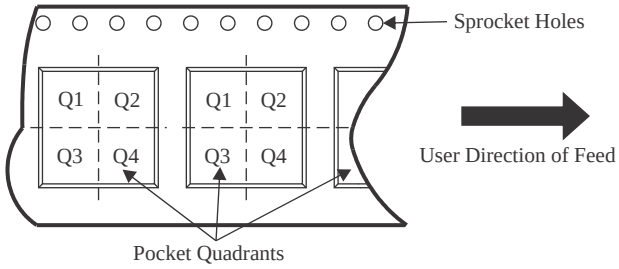


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

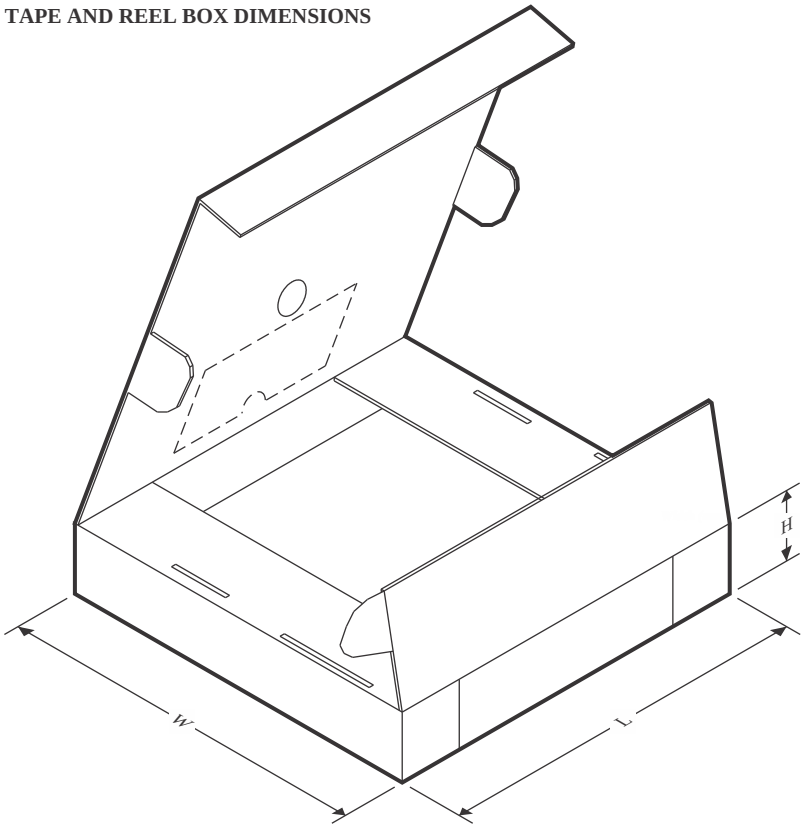
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR62421XMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR62421XMFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR62421XMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR62421XSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR62421XSDE/NOPB	WSON	NGG	6	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR62421XSDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

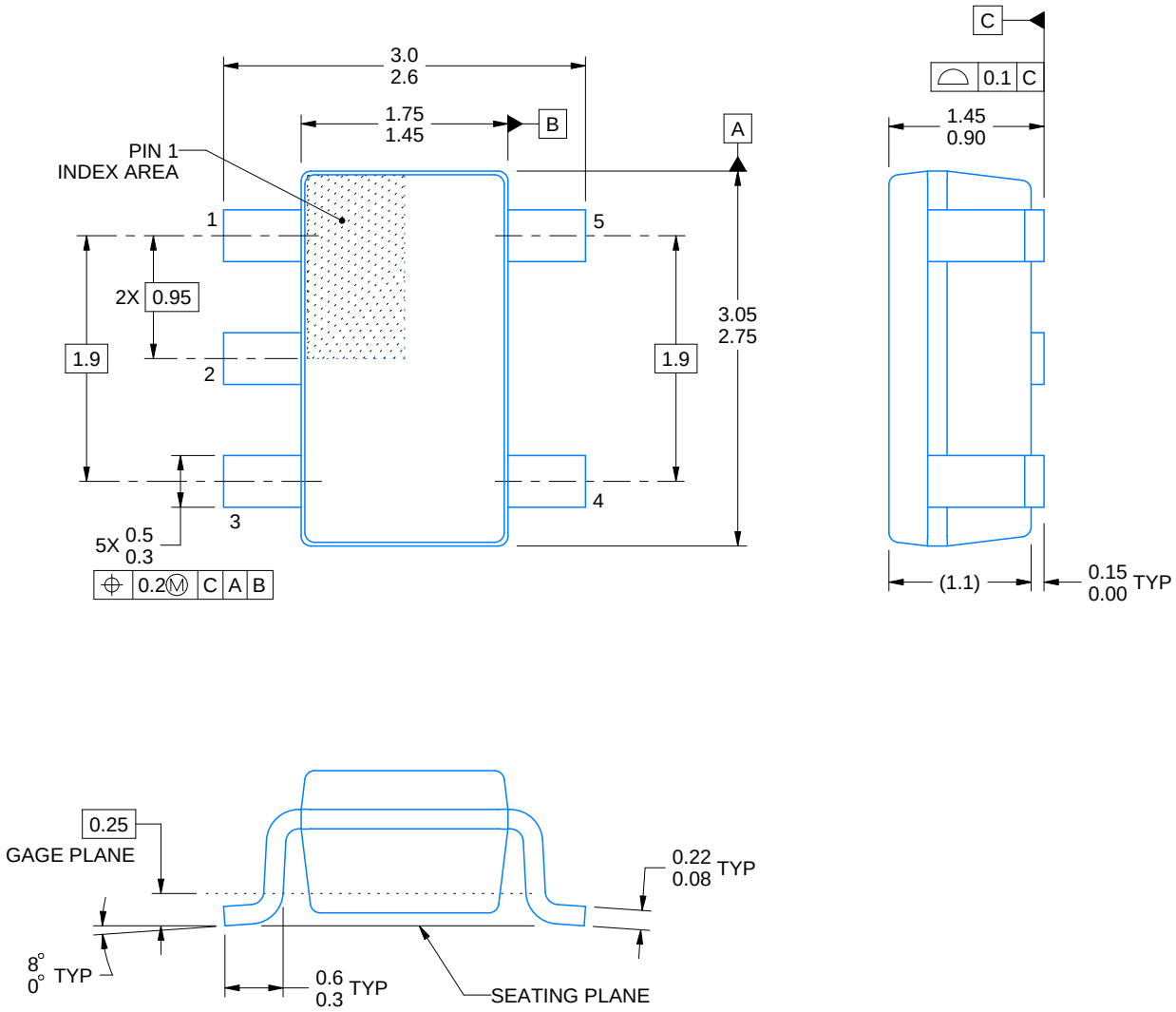
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR62421XMF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMR62421XMFE/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LMR62421XMFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMR62421XSD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LMR62421XSDE/NOPB	WSON	NGG	6	250	208.0	191.0	35.0
LMR62421XSDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

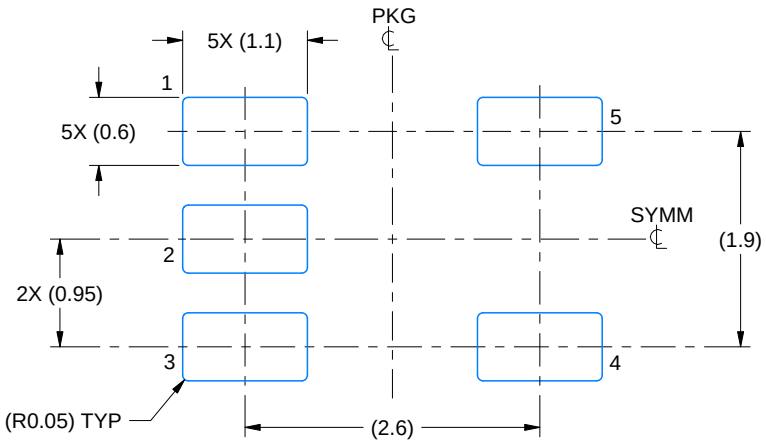
SMALL OUTLINE TRANSISTOR



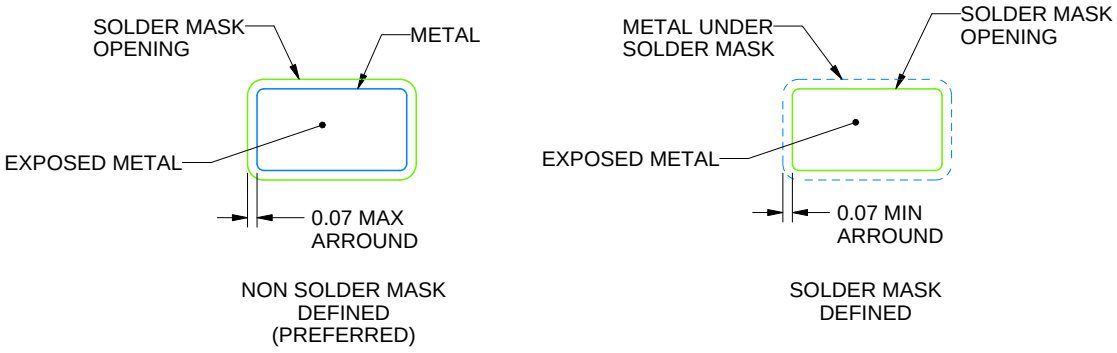
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

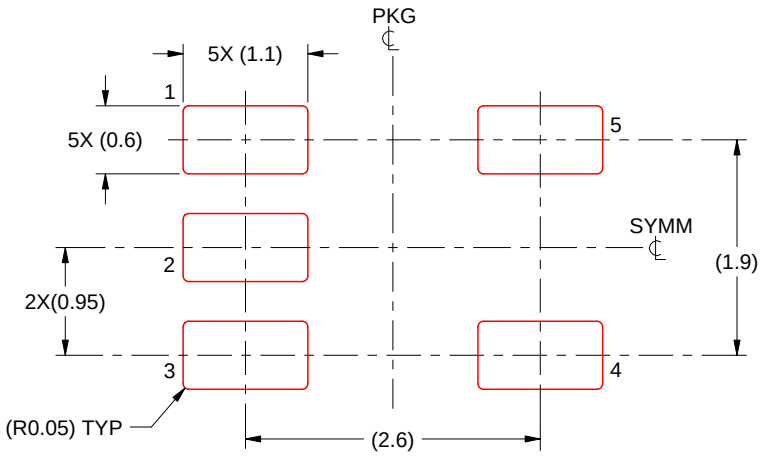


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



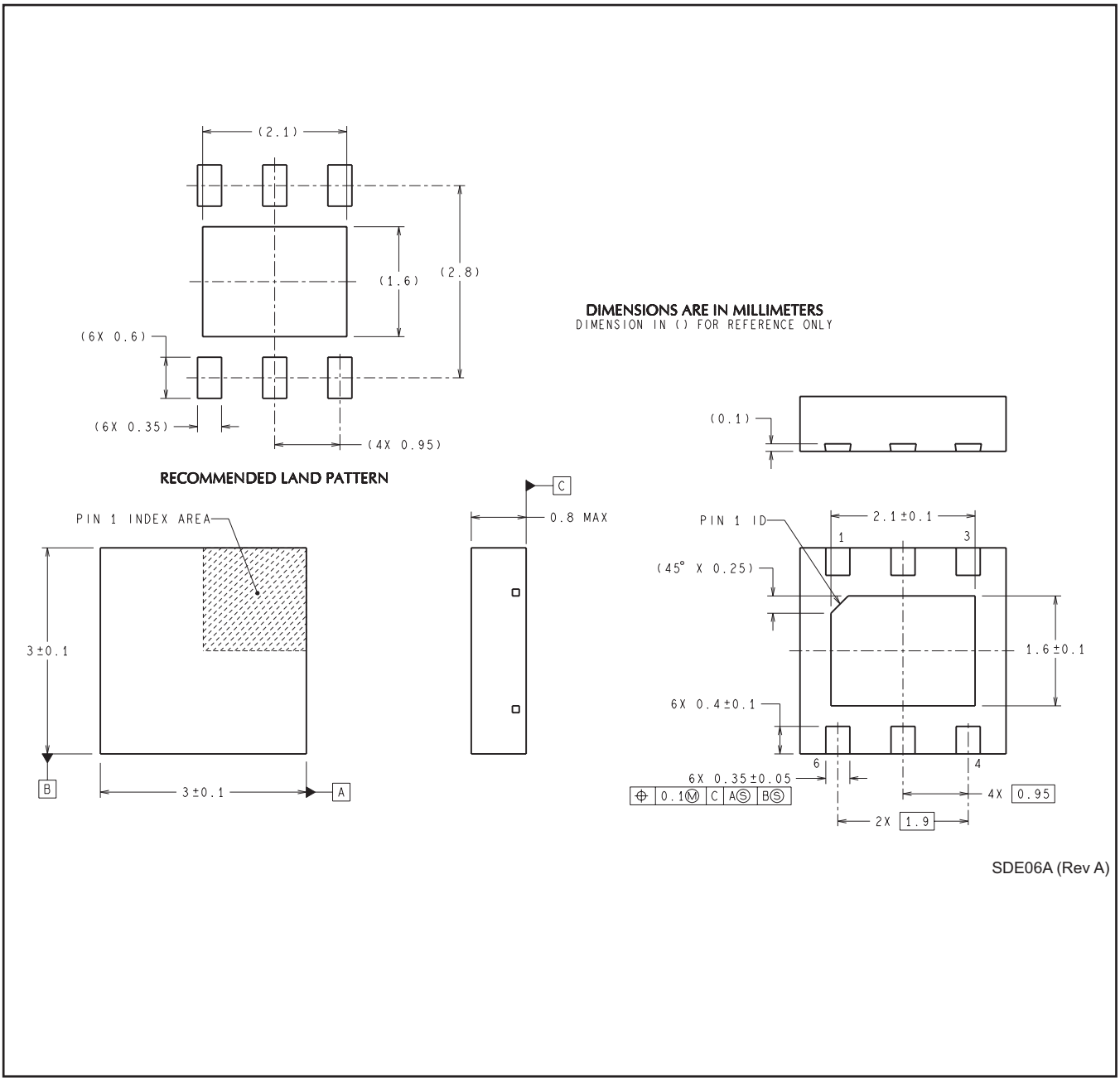
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

NGG0006A



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