3MHz, 600mA Miniature Step-Down DC-DC Converter for Ultra Low Voltage Circuits

Check for Samples: LM3677

FEATURES

- **16 µA typical quiescent current**
- **600 mA maximum load capability**
- **3 MHz PWM fixed switching frequency (typ.)**
- **Automatic PFM/PWM mode switching**
- **Available in 5-bump DSBGA package and 6-pin USON package**
- **Internal synchronous rectification for high efficiency**
- **Internal soft start**
- **0.01 µA typical shutdown current**
- **Operates from a single Li-Ion cell battery**
- **Only three tiny surface-mount external components required (solution size less than 20 mm^2)**
- **Current overload and thermal shutdown protection**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **MP3 Players**
- **W-LAN**
- **Portable Instruments**
- **Digital Still Cameras**
- **Portable Hard Disk Drives**

DESCRIPTION

The LM3677 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Li-Ion cell battery and input voltage rails from 2.7V to 5.5V. It provides up to 600 mA load current over the entire input voltage range. The LM3677 is configured to different fixed voltage output options as well as an adjustable output voltage version range from 1.2V to 3.3V.

TYPICAL APPLICATION CIRCUITS

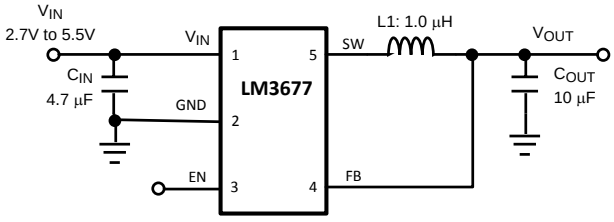


Figure 1. Typical Application Circuit

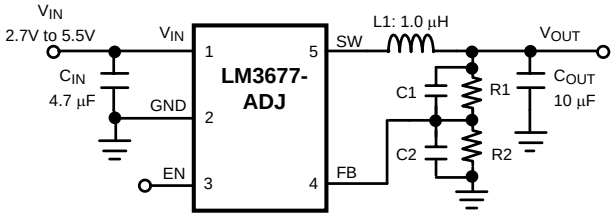


Figure 2. Typical Application Circuit - ADJ. Version

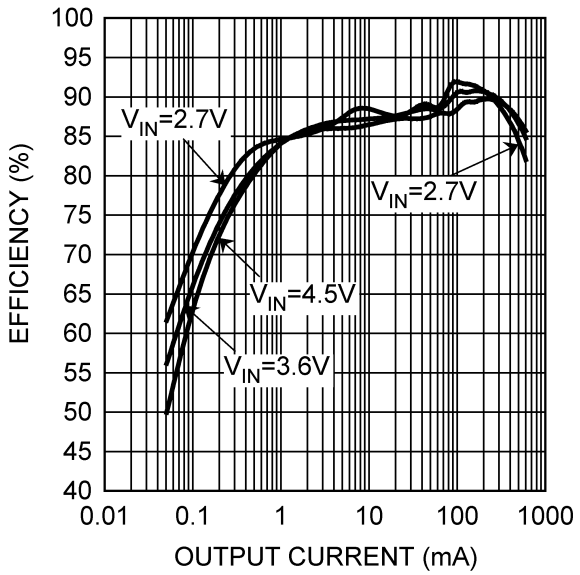


Figure 3. Efficiency vs. Output Current (V_{OUT} = 1.8V)

DESCRIPTION (CONTINUED)

The device offers superior features and performance for mobile phones and similar portable applications with complex power management systems. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During PWM mode operation, the device operates at a fixed frequency of 3 MHz (typ). PWM mode drives loads from ~ 80 mA to 600 mA max. Hysteretic PFM mode extends the battery life by reducing the quiescent current to 16 µA (typ.) during light load and standby operation. Internal synchronous rectification provides high efficiency. In shutdown mode (Enable pin pulled down), the device turns off and reduces battery consumption to 0.01 µA (typ.).

The LM3677 is available in a lead-free (NOPB) 5-bump DSBGA package and 6-pin USON package. A switching frequency of 3 MHz (typ.) allows use of tiny surface-mount components. Only three external surface-mount components, an inductor and two ceramic capacitors, are required.

CONNECTION DIAGRAMS

5-Bump DSBGA Package
See Package Number YZR0005

6-Pin USON Package
See Package Number NGE0006A

PIN DESCRIPTIONS(1)

Name	Pin No.		Description
V_{IN}	A1	1	Power supply input. Connect to the input filter capacitor (Figure 1).
GND	A3	6	Ground pin.
EN	C1	3	Enable pin. The device is in shutdown mode when voltage to this pin is < 0.4V and enabled when > 1.0V. Do not leave this pin floating.
FB	C3	4	Feedback analog input. Connect directly to the output filter capacitor (FIGURE 1).
SW	B2	2, 5	Switching node connection to the internal PFET switch and NFET synchronous rectifier.

(1) For output voltage 1.2V or lower, input voltage needs to be derated to the range of 2.7V to 5.0V in order to perform within specification.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributor for availability and specifications.

V_{IN} Pin: Voltage to GND	−0.2V to 6.0V
FB, SW, EN Pin:	(GND−0.2V) to (V_{IN} + 0.2V)
Continuous Power Dissipation (3)	Internally Limited
Junction Temperature (T_{J-MAX})	+125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating (4)	
Human Body Model: All Pins	2.0 kV
Machine Model: All Pins	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 150°C (typ.) and disengages at T_J= 130°C (typ.).
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

OPERATING RATINGS(1), (2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0 mA to 600 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In Applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX}), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction to ambient thermal resistance of the package (θ_{JA}) in the application, as given by the following equation: T_{A-MAX}= T_{J-MAX}− (θ_{JA}x P_{D-MAX}). Refer to Dissipation rating table for P_{D-MAX} values at different ambient temperatures.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ_{JA}) (1)	85°C/W

(1) Junction to ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design. Value specified here 85 °C/W is based on measurement results using a 4 layer board as per JEDEC standards.

ELECTRICAL CHARACTERISTICS(1)(2)(3)

Limits in standard typeface are for $T_J = T_A = 25°C$. Limits in **boldface** type apply over the operating ambient temperature range ($-30°C \le T_A \le +85°C$). Unless otherwise noted, specifications apply to the LM3677 with V_{IN} = EN = 3.6V.

Parameter		Test Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage (4)		2.7		5.5	V
V_{FB}	Feedback Voltage (TL)	PWM mode	**-2.5**		**+2.5**	%
	Feedback Voltage (LE)		**-4.0**		**+4.0**	
V_{REF}	Internal Reference Voltage			0.5		V
I_{SHDN}	Shutdown Supply Current	EN = 0V		0.01	**1**	µA
I_Q	DC Bias Current into V_{IN}	No load, device is not switching		16	**35**	µA
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	V_{IN}= V_{GS}= 3.6V, I_{SW}= 100mA		350	450	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for NFET	V_{IN}= V_{GS}= 3.6V, I_{SW}= -100mA		150	250	mΩ
I_{LIM}	Switch Peak Current Limit	Open Loop(5)	**1085**	1220	**1375**	mA
V_{IH}	Logic High Input		**1.0**			V
V_{IL}	Logic Low Input				**0.4**	V
I_{EN}	Enable (EN) Input Current			0.01	**1**	µA
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**2.5**	3	**3.5**	MHz

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested under open loop conditions at V_{IN}= 3.6V unless otherwise specified. For performance over the input voltage range and closed loop condition, refer to the datasheet curves.
(4) For output voltage 1.2V or lower, input voltage needs to be derated to the range of 2.7V to 5.0V in order to perform within specification.
(5) Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB=0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

DISSIPATION RATING TABLE

θ_{JA}	$T_A \le 25°C$ Power Rating	$T_A = 60°C$ Power Rating	$T_A = 85°C$ Power Rating
85°C/W (4-layer board) DSBGA	1178 mW	785 mW	470 mW
117°C/W (4-layer board) USON	855 mW	556 mW	342 mW

BLOCK DIAGRAM

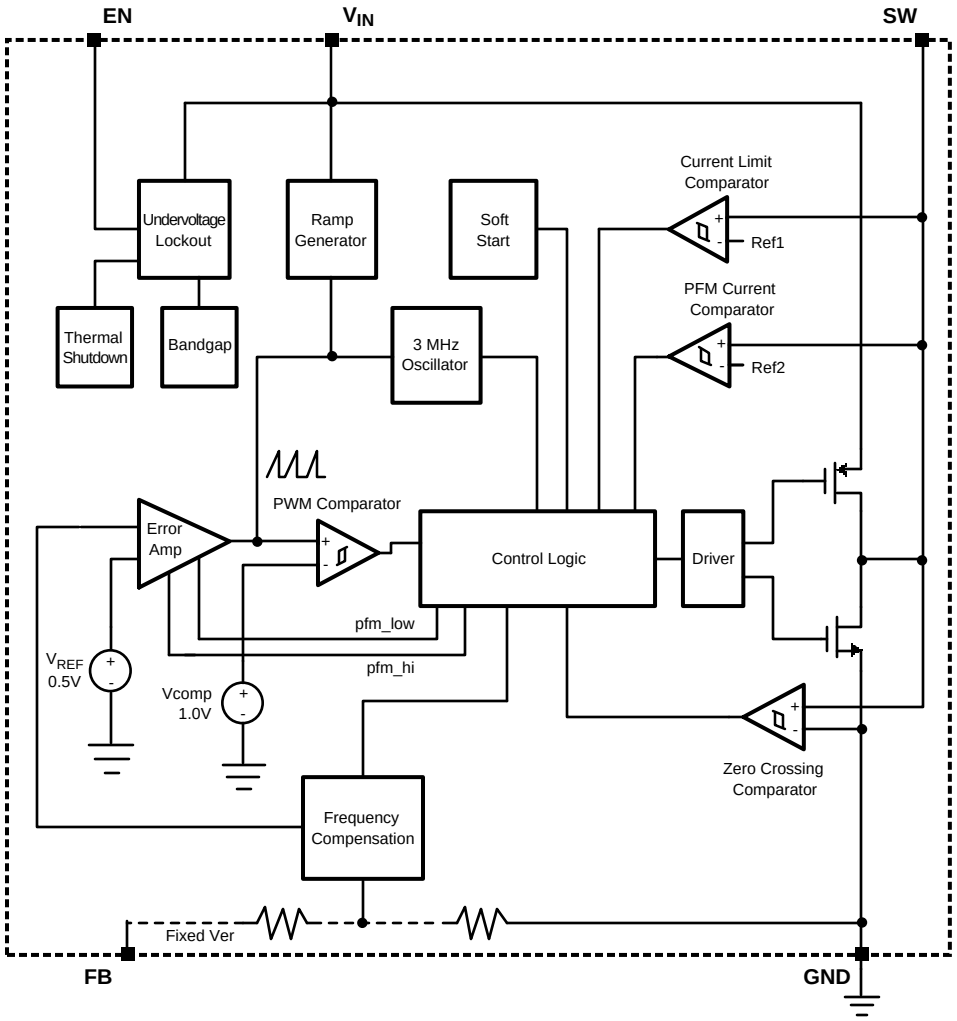


Figure 4. Simplified Functional Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

LM3677, Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

Quiescent Supply Current vs. Supply Voltage (Switching)

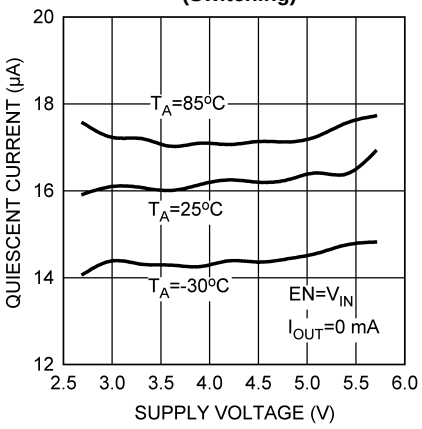


Figure 5.

Shutdown Current vs. Temp

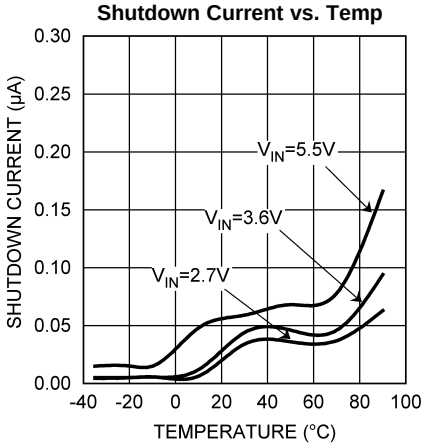


Figure 6.

Switching Frequency vs. Temperature

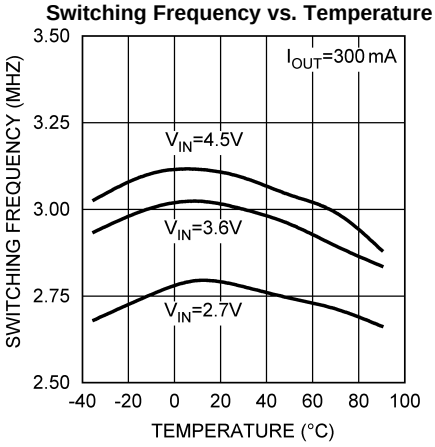


Figure 7.

$R_{DS(ON)}$ vs. Temperature

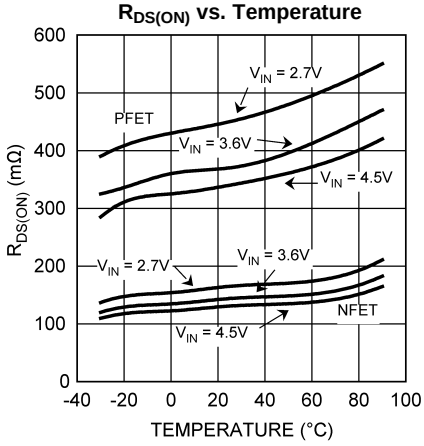


Figure 8.

Open/Closed Loop Current Limit vs. Temperature

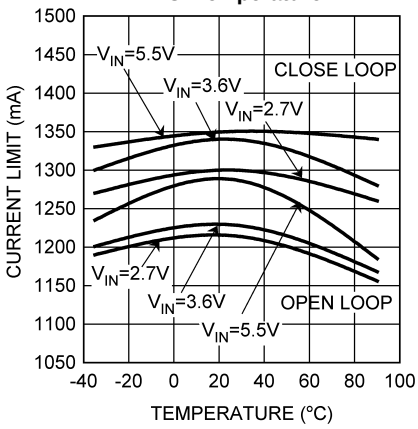


Figure 9.

Output Voltage vs. Supply Voltage (V_{OUT} = 1.8V)

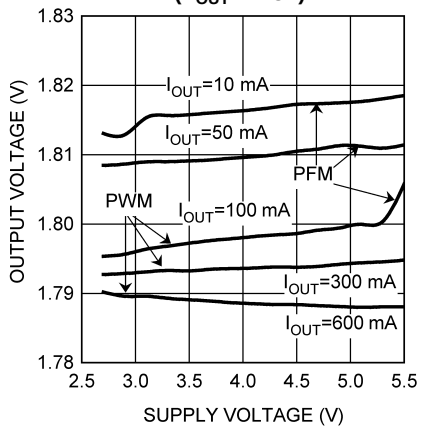


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM3677, Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

Output Voltage vs. Supply Voltage (V_{OUT} = 2.5V)

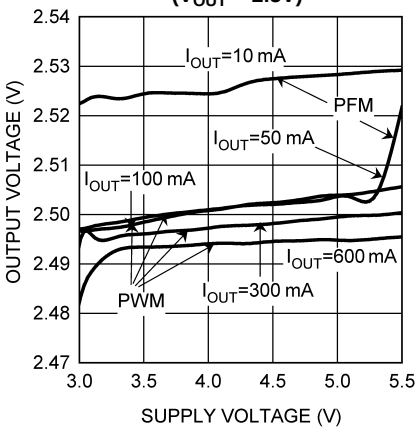


Figure 11.

Output Voltage vs. Temperature (V_{OUT} = 1.3V)

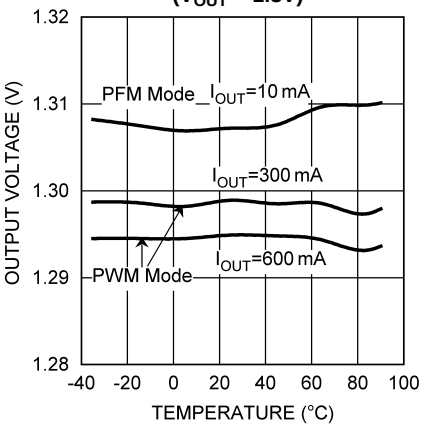


Figure 12.

Output Voltage vs. Temperature (V_{OUT} = 1.8V)

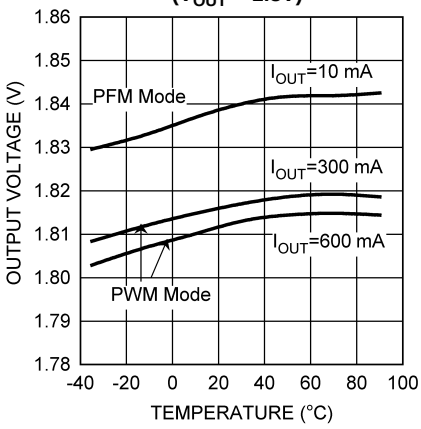


Figure 13.

Output Voltage vs. Temperature (V_{OUT} = 2.5V)

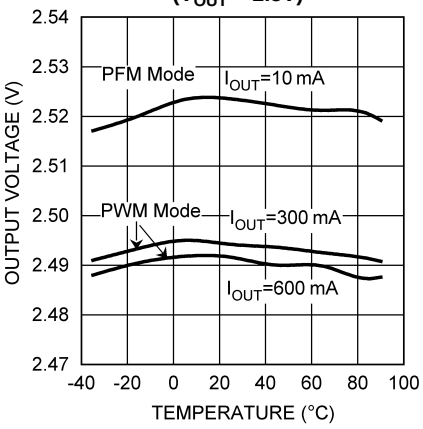


Figure 14.

Output Voltage vs. Output Current (V_{OUT} = 1.8V)

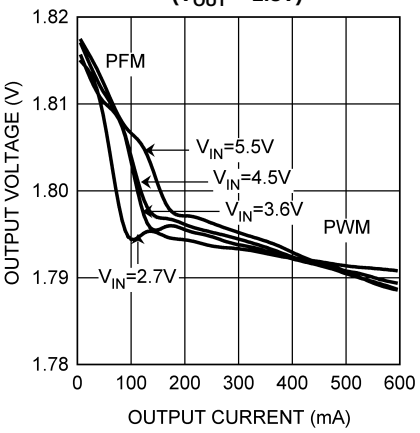


Figure 15.

Output Voltage vs. Output Current (V_{OUT} = 2.5V)

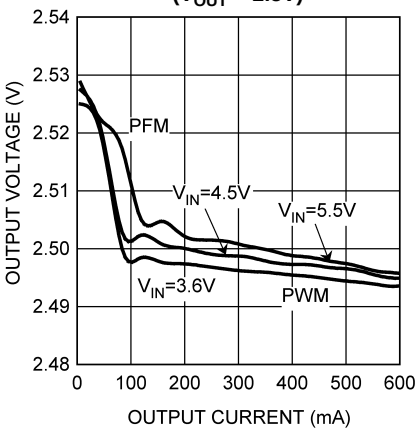


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM3677, Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current (V_{OUT} = 1.3V)

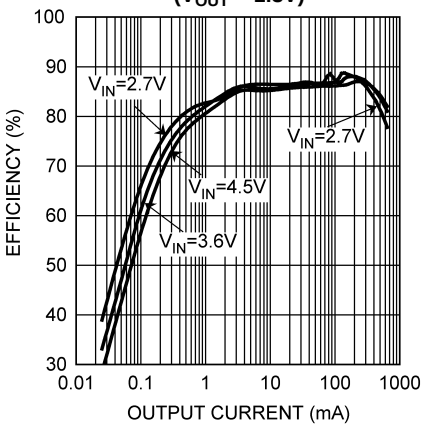


Figure 17.

Efficiency vs. Output Current (V_{OUT} = 1.8V)

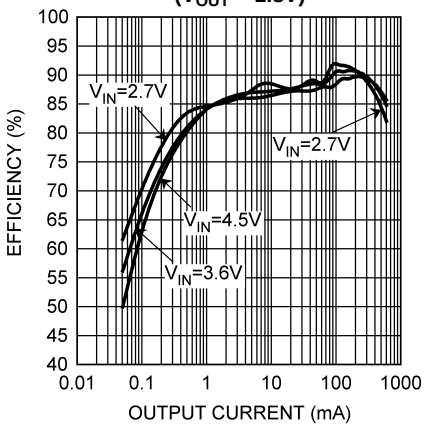


Figure 18.

Efficiency vs. Output Current (V_{OUT} = 2.5V)

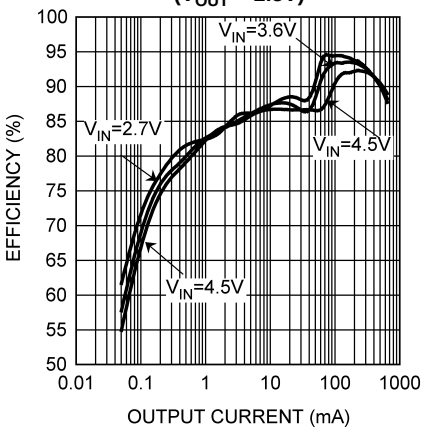


Figure 19.

Output Current vs. Input Voltage at Mode Change Point (V_{OUT} = 1.3V)

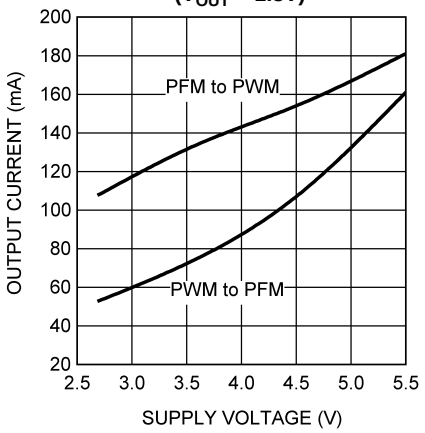


Figure 20.

Output Current vs. Input Voltage at Mode Change Point (V_{OUT} = 1.8V)

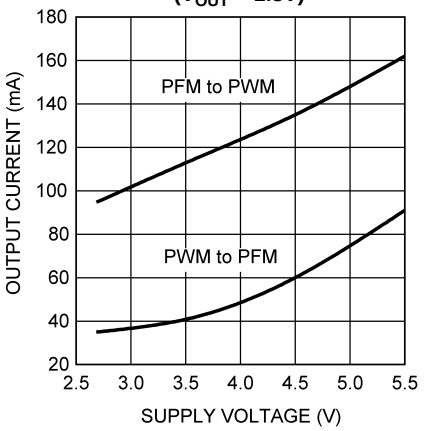


Figure 21.

Output Current vs. Input Voltage at Mode Change Point (V_{OUT} = 2.5V)

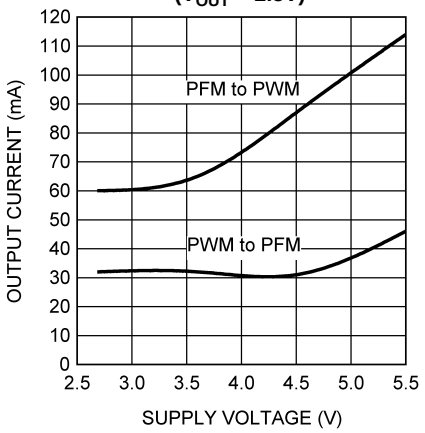


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM3677, Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

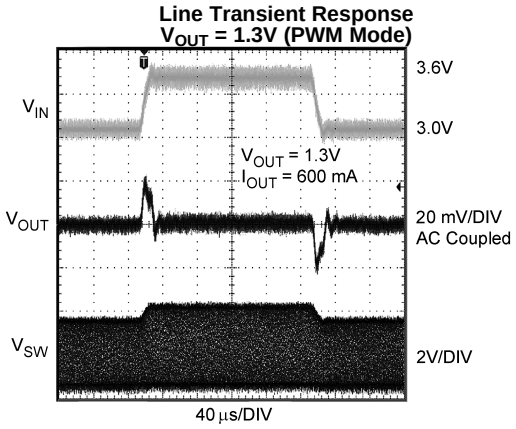


Figure 23.

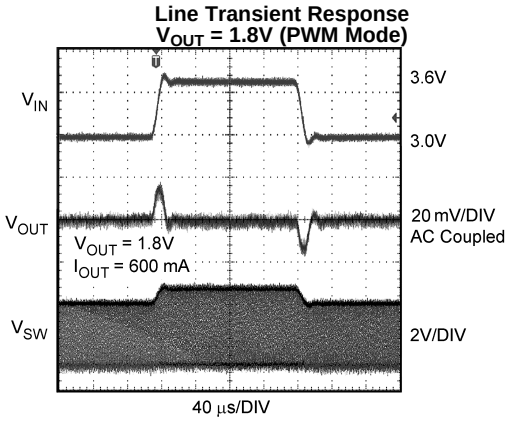


Figure 24.

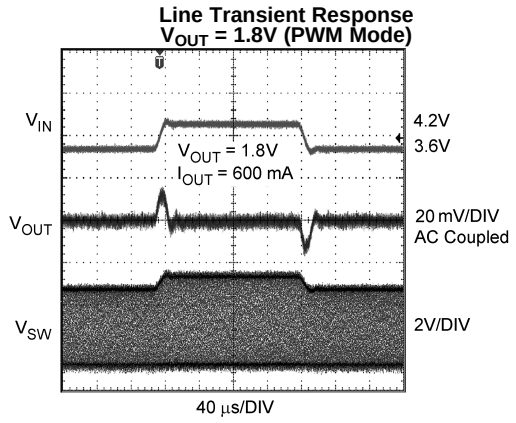


Figure 25.

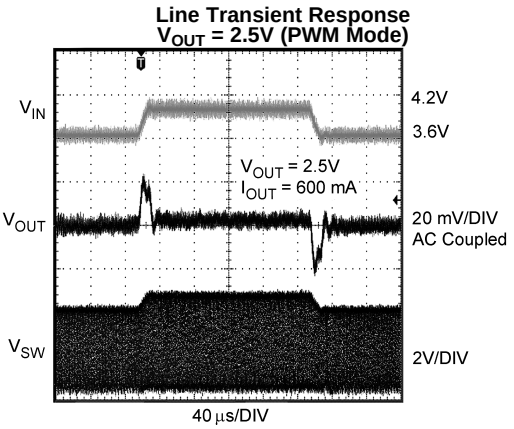


Figure 26.

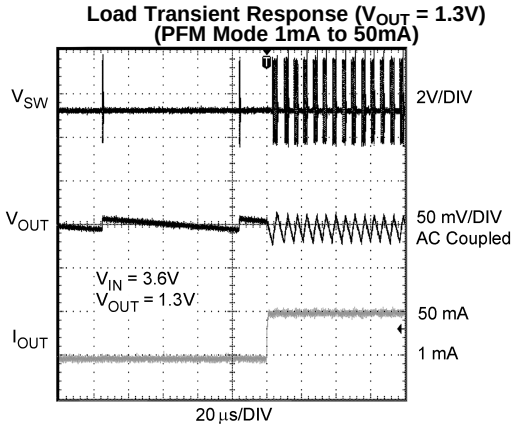


Figure 27.

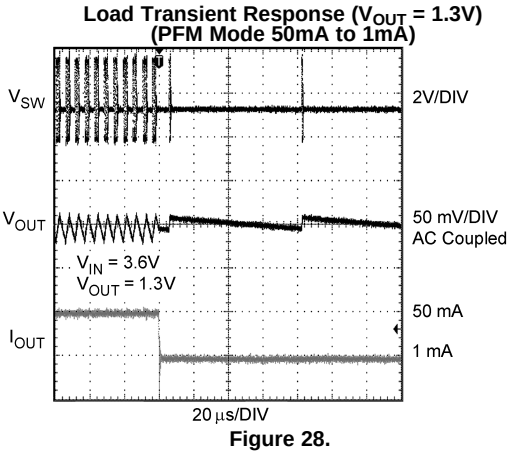


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM3677, Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

Load Transient Response (V_{OUT} = 1.8V)
(PFM Mode 1mA to 50mA)

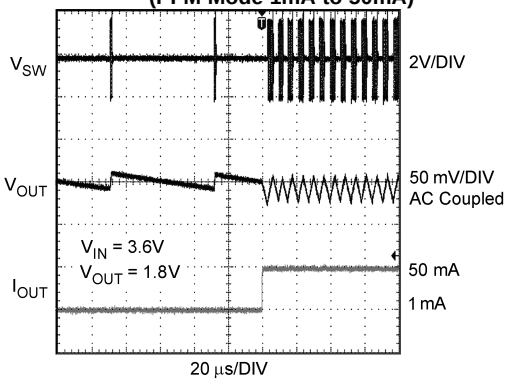


Figure 29.

Load Transient Response (V_{OUT} = 1.8V)
(PFM Mode 50mA to 1mA)

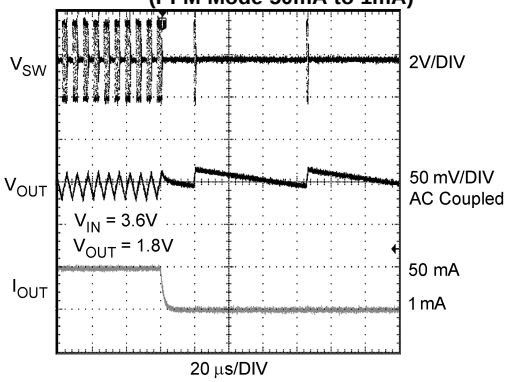


Figure 30.

Load Transient Response (V_{OUT} = 2.5V)
(PFM Mode 1mA to 50mA)

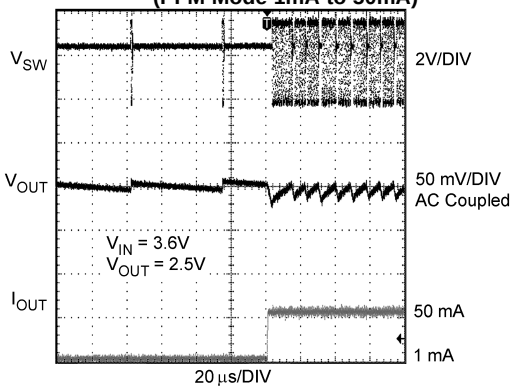


Figure 31.

Load Transient Response (V_{OUT} = 2.5V)
(PFM Mode 50mA to 1mA)

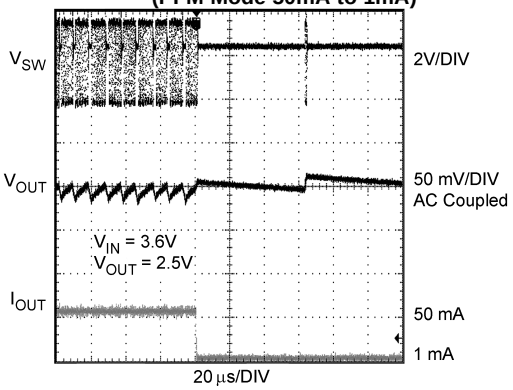


Figure 32.

Mode Change by Load Transients
V_{OUT} = 1.3V (PFM to PWM)

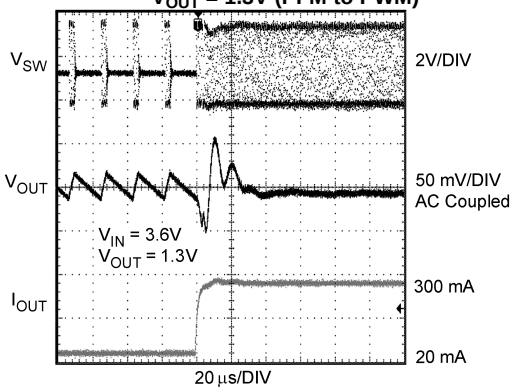


Figure 33.

Mode Change by Load Transients
V_{OUT} = 1.3V (PWM to PFM)

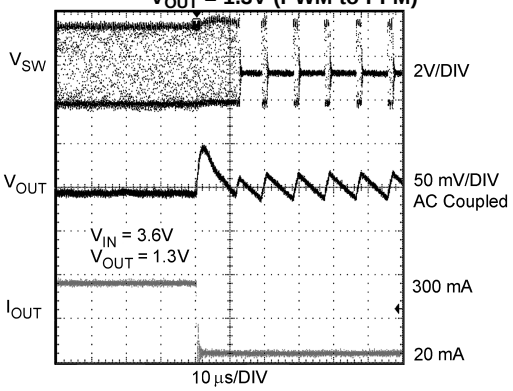


Figure 34.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM3677, Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

Mode Change by Load Transients
V_{OUT} = 1.8V (PFM to PWM)

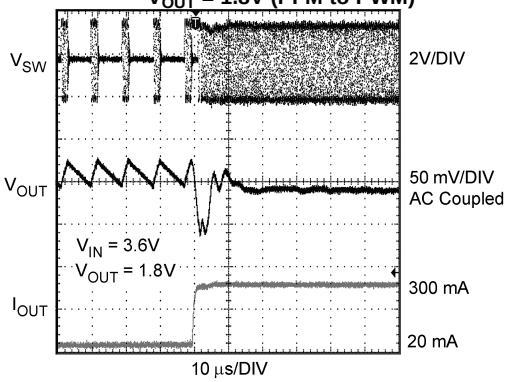


Figure 35.

Mode Change by Load Transients
V_{OUT} = 1.8V (PWM to PFM)

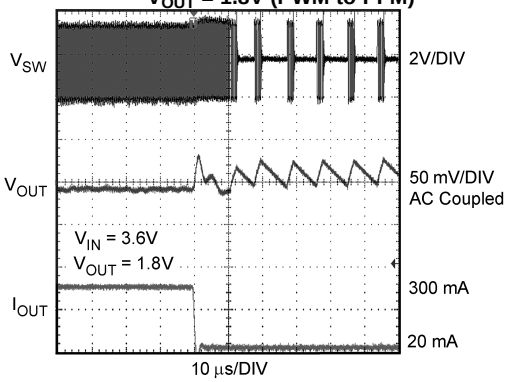


Figure 36.

Load Transient Response
V_{OUT} = 1.3V (PWM Mode)

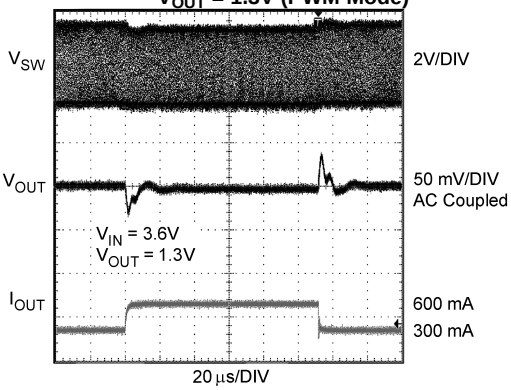


Figure 37.

Load Transient Response
V_{OUT} = 1.8V (PWM Mode)

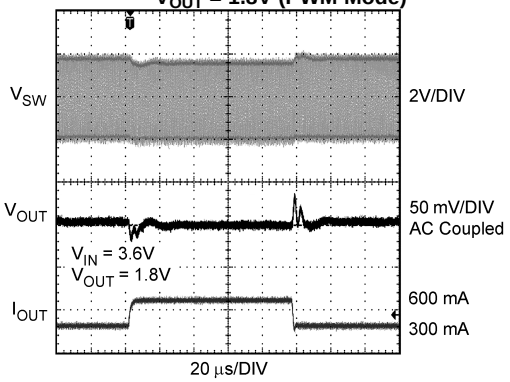


Figure 38.

Load Transient Response
V_{OUT} = 2.5V (PWM Mode)

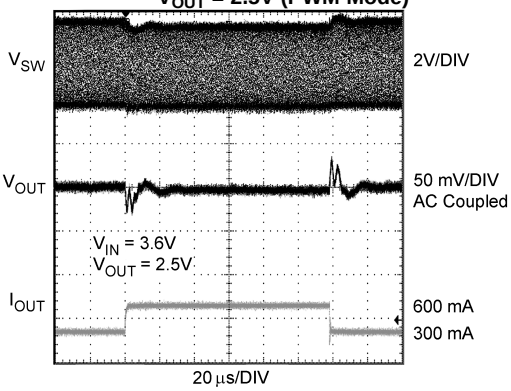


Figure 39.

Start Up into PWM Mode
V_{OUT} = 1.3V (Output Current= 300mA)

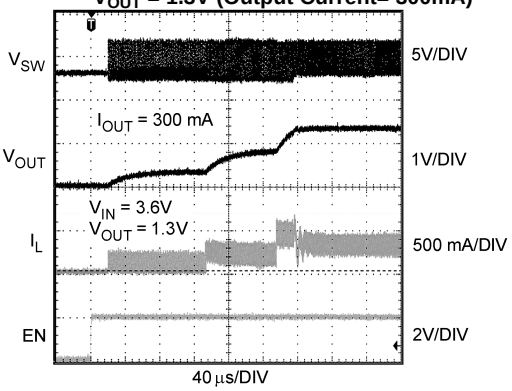


Figure 40.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM3677, Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

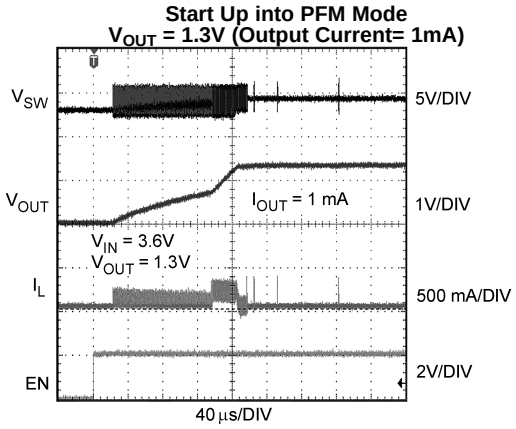


Figure 41.

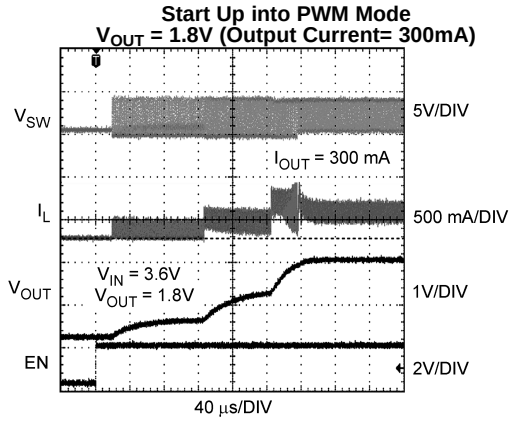


Figure 42.

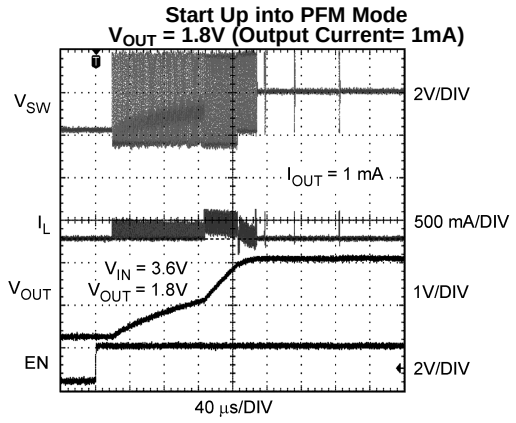


Figure 43.

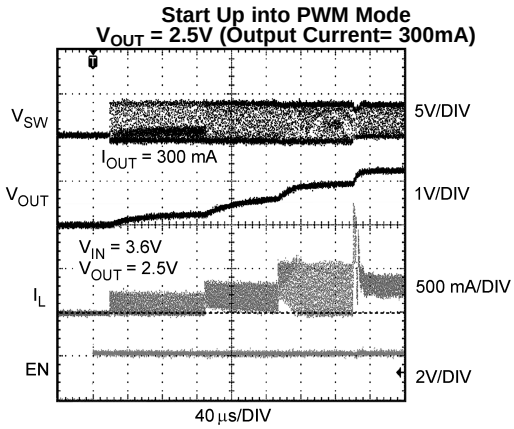


Figure 44.

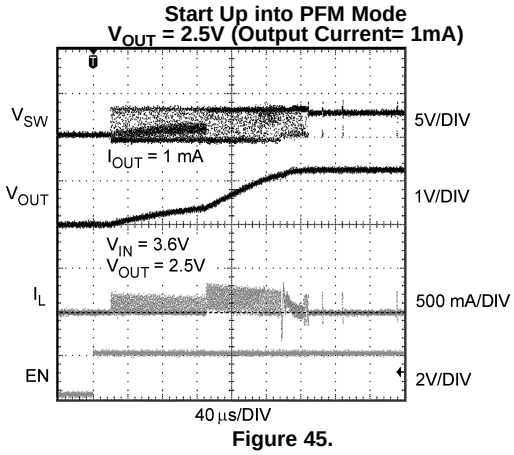


Figure 45.

OPERATION DESCRIPTION

DEVICE INFORMATION

The LM3677, a high-efficiency step-down DC-DC switching buck converter, delivers a constant voltage from a single Li-Ion battery and input voltage rails from 2.7V to 5.5V to devices such as cell phones and PDAs. Using a voltage-mode architecture with synchronous rectification, the LM3677 has the ability to deliver up to 600 mA depending on the input voltage and output voltage, ambient temperature, and the inductor chosen.

There are three modes of operation depending on the current required: PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation), and shutdown. The device operates in PWM mode at load current of approximately 80 mA or higher, having a voltage precision of ±2.5% with 90% efficiency or better. Lighter load current causes the device to automatically switch into PFM mode for reduced current consumption (I_Q = 16 µA typ.) and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.01 µA (typ.).

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in Figure 1, only three external power components are required for implementation.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage exceeds 2.7V.

CIRCUIT OPERATION

The LM3677 operates as follows. During the first portion of each switching cycle, the control block in the LM3677 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN}–V_{OUT})/L, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of - V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch-on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation, the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

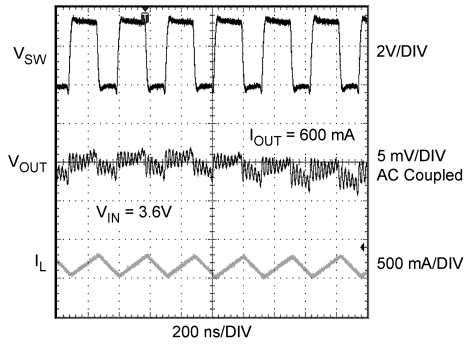


Figure 46. Typical PWM Operation

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the LM3677 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows the LM3677 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1220 mA (typ.). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of the following conditions occurs for a duration of 32 or more clock cycles:

A. The NFET current reaches zero.

B. The peak PMOS switch current drops below the I_{MODE} level, (Typically I_{MODE} < 75 mA + V_{IN}/55Ω).

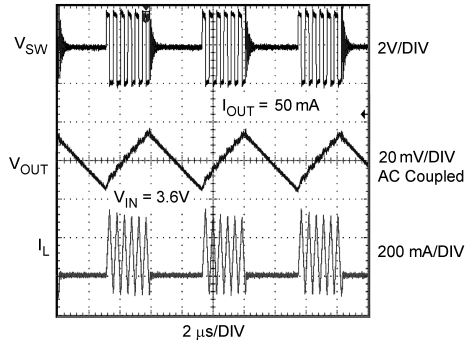


Figure 47. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.2% and ~1.8% above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112 mA + V_{IN}/20Ω .

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 48), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero, and then both output switches are turned off and the part enters an extremely low-power mode. Quiescent supply current during this 'sleep' mode is 16 µA (typ.), which allows the part to achieve high efficiencies under extremely light load conditions.

If the load current should increase during PFM mode (Figure 48) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode. When V_{IN} =2.7V the part transitions from PWM to PFM mode at ~ 35 mA output current and from PFM to PWM mode at ~ 95 mA , when V_{IN}=3.6V, PWM to PFM transition occurs at ~ 42 mA and PFM to PWM transition occurs at ~ 115 mA, when V_{IN} =4.5V, PWM to PFM transition occurs at ~ 60 mA and PFM to PWM transition occurs at ~ 135 mA.

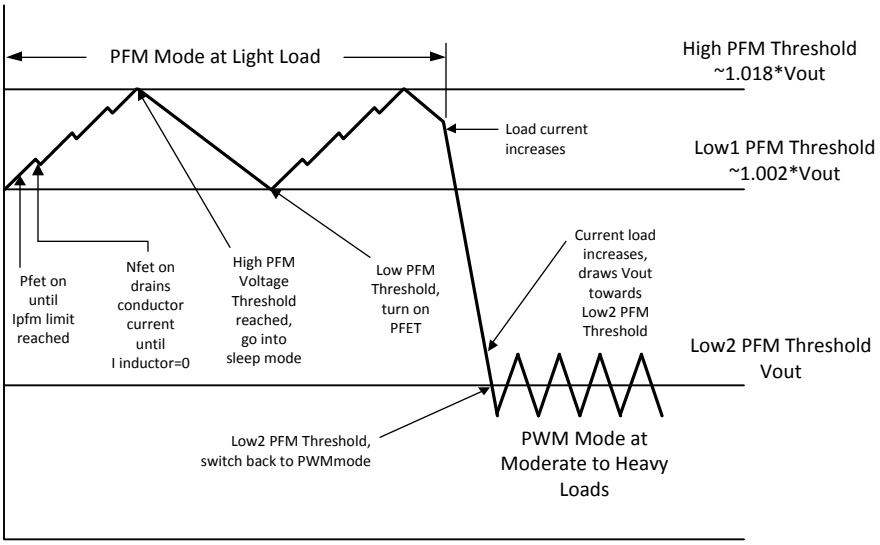


Figure 48. Operation in PFM Mode and Transfer to PWM Mode

SHUTDOWN MODE

Setting the EN input pin low (<0.4V) places the LM3677 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM3677 are turned off. Setting EN high (>1.0V) enables normal operation. It is recommended to set EN pin low to turn off the LM3677 during system power up and undervoltage conditions when the supply is less than 2.7V. Do not leave the EN pin floating.

SOFT START

The LM3677 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 200 mA, 400 mA, 600 mA and 1220 mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with a 10 µF output capacitor and 300 mA load is 300 µs and with 1 mA load is 200 µs.

APPLICATION INFORMATION

INDUCTOR SELECTION

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested form the manufacturer. **The minimum value of inductance to ensure good performance is 0.7 µH at I_{LIM} (typ.) DC current over the ambient temperature range.** Shielded inductors radiate less noise and should be preferred.

There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \quad (1)$$

- I_{RIPPLE}: average to peak inductor current
- I_{OUTMAX}: maximum load current (600 mA)
- V_{IN}: maximum input voltage in application
- L : min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f : minimum switching frequency (2.5 MHz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the max current limit of 1375 mA.

A 1.0 µH inductor with a saturation current rating of at least 1375 mA is recommended for most applications. The inductor's resistance should be less than 0.15Ω for good efficiency. Table 1 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor in the event that noise from low-cost bobbin models is unacceptable.

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 4.7 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0603 and 0805. **The minimum input capacitance to ensure good performance is 2.2 µF at 3V DC bias; 1.5 µF at 5V DC bias including tolerances and over ambient temperature range.** The input filter capacitor supplies current to the PFET switch of the LM3677 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

$$\text{The worst case is when } V_{IN} = 2 * V_{OUT} \quad (2)$$

Table 1. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH(mm)	D.C.R (max)
MIPSA2520D 1R0	FDK	2.5 x 2.0 x 1.2	100 mΩ
LQM2HP 1R0	Murata	2.5 x 2.0 x 0.95	100 mΩ
BRL2518T1R0M	Taiyo Yuden	2.5x 1.8 x 1.2	80 mΩ

OUTPUT CAPACITOR SELECTION

A ceramic output capacitor of 10 µF, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0603 and 0805. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The minimum output capacitance to ensure good performance is 5.75 µF at 2.5V DC bias including tolerances and over ambient temperature range. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follows

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4*f*C} \tag{3}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows

$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR}$

Because these two components are out of phase the rms (root mean squared) value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, rms can be expressed as follow:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^{\,2} + V_{PP\text{-}ESR}^{\,2}} \tag{4}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 2. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
4.7 µF for C_{IN}				
C1608X5R0J475	Ceramic, X5R	TDK	6.3V	0603 (1608)
C2012X5R0J475	Ceramic, X5R	TDK	6.3V	0805 (2012)
GRM21BR60J475	Ceramic, X5R	muRata	6.3V	0805 (2012)
JMK212BJ475	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
10 µF for C_{OUT}				
C1608X5R0J106	Ceramic, X5R	TDK	6.3V	0603 (1608)
C2012X5R0J106	Ceramic, X5R	TDK	6.3V	0805 (2012)
GRM21BR60J106	Ceramic, X5R	muRata	6.3V	0805 (2012)
JMK212BJ106	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)

OUTPUT VOLTAGE SELECTION FOR LM3677-ADJ

The output voltage of the adjustable parts can be programmed through the resistor network connected from V_{OUT} to FB to GND. The resistor and FB to GND (R_2) should be 200 kΩ to keep the current drawn through this network well below 16 µA quiescent current level (PFM mode) but large enough that it is not susceptible to noise. If R_2 is 200 kΩ, and given the V_{FB} is 0.5V, then the current through the resistor feedback network will be 2.5 µA. The output voltage of the adjustable parts ranges from 1.2V and 3.3V. The output voltage formula is:

$$V_{OUT} = V_{FB}\left[\frac{R_1}{R_2} + 1\right]$$

V_{OUT}: output voltage (V)

V_{FB}: feedback voltage (0.5V typical)

R_1: feedback resistor from V_{OUT} to FB (Ω)

R_2: feedback resistor from to FB to GND (Ω)

For the fixed output voltage parts the feedback resistors are internal and R_1 is 0Ω.

The bypass capacitors C_1 and C_2 (labeled C3 and C4 on Evaluation Board) in parallel with the feedback resistors are chosen for increased stability. Below are the formulas for C_1 and C_2:

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times 70\ kHz}$$

$$C_2 = \frac{1}{2 \times \pi \times R_2 \times 70\ kHz}$$

Table 3. LM3677–ADJ Configurations for Various V_{OUT} (Circuit of Figure 2)

V_{OUT} (V)	R_1(kΩ)	R_2(kΩ)	C_1(pF)	C_2(pF)	L (µH)	C_{IN} (µF)	C_{OUT} (µF)
1.2	280	200	8.2	none	1.0	4.7	10
1.3	320	200	8.2	none	1.0	4.7	10
1.5	357	178	6.8	none	1.0	4.7	10
1.6	442	200	5.6	none	1.0	4.7	10
1.8	464	178	5.6	none	1.0	4.7	10
2.5	402	100	6.0	none	1.0	4.7	10
2.8	464	100	5.6	24	1.0	4.7	10
3.3	562	100	5.6	24	1.0	4.7	10

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Application Report 1112, DSBGA Wafer Level Chip Scale Package (SNVA009). Refer to the section "*Surface Mount Technology (SMD) Assembly Considerations*". For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined typ.). This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 for specific instructions how to do this. The 5-bump package used for LM3677 has 300–micron solder balls and requires 10.82 mils pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7 mil wide, for a section approximately 7 mil long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criteria is symmetry. This ensures the solder bumps on the LM3677 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1 and A3, because GND and V_{IN} are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance.

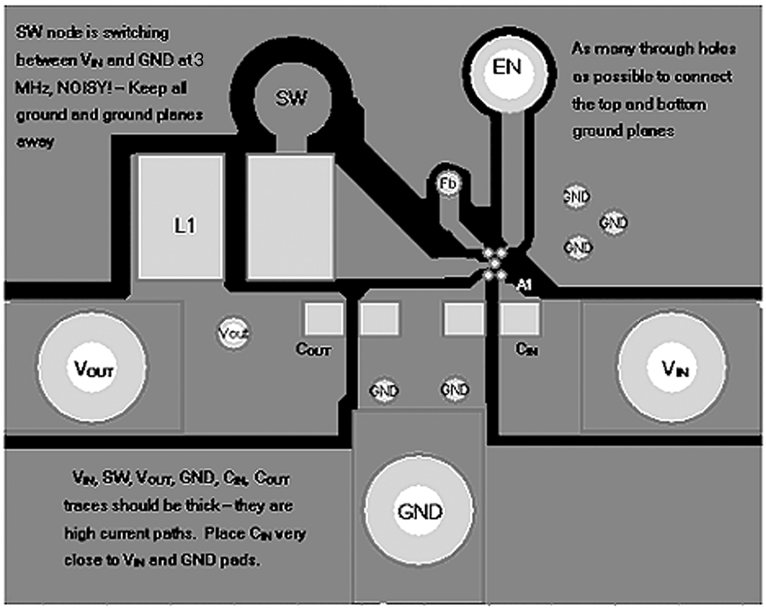


Figure 49. Board Layout Design Rules for the LM3677

Good layout for the LM3677 can be implemented by following a few simple design rules.

- Place the LM3677 on 10.82 mil pads. As a thermal relief, connect to each pad with a 7 mil wide, approximately 7 mil long trace, and then incrementally increase each trace to its optimal width. The important criterion is symmetry to ensure the solder bumps on the re-flow evenly (see *DSBGA Package Assembly and Use*).
- Place the LM3677, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM3677 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3677 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Connect the ground pins of the LM3677, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3677 by giving it a low-impedance ground connection.
- Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces

- Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3677 circuit and should be routed directly from FB to V_{OUT} at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
- Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3677LEE-1.2/NOPB	ACTIVE	USON	NGE	6	250	RoHS & Green	SN	Level-1-260C-UNLIM		K	Samples
LM3677LEE-1.5/NOPB	ACTIVE	USON	NGE	6	250	RoHS & Green	SN	Level-1-260C-UNLIM		L	Samples
LM3677LEE-1.8/NOPB	ACTIVE	USON	NGE	6	250	RoHS & Green	SN	Level-1-260C-UNLIM		N	Samples
LM3677TL-1.2/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		3	Samples
LM3677TL-1.8/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	Y	Samples
LM3677TL-2.5/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	Z	Samples
LM3677TL-ADJ/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		4	Samples
LM3677TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

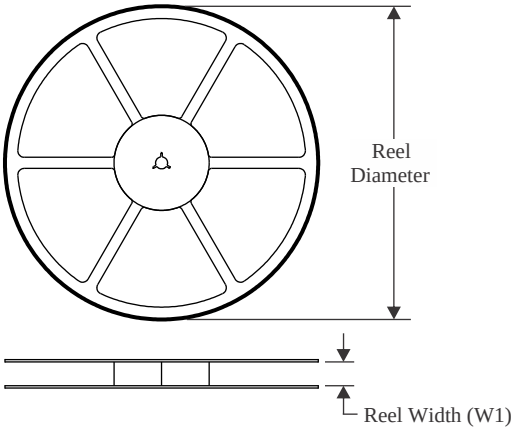
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

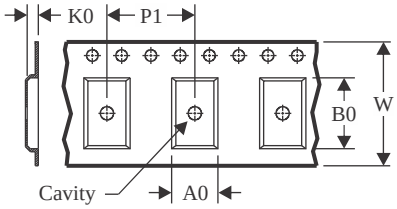
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

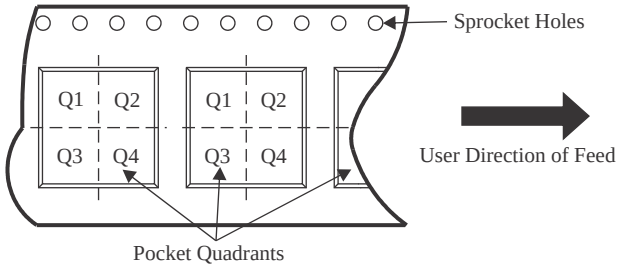


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

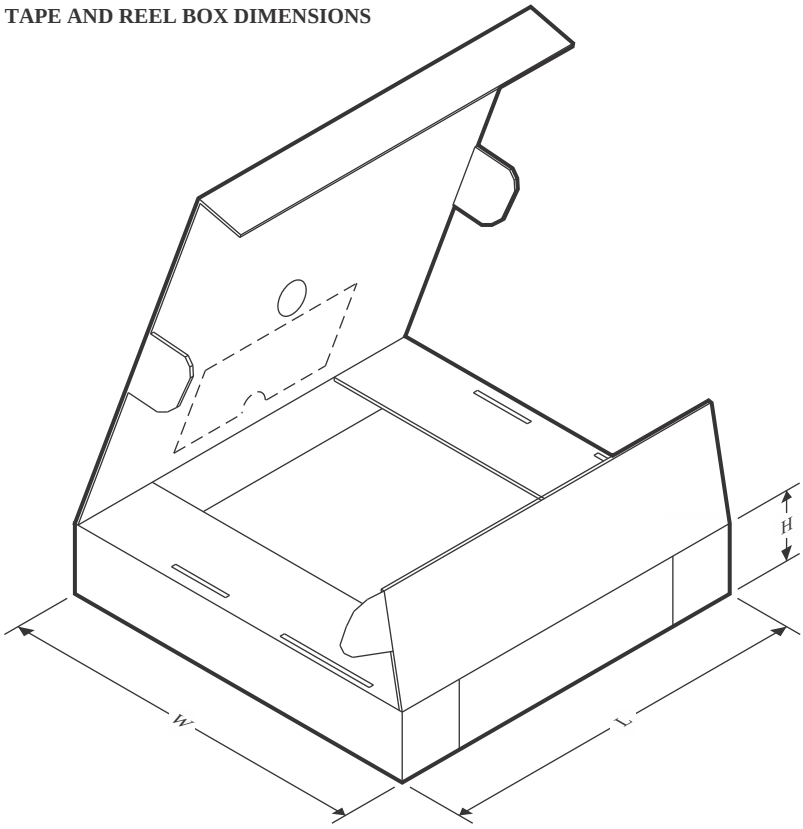
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3677LEE-1.2/NOPB	USON	NGE	6	250	178.0	12.4	1.7	2.2	0.8	8.0	12.0	Q1
LM3677LEE-1.5/NOPB	USON	NGE	6	250	178.0	12.4	1.7	2.2	0.8	8.0	12.0	Q1
LM3677LEE-1.8/NOPB	USON	NGE	6	250	178.0	12.4	1.7	2.2	0.8	8.0	12.0	Q1
LM3677TL-1.2/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LM3677TL-1.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LM3677TL-2.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LM3677TL-ADJ/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LM3677TLX-1.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1

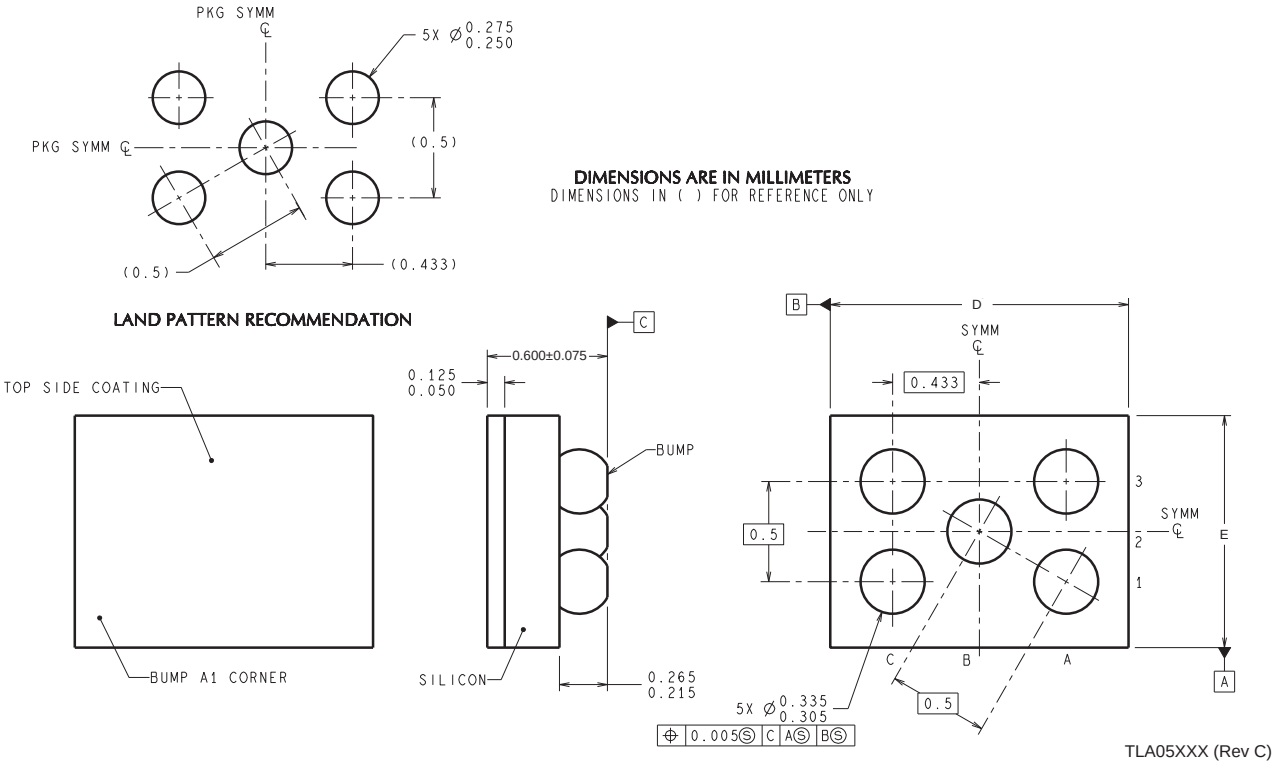
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3677LEE-1.2/NOPB	USON	NGE	6	250	208.0	191.0	35.0
LM3677LEE-1.5/NOPB	USON	NGE	6	250	208.0	191.0	35.0
LM3677LEE-1.8/NOPB	USON	NGE	6	250	208.0	191.0	35.0
LM3677TL-1.2/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LM3677TL-1.8/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LM3677TL-2.5/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LM3677TL-ADJ/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LM3677TLX-1.8/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0

YZR0005



D: Max = 1.514 mm, Min =1.454 mm

E: Max = 1.133 mm, Min =1.073 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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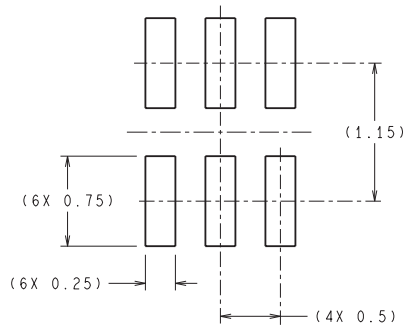
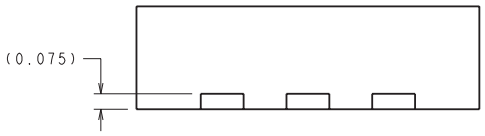
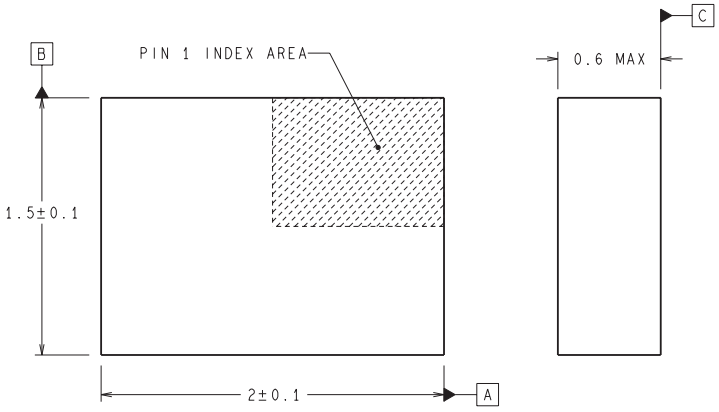


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY





LEB06A (Rev B)

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