# LM2665 Switched Capacitor Voltage Converter

## 1 Features

- Input Voltage for Voltage Doubler: 2.5 V to 5.5 V
- Voltage Divider Splits Voltage: 1.8 V to 11 V
- Doubles or Splits Input Supply Voltage
- 12-Ω Typical Output Impedance
- 90% Typical Conversion Efficiency at 40 mA
- 1-µA Typical Shutdown Current

## 2 Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments
- Fire Detection and Notification
- Industrial Handheld Radios
- Blood Pressure Monitors

## 3 Description

The LM2665 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 2.5 V to 5.5 V. Two low-cost capacitors and a diode (needed during start-up) are used in this circuit to provide up to 40 mA of output current. The LM2665 can also work as a voltage divider to split a voltage in the range of 1.8 V to 11 V in half.

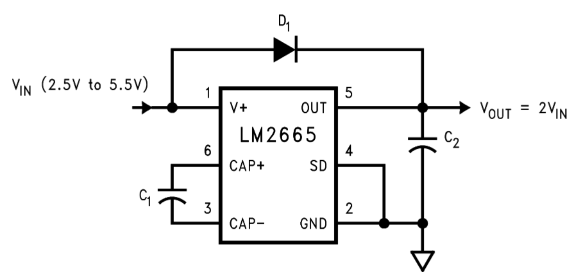
The LM2665 operates at 160-kHz oscillator frequency to reduce output resistance and voltage ripple. With an operating current of only 650 µA (operating efficiency greater than 90% with most loads) and 1-µA typical shutdown current, the LM2665 provides ideal performance for battery powered systems.

**Device Information(1)**

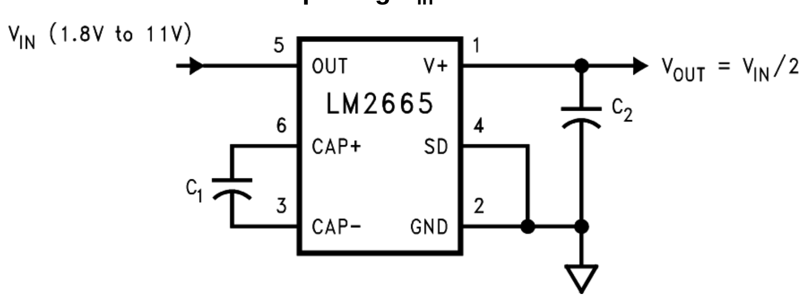
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LM2665 | SOT-23 (6) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Voltage Doubler**




**Splitting $V_{in}$ in Half**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision G (July 2015) to Revision H** **Page**

- Added several new "Applications" to page 1 ........ 1

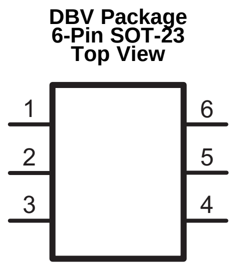
**Changes from Revision F (May 2013) to Revision G** **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* , *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ........ 1

**Changes from Revision E (May 2013) to Revision F** **Page**

- Changed layout of National Data Sheet to TI format ........ 12

# 5 Pin Configuration and Functions




**Pin Functions**

| PIN | | TYPE | DESCRIPTION | |
|---|---|---|---|---|
| NO. | NAME | | VOLTAGE DOUBLER | VOLTAGE SPLIT |
| 1 | V+ | Power | Power supply positive voltage input | Positive voltage output |
| 2 | GND | Ground | Power supply ground input | Same as doubler |
| 3 | CAP− | Power | Connect this pin to the negative terminal of the charge-pump capacitor. | Same as doubler |
| 4 | SD | Input | Shutdown control pin, tie this pin to ground in normal operation. | Same as doubler |
| 5 | OUT | Power | Positive voltage output | Power supply positive voltage input |
| 6 | CAP+ | Power | Connect this pin to the positive terminal of the charge-pump capacitor. | Same as doubler |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

| | MIN | MAX | UNIT |
|---|---|---|---|
| V+ to GND voltage | | 5.8 | V |
| OUT to GND voltage | | 11.6 | V |
| OUT to V+ voltage | | 5.8 | V |
| SD | (GND − 0.3 V) | (V+ + 0.3 V) | |
| V+ and OUT continuous output current | | 50 | mA |
| Output short-circuit duration to GND[3] | | 1 | sec |
| Continuous power dissipation ($T_A$ = 25°C)[4] | | 600 | mW |
| $T_{J\text{-}MAX}$[4] | | 150 | °C |
| Lead temperature (soldering, 10 sec.) | | 300 | °C |
| Storage temperature, $T_{stg}$ | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and must be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{D\text{-}MAX} = (T_{J\text{-}MAX} - T_A)/R_{\theta JA}$, where $T_{J\text{-}MAX}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Operating junction temperature | –40 | | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | LM2665 DBV (SOT-23) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 210 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

MIN and MAX limits apply over the full operating temperature range. Unless otherwise specified: $T_J$ = 25°C, V+ = 5 V, $C_1 = C_2$ = 3.3 µF.(1)

| PARAMETER | | TEST CONDITIONS | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|
| V+ | Supply voltage | | 2.5 | | 5.5 | V |
| $I_Q$ | Supply current | No load | | 650 | 1250 | µA |
| $I_{SD}$ | Shutdown supply current | | | 1 | | µA |
| $V_{SD}$ | Shutdown pin input voltage | Normal operation | 2(4) | | | V |
| | | Shutdown mode | | | 0.8(5) | |
| $I_L$ | Output current | | 40 | | | mA |
| $R_{SW}$ | Sum of the $R_{ds(on)}$ of the four internal MOSFET switches | $I_L$ = 40 mA | | 3.5 | 8 | Ω |
| $R_{OUT}$ | Output resistance(6) | $I_L$ = 40 mA | | 12 | 25 | Ω |
| $f_{OSC}$ | Oscillator frequency | See(7) | 80 | 160 | | kHz |
| $f_{SW}$ | Switching frequency | See(7) | 40 | 80 | | kHz |
| $P_{EFF}$ | Power efficiency | $R_L$ (1 kΩ) between GND and OUT | 90% | 94% | | |
| | | $I_L$ = 40 mA to GND | | 90% | | |
| $V_{OEFF}$ | Voltage conversion efficiency | No load | 99% | 99.96% | | |

(1) In the test circuit, capacitors $C_1$ and $C_2$ are 3.3-µF, 0.3-Ω maximum ESR capacitors. Capacitors with higher ESR increase output resistance, reduce output voltage and efficiency.
(2) Min. and Max. limits are ensured by design, test, or statistical analysis.
(3) Typical numbers are not ensured but represent the most likely norm.
(4) The minimum input high for the SD pin equals 40% of V+.
(5) The maximum input low for the SD pin equals 20% of V+.
(6) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in *Application and Implementation* for simple negative voltage converter.
(7) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

## 6.6 Typical Characteristics

(Circuit of Figure 9, V+ = 5 V unless otherwise specified)

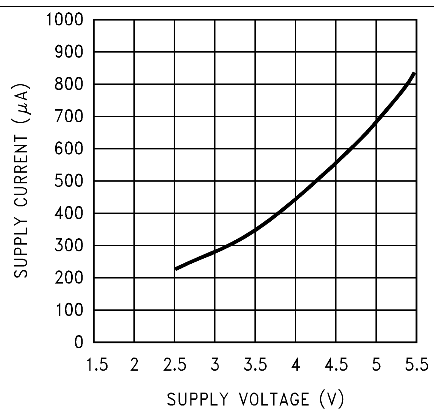



**Figure 1. Supply Current vs Supply Voltage**

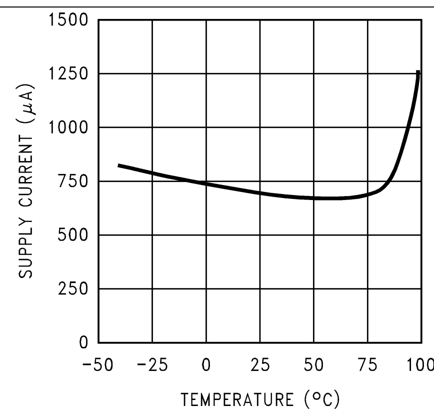



**Figure 2. Supply Current vs Temperature**

## Typical Characteristics (continued)

(Circuit of Figure 9, V+ = 5 V unless otherwise specified)

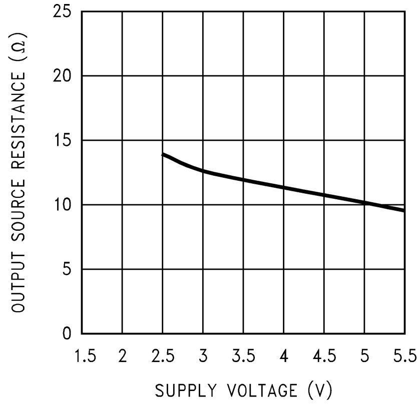



**Figure 3. Output Source Resistance vs Supply Voltage**

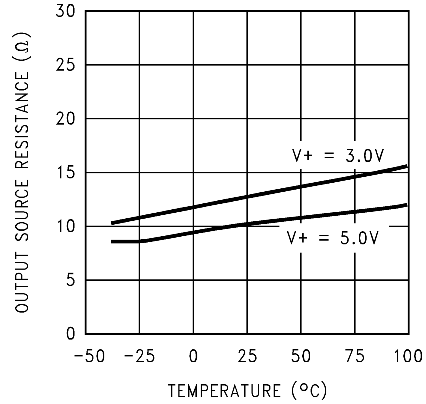



**Figure 4. Output Source Resistance vs Temperature**

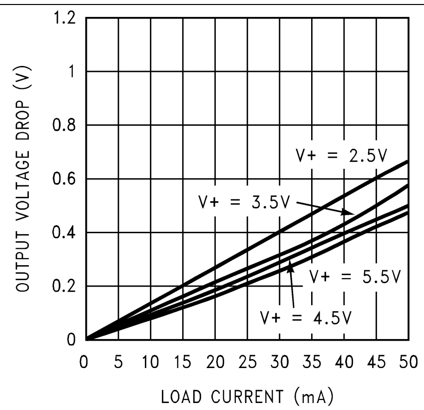



**Figure 5. Output Voltage Drop vs Load Current**

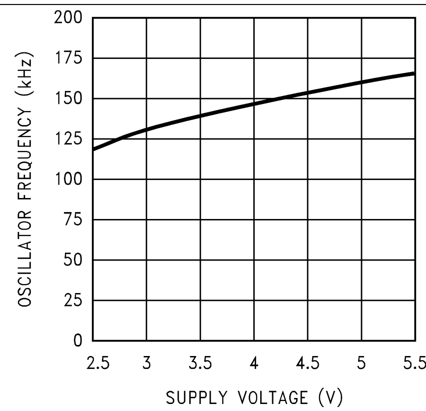



**Figure 6. Oscillator Frequency vs Supply Voltage**

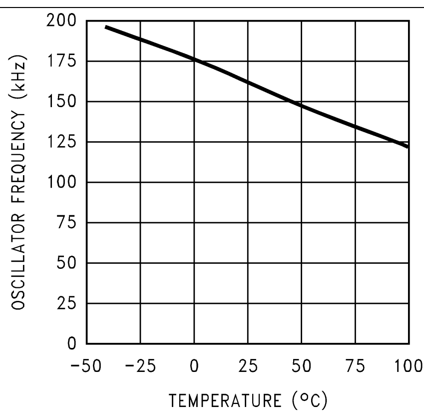



**Figure 7. Oscillator Frequency vs Temperature**

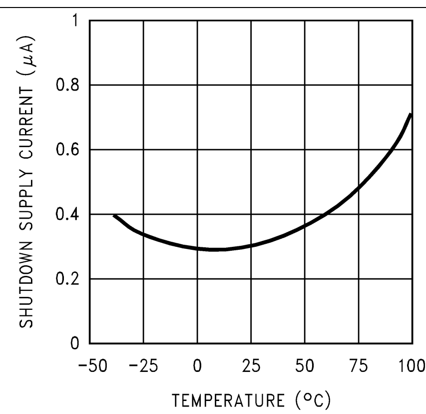
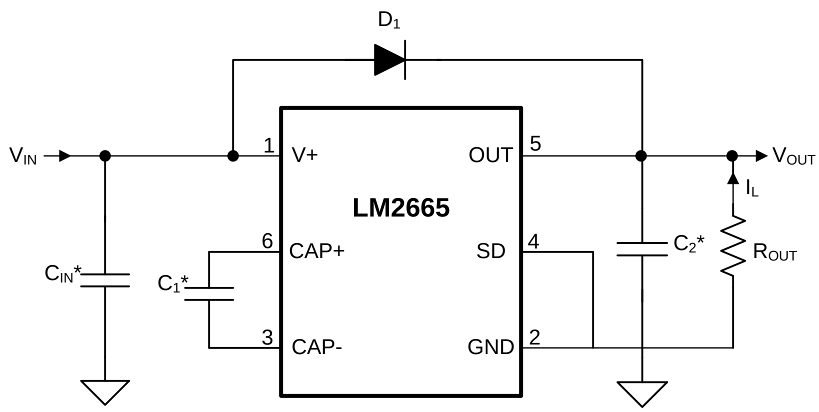



**Figure 8. Shutdown Supply Current vs Temperature**

# 7 Parameter Measurement Information

## 7.1 Test Circuit




*$C_{IN}$, $C_1$ and $C_2$ are 3.3 µF OS-CON capacitors.

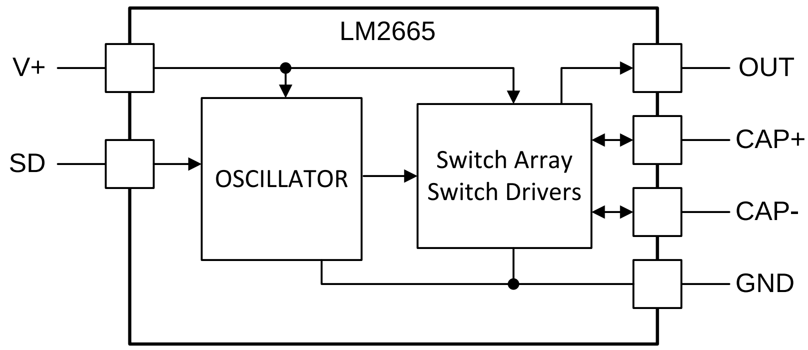
**Figure 9. LM2665 Test Circuit**

# 8 Detailed Description

## 8.1 Overview

The LM2665 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 2.5 V to 5.5 V. Two low-cost capacitors and a diode (needed during start-up) are used in this circuit to provide up to 40 mA of output current. The LM2665 can also work as a voltage divider to split a voltage in the range of 1.8 V to 11 V in half.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Circuit Description

The LM2665 contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 10 illustrates the voltage conversion scheme. When $S_2$ and $S_4$ are closed, $C_1$ charges to the supply voltage V+. During this time interval, switches $S_1$ and $S_3$ are open. In the next time interval, $S_2$ and $S_4$ are open; at the same time, $S_1$ and $S_3$ are closed, the sum of the input voltage V+ and the voltage across $C_1$ gives the 2-V+ output voltage when there is no load. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{DS(on)}$ of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. Details are discussed in *Application and Implementation*.

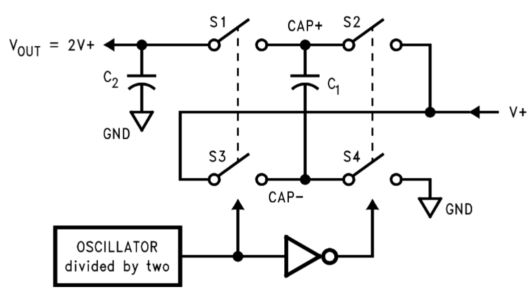



**Figure 10. Voltage Doubling Principle**

## 8.4 Device Functional Modes

### 8.4.1 Shutdown Mode

A shutdown (SD) pin is available to disable the device and reduce the quiescent current to 1 µA. In normal operating mode, the SD pin is connected to ground. The device can be brought into the shutdown mode by applying to the SD pin a voltage greater than 40% of the V+ pin voltage.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The LM2665 provides a simple and efficient means of creating an output voltage level equal to twice that of the input voltage. Without the need of an inductor, the application solution size can be reduced versus the magnetic DC-DC converter solution.

## 9.2 Typical Applications

### 9.2.1 Voltage Doubler

The main application of the LM2665 is to double the input voltage. The range of the input supply voltage is 2.5 V to 5.5 V.

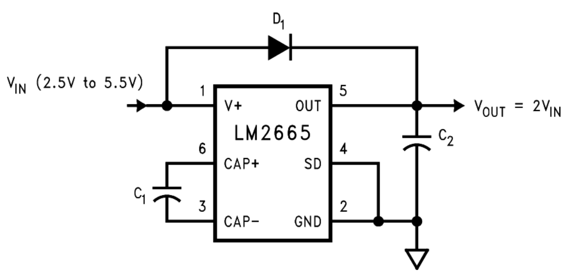



**Figure 11. Voltage Doubler**

#### *9.2.1.1 Design Requirements*

Example requirements for LM2665 device applications:

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 2.5 V to 5.5 V |
| Output current | 0 mA to 40 mA |
| Boost switching frequency | 80 kHz |

### 9.2.1.2 Detailed Design Requirements

#### 9.2.1.2.1 Positive Voltage Doubler

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals 2 V+. The output resistance $R_{OUT}$ is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance and equivalent series resistance (ESR) of $C_1$ and $C_2$. Since the switching current charging and discharging $C_1$ is approximately twice as the output current, the effect of the ESR of the pumping capacitor $C_1$ will be multiplied by four in the output resistance. The output capacitor $C_2$ is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts when in the output resistance. A good approximation of $R_{OUT}$ is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2}$$

where

- $R_{SW}$ is the sum of the ON resistance of the internal MOSFET switches shown in Figure 10. (1)

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the output capacitor $C_2$:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

High capacitance, low-ESR capacitors can reduce both the output resistance and the voltage ripple.

The Schottky diode $D_1$ is only needed for start-up. The internal oscillator circuit uses the OUT pin and the GND pin. Voltage across OUT and GND must be larger than 1.8 V to insure the operation of the oscillator. During start-up, $D_1$ is used to charge up the voltage at the OUT pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode $D_1$ must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

#### 9.2.1.2.2 Capacitor Selection

As discussed in *Positive Voltage Doubler*, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{{I_L}^2 R_L}{{I_L}^2 R_L + {I_L}^2 R_{OUT} + I_Q(V+)}$$

where

- $I_Q(V+)$ is the quiescent power loss of the IC device; and
- ${I_L}^2R_{out}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs. (3)

The selection of capacitors is based on the specifications of the dropout voltage (which equals $I_{OUT}$ $R_{OUT}$), the output voltage ripple, and the converter efficiency. Low ESR capacitors are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

#### 9.2.1.2.3 Paralleling Devices

Any number of LM2665 devices can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor $C_1$, while only one output capacitor $C_{OUT}$ is needed as shown in Figure 12. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT}\ of\ each\ LM2665}{Number\ of\ Devices} \quad (4)$$

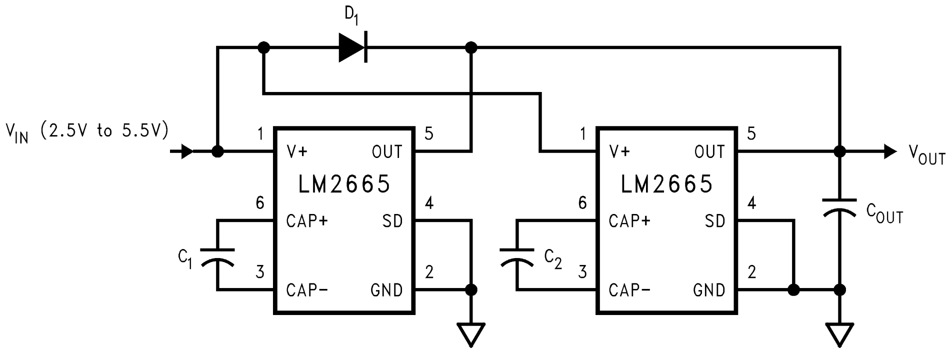



**Figure 12. Lowering Output Resistance By Paralleling Devices**

#### 9.2.1.2.4 Cascading Devices

Cascading the LM2665 devices is an easy way to produce a greater voltage (a two-stage cascade circuit is shown in Figure 13).

The effective output resistance is equal to the weighted sum of each individual device:

$$R_{OUT} = 1.5\ R_{OUT\_1} + R_{OUT\_2} \tag{5}$$

Note that the increasing of the number of cascading stages is pracitically limited since it significantly reduces the efficiency, increases the output resistance and output voltage ripple.

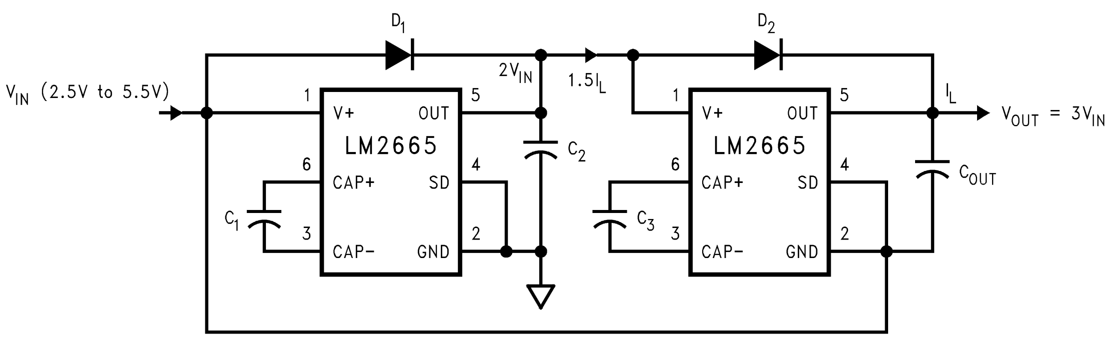



**Figure 13. Increasing Output Voltage By Cascading Devices**

#### 9.2.1.2.5 Regulating $V_{OUT}$

It is possible to regulate the output of the LM2665 by use of a low dropout regulator (such as LP2980-5.0). The whole converter is depicted in Figure 14.

A different output voltage is possible by use of LP2980-3.3, LP2980-3.0, or LP2980-ADJ.

Note that the following conditions must be satisfied simultaneously for worst-case design:

$$2V_{IN\_MIN} > V_{OUT\_MIN} + V_{DROP\_MAX}\ (LP2980) + I_{OUT\_MAX} \times R_{OUT\_MAX}\ \text{(LM2665)} \tag{6}$$

$$2V_{IN\_MAX} < V_{OUT\_MAX} + V_{DROP\_MIN}\ (LP2980) + I_{OUT\_MIN} \times R_{OUT\_MIN}\ \text{(LM2665)} \tag{7}$$

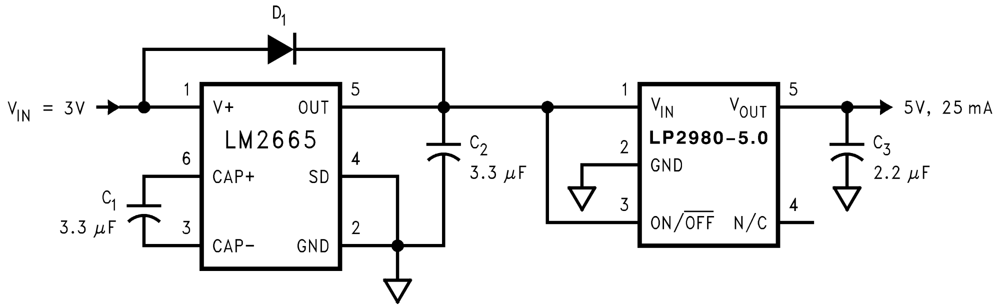



**Figure 14. Generate a Regulated 5-V from 3-V Input Voltage**

#### 9.2.1.3 Application Curve

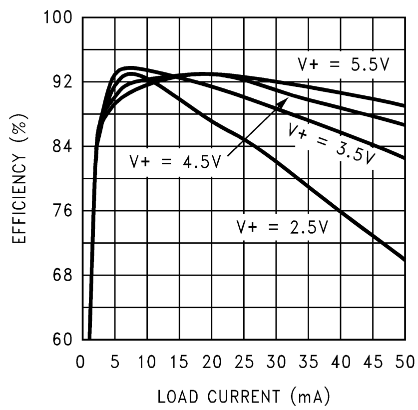



**Figure 15. Efficiency vs Load Current**

### 9.2.2 Splitting V+ In Half

Another interesting application shown in *Splitting $V_{in}$ in Half* is using the LM2665 as a precision voltage divider. This circuit can be derived from the voltage doubler by switching the input and output connections. In the voltage divider, the input voltage applies across the OUT pin and the GND pin (which are the power rails for the internal oscillator), therefore no start-up diode is needed. Also, since the off-voltage across each switch equals $V_{IN}/2$, the input voltage can be raised to 11 V.

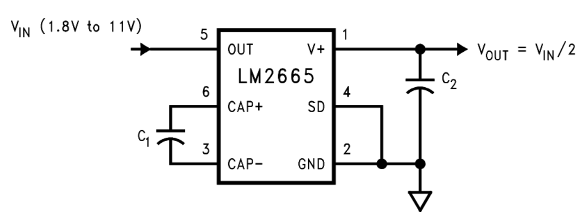



**Figure 16. Application Circuit for Splitting Voltage**

## 10 Power Supply Recommendations

The LM2665 is designed to operate from as an inverter over an input voltage supply range between 2.5 V and 5.5 V when the LV pin is grounded. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

# 11 Layout

## 11.1 Layout Guidelines

The high switching frequency and large switching currents of the LM2665 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

- Place $C_{IN}$ on the top layer (same layer as the LM2665) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the V+ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V+ line.
- Place $C_{OUT}$ on the top layer (same layer as the LM2665) and as close as possible to the OUT and GND pin. The returns for both $C_{IN}$ and $C_{OUT}$ must come together at one point, as close to the GND pin as possible. Connecting $C_{OUT}$ through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the $V_{OUT}$ and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on the top layer (same layer as the LM2665 device) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

## 11.2 Layout Example

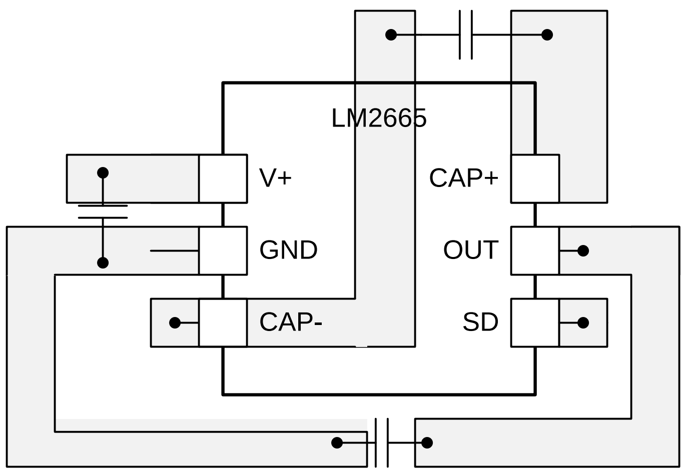



**Figure 17. Typical Layout for LM2665**

# 12 Device and Documentation Support

## 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2665M6 | NRND | SOT-23 | DBV | 6 | 1000 | Non-RoHS & Green | Call TI | Level-1-260C-UNLIM | -40 to 85 | S04A | |
| LM2665M6/NOPB | ACTIVE | SOT-23 | DBV | 6 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | S04A | Samples |
| LM2665M6X | NRND | SOT-23 | DBV | 6 | 3000 | Non-RoHS & Green | Call TI | Level-1-260C-UNLIM | -40 to 85 | S04A | |
| LM2665M6X/NOPB | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | S04A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

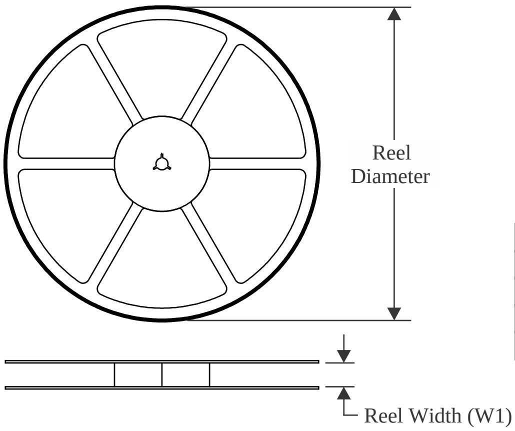
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

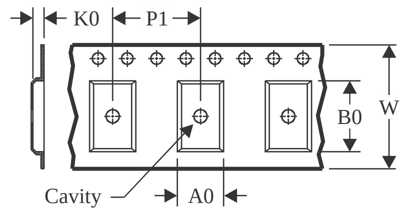
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

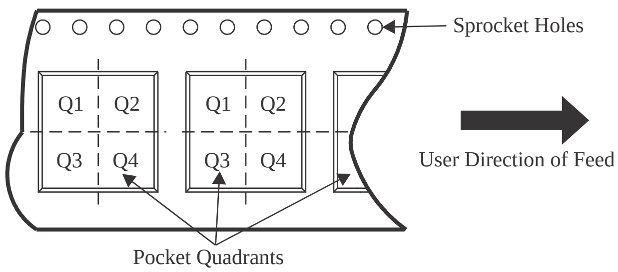



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

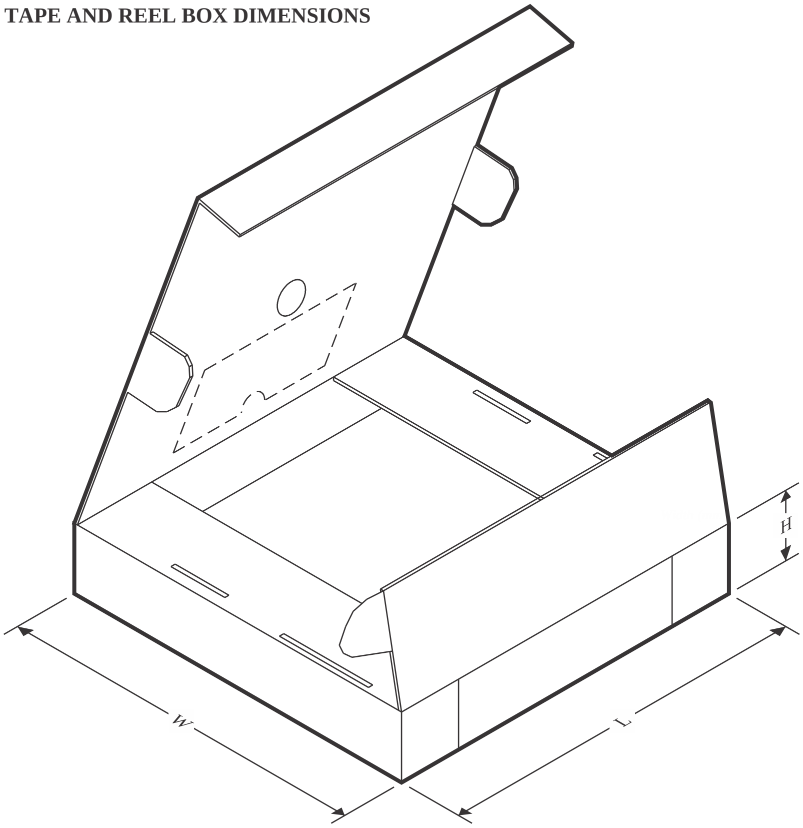
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

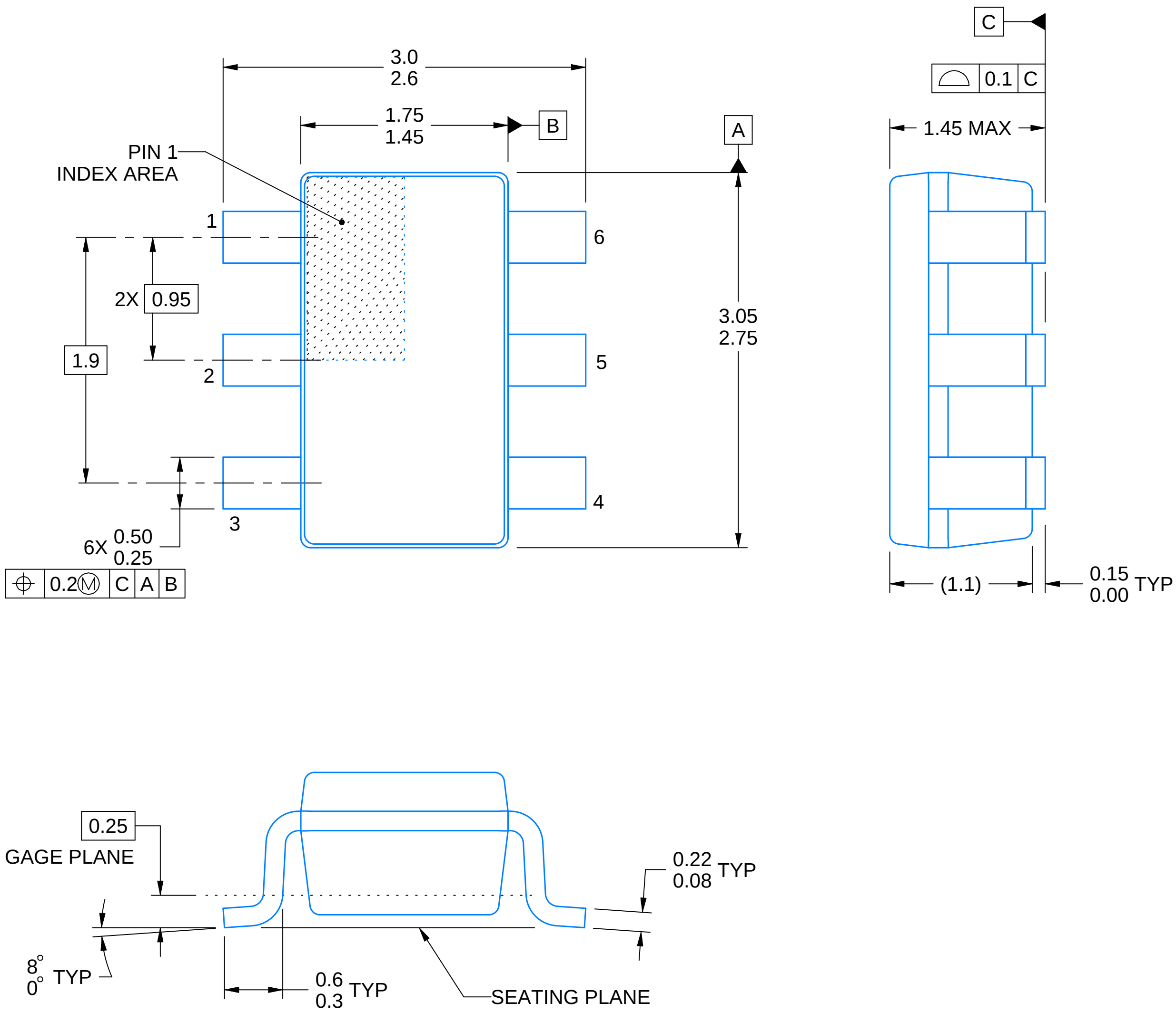
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2665M6 | SOT-23 | DBV | 6 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM2665M6/NOPB | SOT-23 | DBV | 6 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM2665M6X | SOT-23 | DBV | 6 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM2665M6X/NOPB | SOT-23 | DBV | 6 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM2665M6 | SOT-23 | DBV | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LM2665M6/NOPB | SOT-23 | DBV | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LM2665M6X | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| LM2665M6X/NOPB | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |

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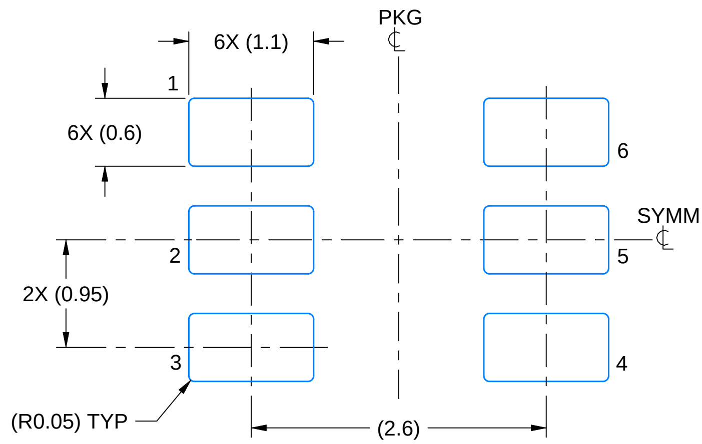
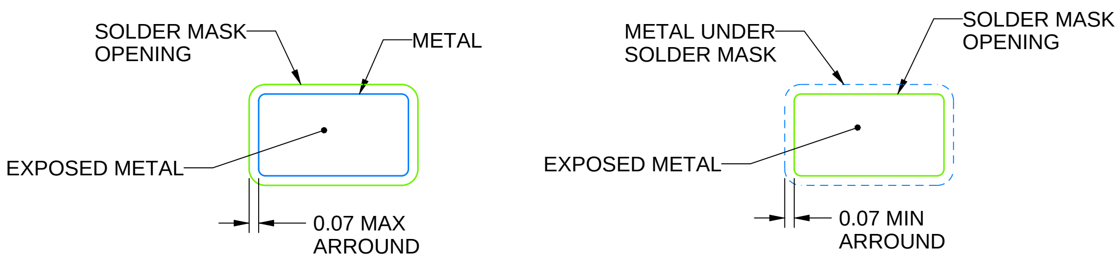
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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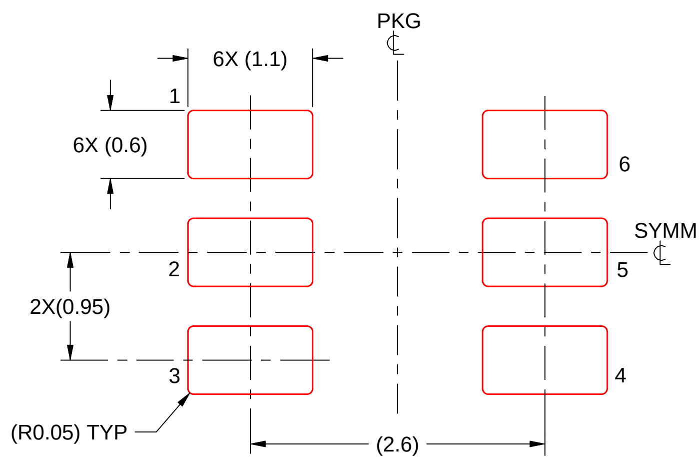
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.