

ADC701
SHC702

16-Bit 512kHz SAMPLING A/D CONVERTER SYSTEM

FEATURES

- **CONVERSION RATE:** to 512kHz Over Temp
- **NO MISSING CODES AT 16 BITS**
- **SPURIOUS-FREE DYNAMIC RANGE:** 107dB
- **LOW NONLINEARITY:** $\pm 0.0015\%$
- **SELECTABLE INPUT RANGES:** $\pm 5V$, $\pm 10V$, 0 to $+10V$, 0 to $+5V$, $-10V$ to 0
- **LOW POWER DISSIPATION:** 2.8W Typical Including Sample/Hold
- **METAL AND CERAMIC DIP PACKAGES**

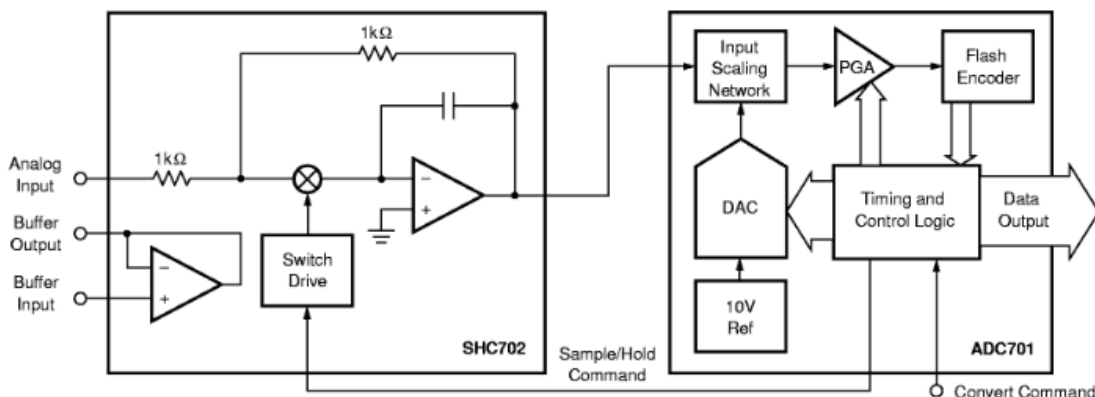
APPLICATIONS

- **MEDICAL IMAGING**
- **SONAR**
- **PROFESSIONAL AUDIO RECORDING**
- **AUTOMATIC TEST EQUIPMENT**
- **HIGH PERFORMANCE FFT SPECTRUM ANALYSIS**
- **ULTRASOUND SIGNAL PROCESSING**
- **HIGH SPEED DATA ACQUISITION**
- **REPLACES DISCRETE MODULAR ADCs**

DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion sample/hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.



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SPECIFICATIONS

ELECTRICAL (ADC701 ONLY)

At $T_A = +25^\circ\text{C}$, 500kHz sampling rate, $\pm V_{CC} = \pm 15\text{V}$, $\pm V_{DD1} = \pm 5\text{V}$, $+V_{DD2} = +5\text{V}$, and five-minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC701JH			ADC701KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
INPUTS								
ANALOG								
Voltage Ranges	Unipolar			0 to +5, 0 to +10, -10 to 0				V
	Bipolar			$\pm 5, \pm 10$				V
Resistance	0 to +5V Range	2.45	2.5	2.55	*	*	*	k Ω
	0 to +10V, -10 to 0, $\pm 5\text{V}$ Ranges	4.9	5	5.1	*	*	*	k Ω
	$\pm 10\text{V}$ Range	9.8	10	10.2	*	*	*	k Ω
Capacitance	All Ranges		5			*		pF
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Convert Command	Start Conversion							
Pulse Width	$t = \text{Conversion Period}$	50		$t - 50$	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error ⁽¹⁾	0 to +10V Range		± 0.03	± 0.1		*	*	%
	$\pm 10\text{V}$ Range		± 0.03	± 0.1		*	*	%
Power Supply Sensitivity of Gain	All Ranges, All Supplies		± 0.005	± 0.1		*	*	%/V
Input Offset Error ⁽¹⁾	0 to +10V Range		± 1	± 3		*	*	mV
	$\pm 10\text{V}$ Range		± 5	± 10		*	*	mV
Power Supply Sensitivity of Offset	All Ranges, All Supplies		± 0.006	± 0.1		*	*	%FSR/V
Integral Linearity Error ⁽²⁾			± 0.002	± 0.003		± 0.0012	*	%FSR ⁽³⁾
Differential Linearity Error ⁽²⁾			± 0.0006	± 0.0012		*	*	%FSR
No Missing Codes			Guaranteed			Guaranteed		
Noise	$R_{\text{SOURCE}} \leq 50\Omega$		0.6			*		LSB rms
CONVERSION CHARACTERISTICS								
Sample Rate	Unadjusted	DC		512	*		*	kHz
Conversion Time ⁽⁴⁾	Unadjusted		1.45	1.5		*	*	μs
OUTPUTS								
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Data Coding	Unipolar Ranges							
	Bipolar Ranges							
Logic "0" Levels (V_{OL})	$I_{OL} \leq 3.2\text{mA}$		0.1	0.4		*	*	V
Logic "1" Levels (V_{OH})	$I_{OH} \leq 80\mu\text{A}$	4	4.9			*	*	V
Data Valid Setup Time Before Strobe	Both Edges	28	37			*	*	ns
INTERNAL REFERENCE								
Voltage	$R_{\text{LOAD}} \geq 5\text{k}\Omega$	+9.995	+10.000	+10.005	*	*	*	V
Current Available to External Loads		2	5		*	*	*	mA
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		-14.25	-15	-15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD1}$		-4.25	-5	-6	*	*	*	V
$+V_{DD2}$		+4.25	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		25	30		*	*	mA
$-I_{CC}$			33	45		*	*	mA
$+I_{DD1}$			45	55		*	*	mA
$-I_{DD1}$			37	50		*	*	mA
$+I_{DD2}$			133	150		*	*	mA
Power Dissipation	Nominal Voltages		1.95	2.3		*	*	W
PERFORMANCE OVER TEMPERATURE								
Specification Temperature Range	T_A Min to T_A Max	+15		+55	0		+70	$^\circ\text{C}$
Gain Error	All Ranges		± 10	± 15		*	*	ppm/ $^\circ\text{C}$
Input Offset Error	All Unipolar Ranges		± 1	± 5		*	*	ppm FSR/ $^\circ\text{C}$
	All Bipolar Ranges		± 1	± 5		*	*	ppm FSR/ $^\circ\text{C}$
Integral Linearity Error ⁽²⁾			± 0.2			*	± 0.5	ppm/ $^\circ\text{C}$
Differential Linearity Error ⁽²⁾			± 0.05			*	± 0.3	ppm/ $^\circ\text{C}$
No Missing Codes			Typical			Guaranteed		
Reference Output Drift			± 3			*	*	ppm/ $^\circ\text{C}$
Drift of Conversion Time	Unadjusted		+3	+4		*	*	ns/ $^\circ\text{C}$
Sample Rate	Unadjusted	DC		512	*		*	kHz

* Same specifications as ADC701JH.