Full Bridge Power Amplifier

FEATURES

- Dual Power Operational Amplifiers
- ±2A Output Current Guaranteed
- Precision Current Sense Amplifier
- Two Supply Monitoring Inputs
- Parking Function and Under-Voltage Lockout
- Safe Operating Area Protection
- 3V to 35V Operation

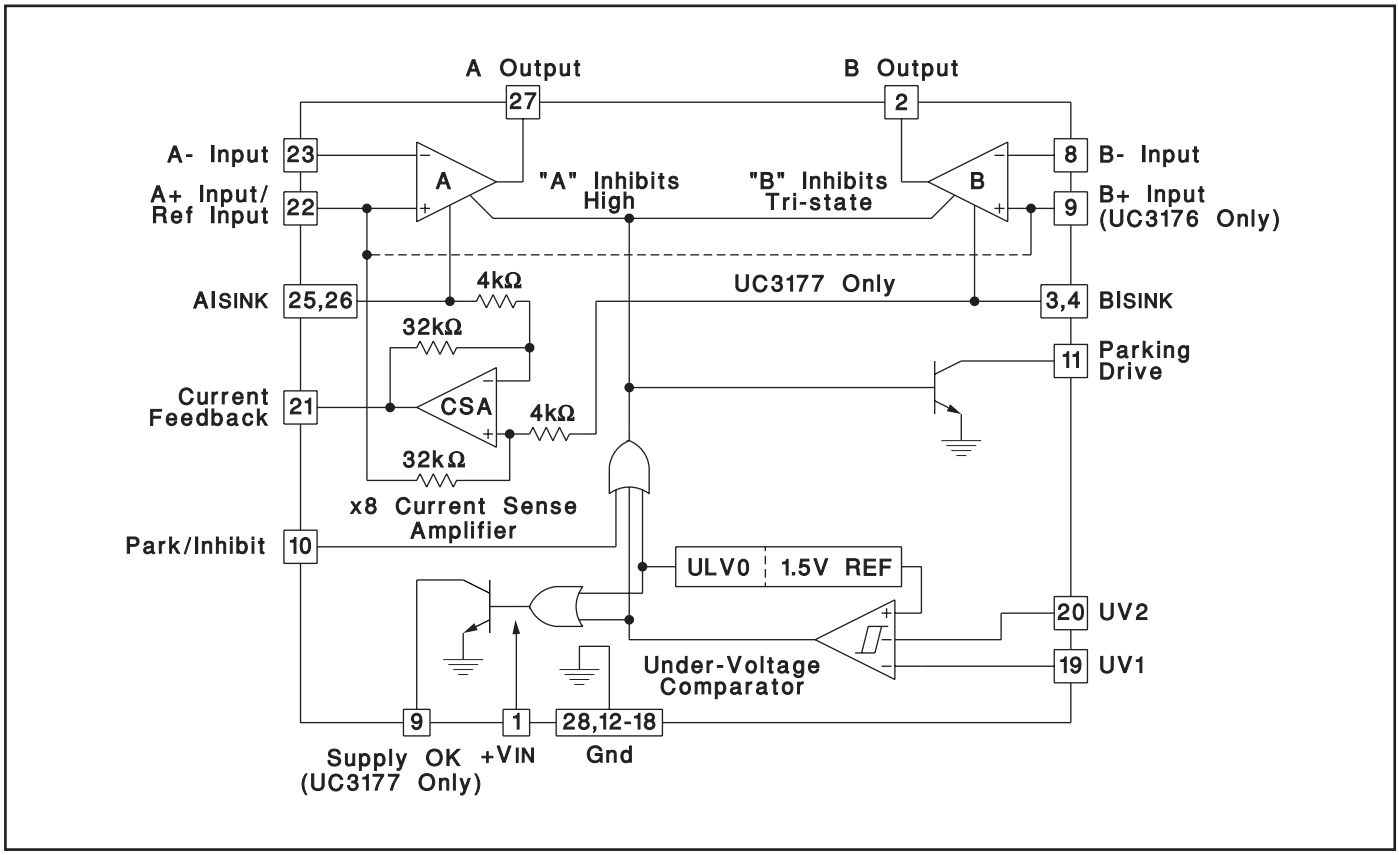
DESCRIPTION

The UC3176/7 family of full bridge power amplifiers is rated for a continuous output current of 2A. Intended for use in demanding servo applications such as disk head positioning, the onboard current sense amplifier can be used to obtain precision control of load current, or where voltage mode drive is required, a standard voltage feedback scheme can be used. Output stage protection includes foldback current limiting and thermal shutdown, resulting in a very rugged device.

Auxiliary functions on this device include a dual input under-voltage comparator that can be programmed to respond to low voltage conditions on two independent supplies. In response to an under-voltage condition the power Op-Amps are inhibited and a high current, 100mA, open collector drive output is activated. A separate Park/Inhibit command input.

The devices are operational over a 3V to 35V supply range. Internal under-voltage lockout provides predictable power-up and power-down characteristics.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

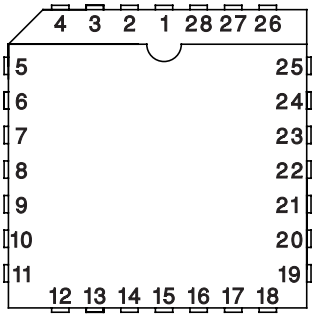
Input Supply voltage, ($+V_{IN}$) 40V
Park/Inhibit, UV1 and UV2 inputs (zener clamped)
  Maximum forced voltage . . . . . –0.3V to 10V
  Maximum forced current . . . . . ±10mA
Other Input Voltages . . . . . –0.3V to $+V_{IN}$
AI_{SINK} and BI_{SINK} Voltages . . . . . –0.3V to 6V
Open Collector Output Voltages 40V
A and B Output Currents (Continuous)
  Source . . . . . Internally Limited
  Sink 2.5A
Total Supply Current (Continuous) 4A
Parking Drive Output Current (Continuous) 200mA
Supply OK Output Current, UC3177 (Continuous) 30mA
Operating Junction Temperature . . . . . –55°C to +150°C
Power Dissipation at TC = +75°C
  QP package 4W
Storage Temperature . . . . . –65°C to +150°C

THERMAL DATA

QP package:
  Thermal Resistance Junction to Leads, θ_{JL} . . . . . 15°C/W
  Thermal Resistance Junction to Ambient, θ_{JA} . . . . . 50°C/W
  Thermal Resistance Junction to C_{OSC}, θ_{JC} . . . . . 30°C/W

CONNECTION DIAGRAM

PLCC-28 (Top View)
QP Package



*Pin 9: UC3176, B+ Input
UC3177, Supply OK

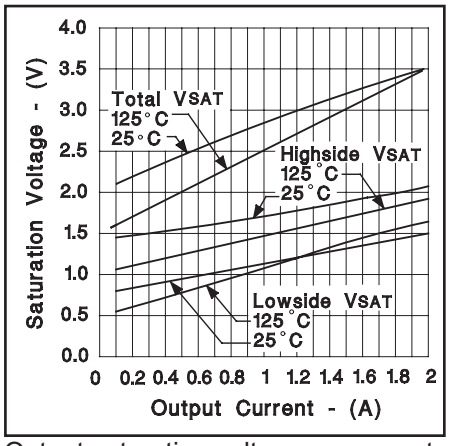
PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
$+V_{IN}$	1
B Output	2
BI_{SINK} (Sense)	3
BI_{SINK}	4
N/C	5-7
B– Input	8
*	9
Park/Inhibit	10
Parking Drive	11
Gnd (Heat Flow Pins)	12-18
UV1	19
UV2	20
Current Feedback	21
A+ Input	22
A– Input	23
N/C	24
AI_{SINK}	25
AI_{SINK} (Sense)	26
A Output	27
Gnd	28

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0 to 70°C, $+V_{IN}$ = 12V, $T_A = T_J$.

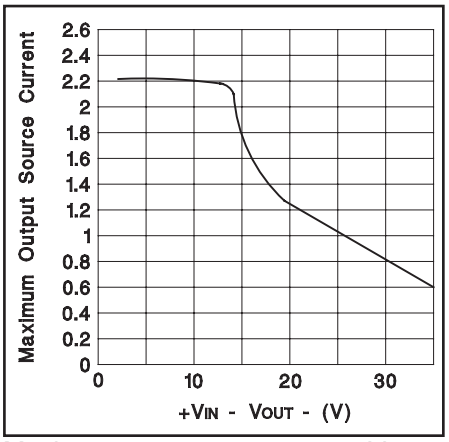
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	$+V_{IN}$ = 12V		18	25	mA
	$+V_{IN}$ = 35V		21	30	mA
UVOL Threshold	$+V_{IN}$ low to high		2.8	3.0	V
	Threshold Hysteresis		220	300	mV
Power, Amplifier, A and B					
Input Offset Voltage	V_{CM} = 6V, V_{OUT} = 6V			8	mV
Input Bias Current	V_{CM} = 6V, Except A+ Input	–500	–100		nA
Input Bias Current at A+/Reference Input	(A+/REF - BI_{SINK}) /36kΩ; T_J = 25°C	23	28	35	µA/V
Input Offset Current B Amp (UC3176 Only)	V_{CM} = 6V			200	nA
CMRR	V_{CM} = 1 to 33V, $+V_{IN}$ = 35V, V_{OUT} = 6V	70	100		dB
PSRR	$+V_{IN}$ = 5 to 35V, V_{CM} = 2.5V	70	100		dB
Large Signal Voltage Gain	V_{OUT} = 3V, w/I_{OUT} = 1A to V_{OUT} = 9V, w/I_{OUT} = –1A	1.5	4		V/mV
Thermal Feedback	$+V_{IN}$ = 20V, Pd = 20W at opposite output		25	200	µV/W
Saturation Voltage	I_{OUT} = –2A, High Side, T_J = 25°		1.9		V
	CI_{OUT} = 2A, Low Side, T_J = 25°C		1.6		V
	Total V_{SAT} at 2A, T_J = 25°C		3.5	3.7	V
Unity Gain Bandwidth			1		MHz
Slew Rate			1		V/µs
Differential I_{OUT} Sense Error Current in Bridge Configuration	$I_{OUT}(A) = -I_{OUT}(B)$, $/I_{OUT}/ - /AI_{SINK} - BI_{SINK}/$				
	$I_{OUT} \le 200mA$		3.0	6.0	mA
	$I_{OUT} \le 2A$		5.0	10	mA
High Side Current Limiting	$=V_{IN} - V_{OUT} < 12V$		–2.7	–2.0	A

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0 to 70°C, $+V_{IN}$ = 12V, $T_A = T_J$.

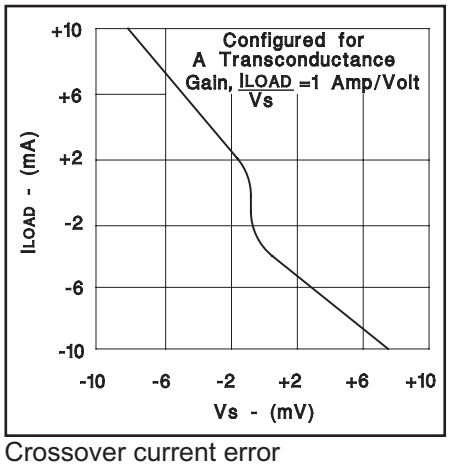
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 0V, A+ / REF at 6V			3	mV
	REF = 2V to 20V, $+V_{IN}$ = 35, change with REF Input voltage			600	µV/V
Thermal Gradient Sensitivity	$+V_{IN}$ = 20V, REF = 10V Pd = 20W @ A or B Output		5.0	75.0	µV/W
PSRR	REF = 2.5V, $+V_{IN}$ = 5 to 35V	70	100		dB
Gain	$/\Delta I_{SINK}$-$B I_{SINK}$ / ≤ 0.5V	7.8	8.0	8.1	V/V
Slew Rate			2		V/µS
3dB Bandwidth			1		MHz
MAX Output Current	$I_{SOURCE} = +V_{IN} - V_{OUT}$ = 0.5V	2.5	3.5		mA
Output Saturation Voltage	I_{SOURCE} = 1.5mA, High Side		0.15	0.30	V
	I_{SINK} = 5mA, Low Side		1.4	1.85	V
Under-Voltage Comparator					
Threshold Voltage	Low to High, other input at 5V	1.44	1.50	1.56	V
	Threshold Hysteresis	50	70	80	mV
Input Current	Input = 2V, other input at 5V	–2.00	–.05		µA
Supply OK V_{SAT} (UC3177 Only)	I_{OUT} = 5mA			0.45	V
Supply OK Leakage (UC3177 Only)	V_{OUT} = 35V			5	µA
Park/Inhibit					
Park/Inhibit Thl'd		1.1	1.3	1.7	V
Park/Inhibit Input Current	At threshold		60	100	µA
Parking Drive Saturation Voltage	I_{OUT} = 100mA		0.3	0.7	V
Parking Drive Leakage	V_{OUT} = 35V			15	µA
Thermal Shutdown					
Shutdown Temperature			165		°C



Output saturation voltage vs. current.

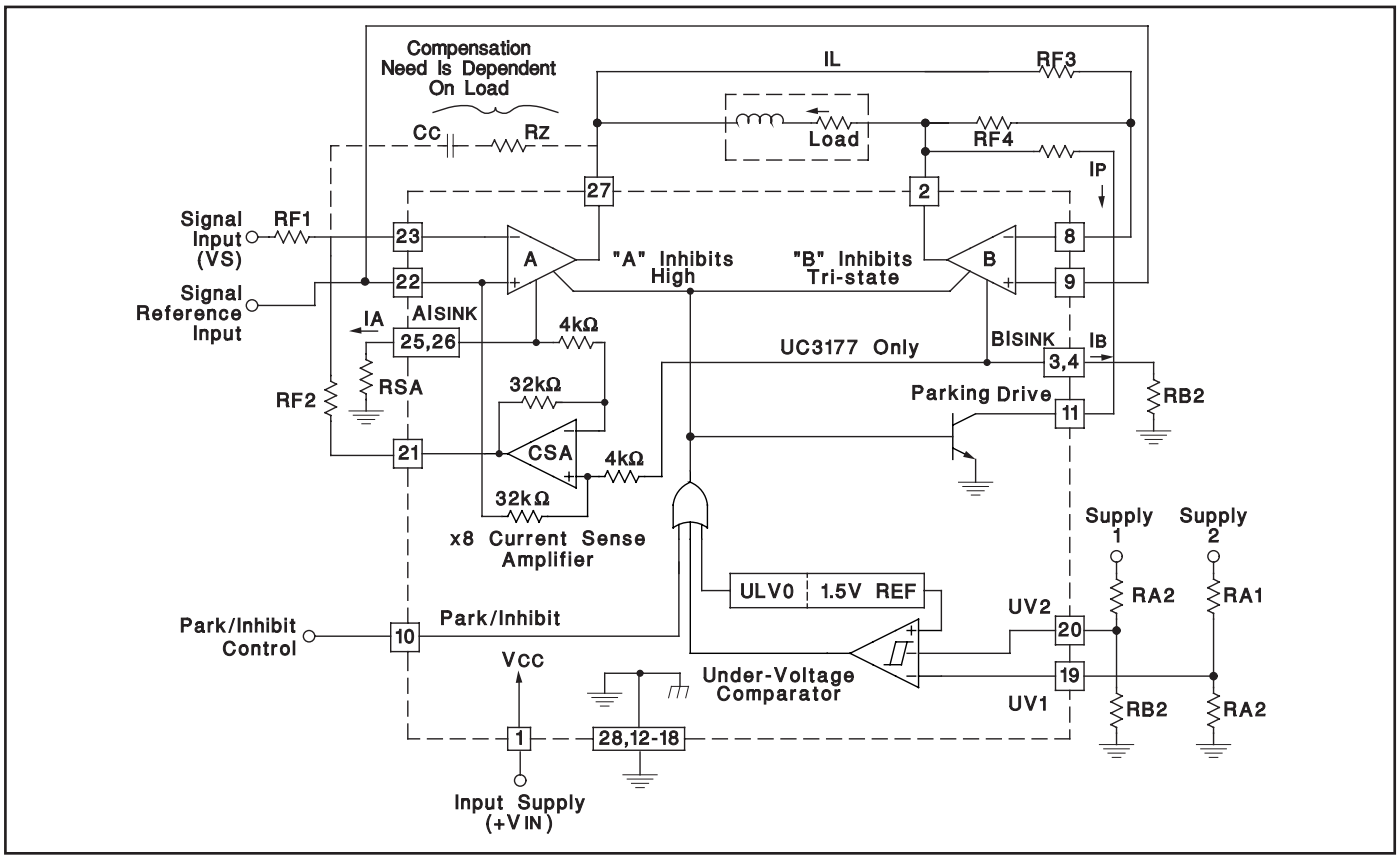


Maximum source current vs. + V_{IN} – V_{OUT}.

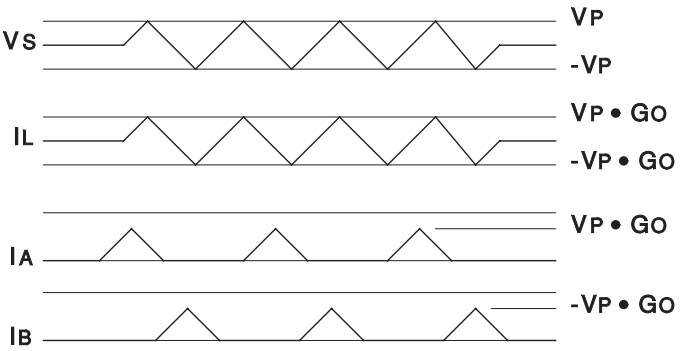


Crossover current error characteristic.

APPLICATION AND OPERATION INFORMATION



WAVEFORMS FOR ABOVE APPLICATION



DESIGN EQUATIONS

Transconductance (G_O) = $\frac{I_L}{V_S} = \frac{R_{F2}}{R_{F1}} \times \left(\frac{1}{8R_S}\right)$

with: $R_{SA} = R_{SB}$ and $R_{F3} = R_{F4}$

Parking Current (I_P) = $\frac{V_{IN} - 1.5}{R_P + R_L}$

where: R_L = load resistance

Under-Voltage Thresholds, at Supplies
High to Low Threshold, (V_{LH}) = 1.425 (R_A + R_B)/R_B
Low to High Threshold, (V_{HL}) = 1.5 (R_A + R_B)/R_B

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3176QP	NRND	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	UC3176QP	
UC3176QPTR	NRND	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	UC3176QP	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

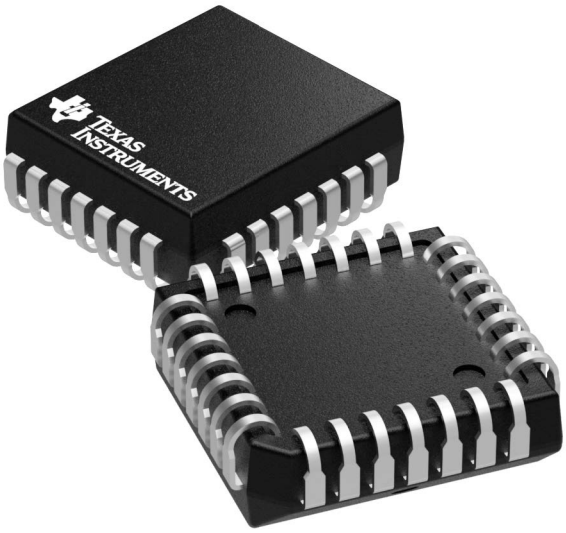
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

FN 28

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

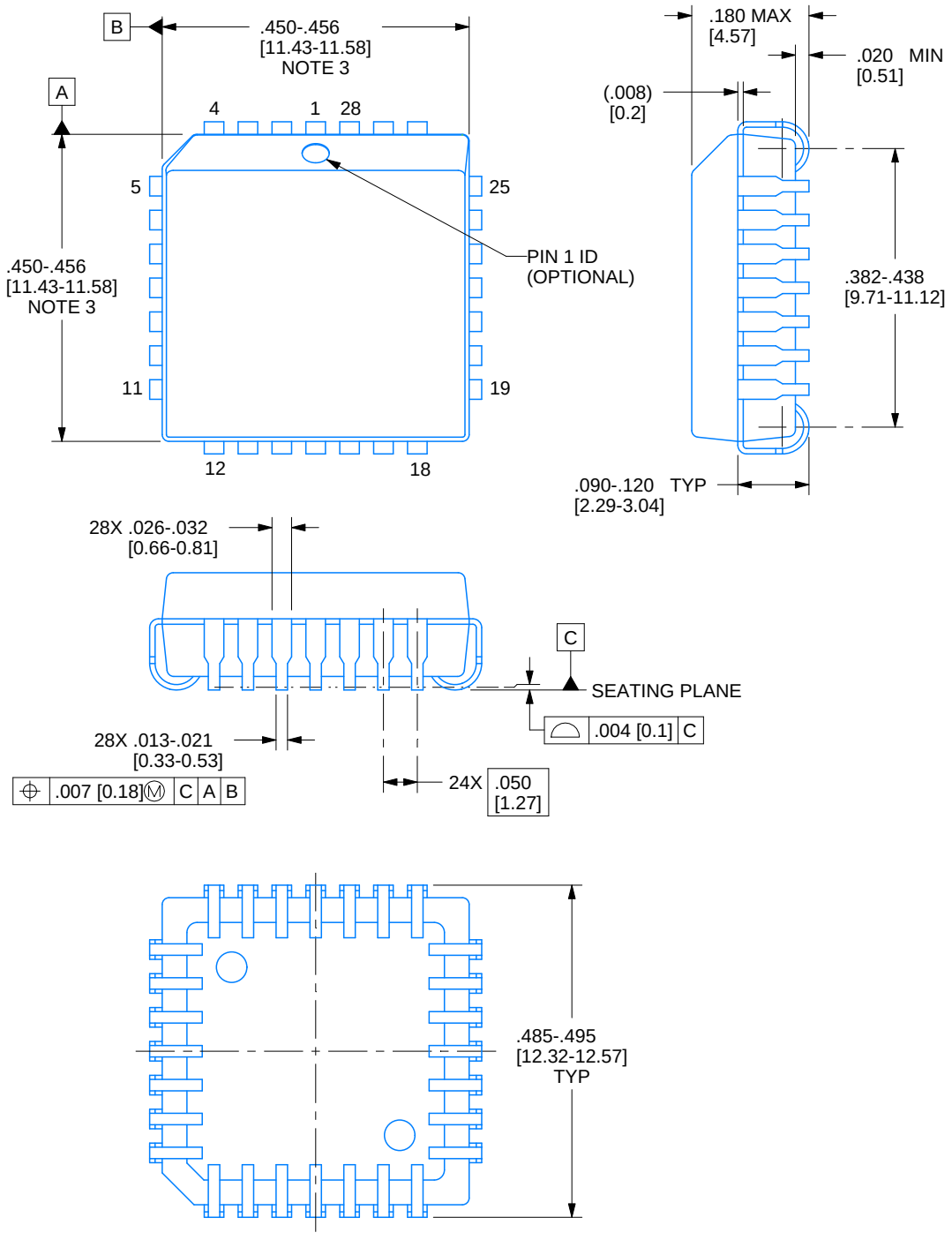
4040005-3/C

PACKAGE OUTLINE

FN0028A

PLCC - 4.57 mm max height

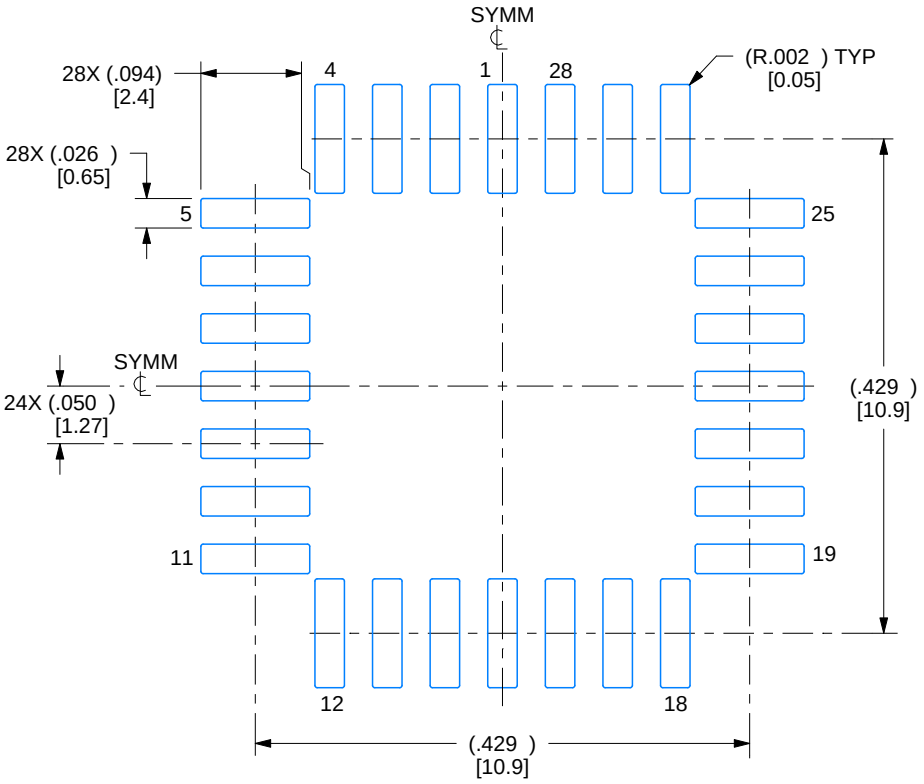
PLASTIC CHIP CARRIER



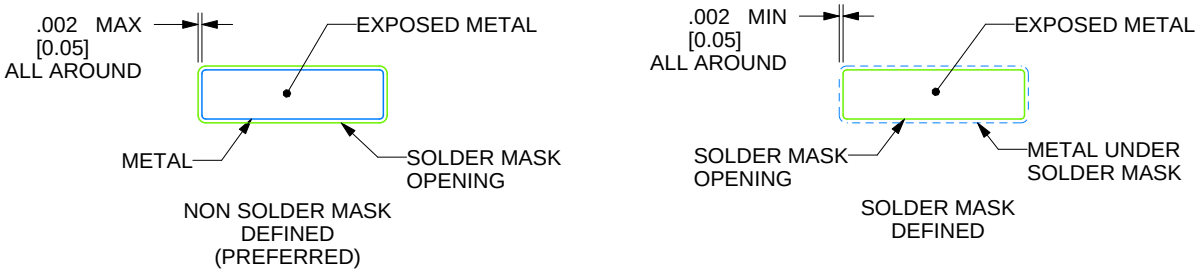
4215153/B 05/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

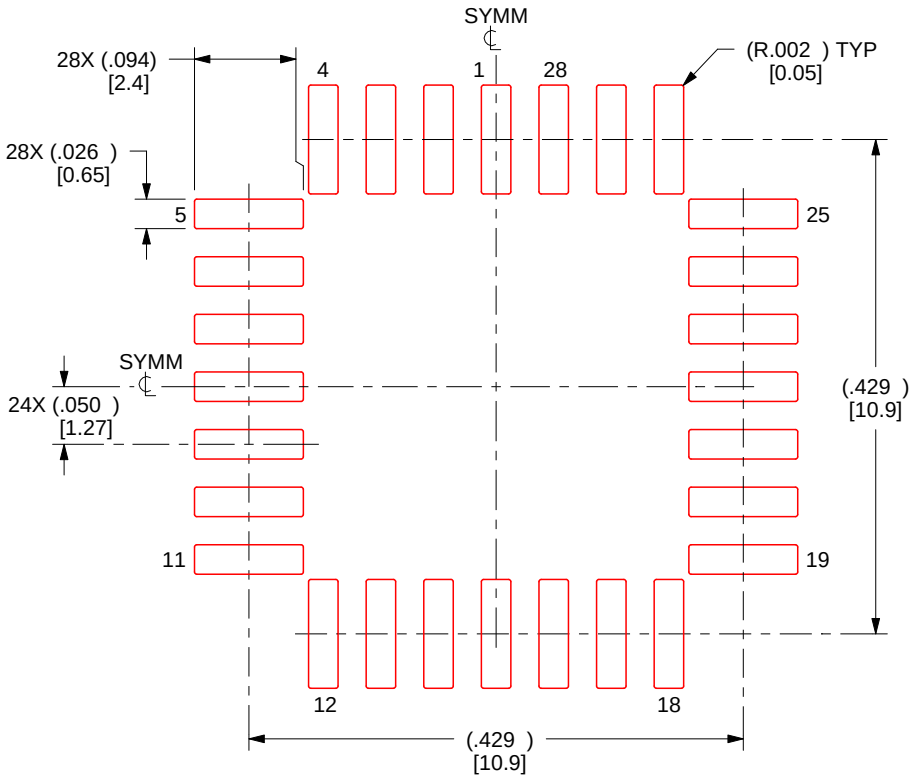


SOLDER MASK DETAILS

4215153/B 05/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215153/B 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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