TLVx379
Cost-Optimized, Low-Voltage, 4-µA, Rail-to-Rail I/O Operational Amplifiers

1 Features

- Cost-Optimized Precision Amplifiers
- microPower: 4 µA (Typical)
- Low Offset Voltage: 0.8 mV (Typical)
- Rail-to-Rail Input and Output
- Unity-Gain Stable
- Wide Supply Voltage Range: 1.8 V to 5.5 V
- microSize Packages:
  - 5-Pin SC70
  - 5-Pin SOT-23
  - 8-Pin SOIC
  - 14-Pin TSSOP

2 Applications

- Power Banks
- Solar Inverters
- Low-Power Motor Controls
- Battery-Powered Instruments
- Portable Devices
- Medical Instruments
- Handheld Test Equipment

3 Description

The TLV379 family of single, dual, and quad operational amplifiers represents a cost-optimized generation of low-voltage and micropower amplifiers. Operating on a supply voltage as low as 1.8 V (±0.9 V) and consuming extremely low quiescent current of 4 µA per channel, these amplifiers are well-suited for power-sensitive applications. In addition, the rail-to-rail input and output capability allows the TLV379 family to be used in virtually any single-supply application.

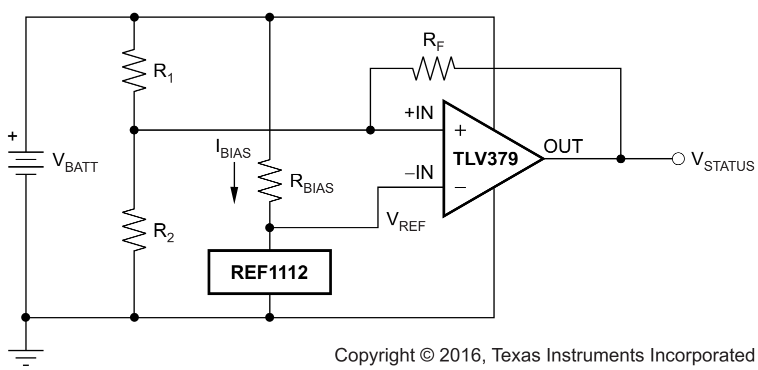
The TLV379 (single) is available in 5-pin SC70 and SOT23, and 8-pin SOIC packages. The TLV2379 (dual) comes in an 8-pin SOIC package. The TLV4379 (quad) is offered in a 14-pin TSSOP package. All versions are specified from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV379	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
TLV2379	SOIC (8)	4.90 mm × 3.91 mm
TLV4379	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TLV379 in a Battery-Monitoring Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2016) to Revision B	Page
• Added underscores to pin names in Pin Functions tables to match connection diagrams	4

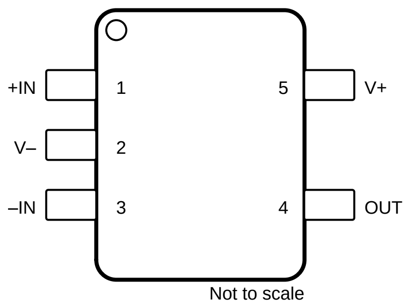
Changes from Original (April 2016) to Revision A	Page
• Changed DBV pinout	3

5 Device Comparison Table

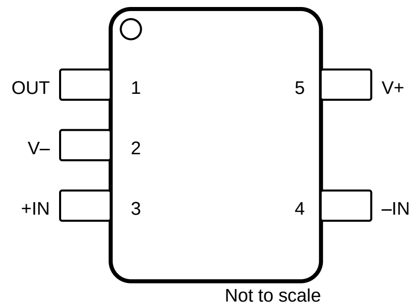
FEATURES	PRODUCT
1 µA, 70 kHz, 2-mV V_{OS}, 1.8-V to 5.5-V supply	OPAx349
1 µA, 5.5 kHz, 390-µV V_{OS}, 2.5-V to 16-V supply	TLV240x
1 µA, 5.5 kHz, 0.6-mV V_{OS}, 2.5-V to 12-V supply	TLV224x
7 µA, 160 kHz, 0.5-mV V_{OS}, 2.7-V to 16-V supply	TLV27Lx
7 µA, 160 kHz, 0.5-mV V_{OS}, 2.7-V to 16-V supply	TLV238x
20 µA, 350 kHz, 2-mV V_{OS}, 2.3-V to 5.5-V supply	OPAx347
20 µA, 500 kHz, 550-µV V_{OS}, 1.8-V to 3.6-V supply	TLV276x
45 µA, 1 MHz, 1-mV V_{OS}, 2.1-V to 5.5-V supply	OPAx348

6 Pin Configuration and Functions

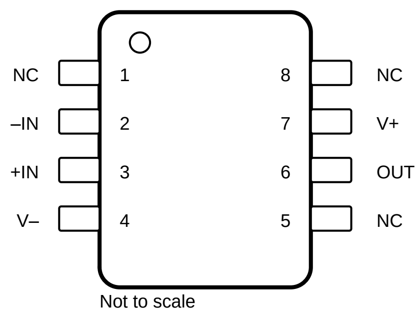
TLV379: DCK Package
5-Pin SC70
Top View



TLV379: DBV Package
5-Pin SOT23
Top View



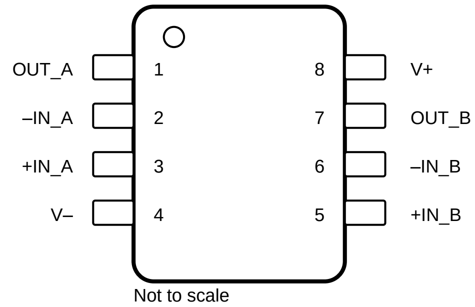
TLV379: D Package
8-Pin SOIC
Top View



Pin Functions: TLV379

NAME	NO.			I/O	DESCRIPTION
	DCK	DBV	D		
–IN	3	4	2	I	Negative (inverting) input
+IN	1	3	3	I	Positive (noninverting) input
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	4	1	6	O	Output
V–	2	2	4	—	Negative (lowest) power supply
V+	5	5	7	—	Positive (highest) power supply

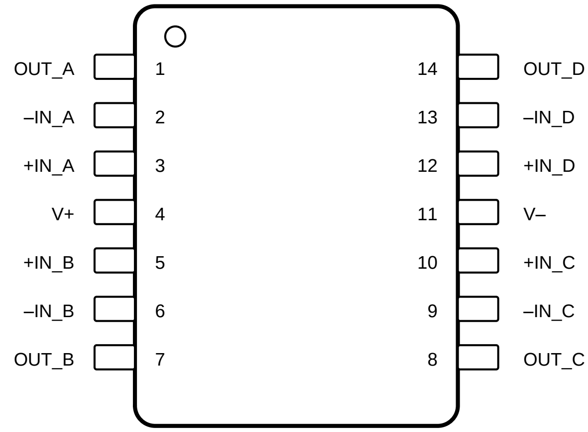
TLV2379: D Package
8-Pin SOIC
Top View



Pin Functions: TLV2379

NAME	NO.	I/O	DESCRIPTION
–IN_A	2	I	Inverting input, channel A
+IN_A	3	I	Noninverting input, channel A
–IN_B	6	I	Inverting input, channel B
+IN_B	5	I	Noninverting input, channel B
OUT_A	1	O	Output, channel A
OUT_B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

TLV4379: PW Package
14-Pin TSSOP
Top View



Not to scale

Pin Functions: TLV4379

NAME	NO.	I/O	DESCRIPTION
–IN_A	2	I	Inverting input, channel A
+IN_A	3	I	Noninverting input, channel A
–IN_B	6	I	Inverting input, channel B
+IN_B	5	I	Noninverting input, channel B
–IN_C	9	I	Inverting input, channel C
+IN_C	10	I	Noninverting input, channel C
–IN_D	13	I	Inverting input, channel D
+IN_D	12	I	Noninverting input, channel D
OUT_A	1	O	Output, channel A
OUT_B	7	O	Output, channel B
OUT_C	8	O	Output, channel C
OUT_D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage	Supply, V_S = (V+) – (V–)		7	V
	Signal input pin[(2)]	(V–) – 0.5	(V+) + 0.5	
Current	Signal input pin[(2)]		±10	mA
	Output short-circuit[(3)]	Continuous		
Temperature	Operating, T_A	–40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	1.8		5.5	V
		Dual supply	±0.9		±2.75	
T_A	Operating temperature		–40		125	°C

7.4 Thermal Information: TLV379

THERMAL METRIC[(1)]		TLV379			UNIT
		DCK (SC70)	DBV (SOT23)	D (SOIC)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.2	220.8	130.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.7	148.3	77.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.0	48.2	71.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	28.6	30.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.2	47.3	70.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: TLV2379

THERMAL METRIC[(1)]		TLV2379	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: TLV4379

THERMAL METRIC[(1)]		TLV4379	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics: V_S = 1.8 V to 5.5 V

at T_A = 25°C, R_L = 25 kΩ connected to V_S / 2, and V_{CM} < (V+) – 1 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		0.8	2.5	mV
dV_{OS}/dT	V_{OS} drift	T_A = –40°C to +125°C		3		µV/°C
PSRR	Power-supply rejection ratio		92	104		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio(1)	(V–) < V_{CM} < (V+) – 1 V	85	100		dB
		T_A = –40°C to +125°C, (V–) < V_{CM} < (V+) – 1 V	62			
INPUT BIAS CURRENT						
I_{IB}	Input bias current	V_S = 5 V, V_{CM} ≤ V_S / 2		±5		pA
I_{IO}	Input offset current	V_S = 5 V		±5		pA
INPUT IMPEDANCE						
	Differential			10^{13} || 3		Ω || pF
	Common-mode			10^{13} || 6		Ω || pF
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2.8		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz		83		nV/√Hz
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5 V, R_L = 5 kΩ, 500 mV < V_O < (V+) – 500 mV	90	110		dB
OUTPUT						
	Voltage output swing from rail	R_L = 5 kΩ		25	50	mV
		T_A = –40°C to +125°C, R_L = 5 kΩ			75	
I_{SC}	Short-circuit current			±5		mA
C_{LOAD}	Capacitive load drive		See *Capacitive Load and Stability* section			
R_{OUT}	Closed-loop output impedance	G = 1, f = 1 kHz, I_O = 0		10		Ω
R_O	Open-loop output impedance	f = 100 kHz, I_O = 0		28		kΩ
FREQUENCY RESPONSE (C_{LOAD} = 30 pF)						
GBW	Gain bandwidth product			90		kHz
SR	Slew rate	G = 1		0.03		V/µs
	Overload recovery time	V_{IN} × Gain > V_S		25		µs
t_{ON}	Turn-on time			1		ms
POWER SUPPLY						
V_S	Specified, operating voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	V_S = 5 V, T_A = –40°C to +125°C		4	12	µA
TEMPERATURE						
T_A	Specified, operating range		–40		125	°C
T_{stg}	Storage range		–65		150	°C

(1) See typical characteristic graph, *Common-Mode Rejection Ratio vs Frequency* (Figure 2).

7.8 Typical Characteristics

at T_A = 25°C, V_S = 5 V, and R_L = 25 kΩ connected to V_S / 2 (unless otherwise noted)

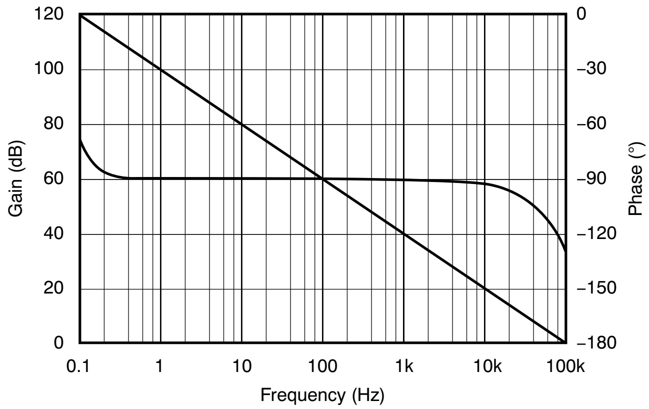


Figure 1. Open-Loop Gain and Phase vs Frequency

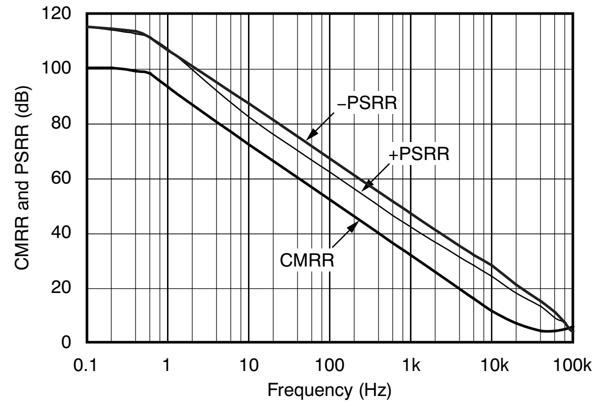


Figure 2. Common-Mode and Power-Supply Rejection Ratio vs Frequency

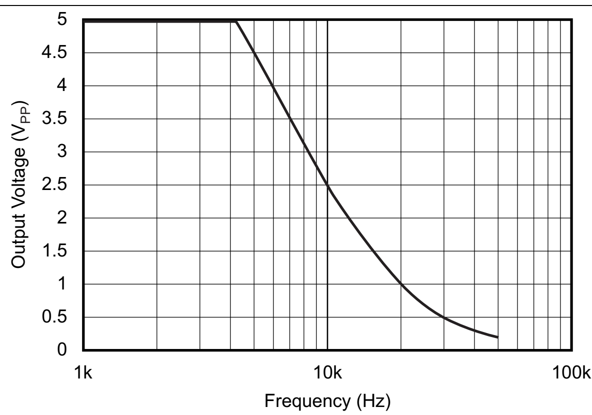
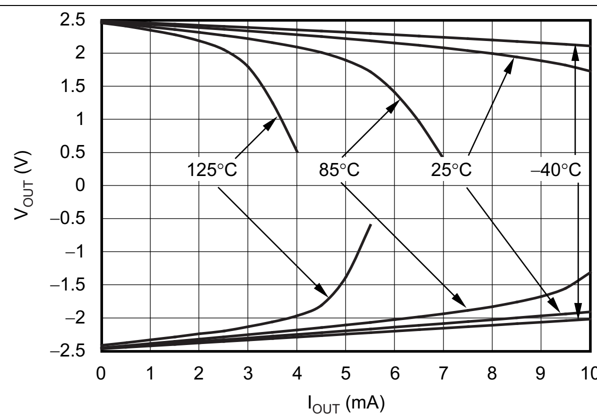


Figure 3. Maximum Output Voltage vs Frequency



V_S = ±2.5 V

Figure 4. Output Voltage vs Output Current

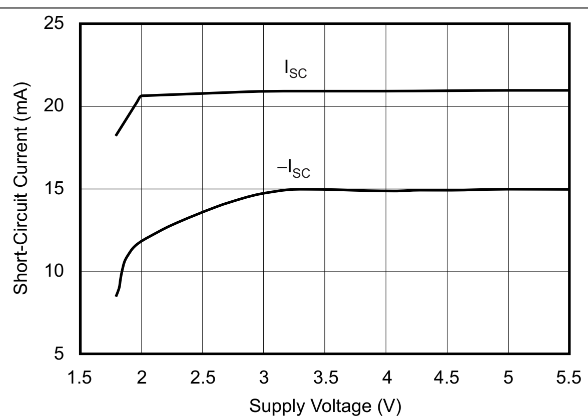


Figure 5. Short-Circuit Current vs Supply Voltage

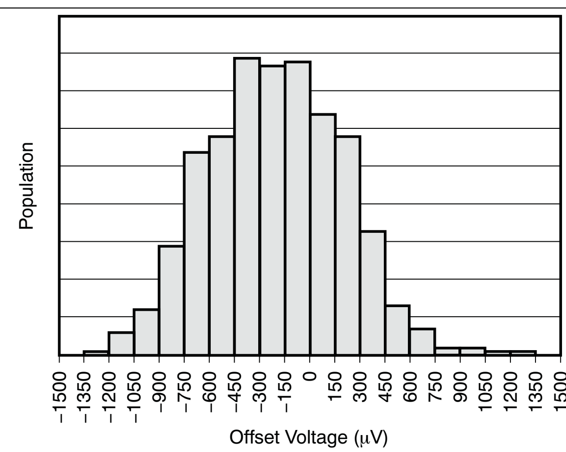


Figure 6. Offset Voltage Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and R_L = 25 kΩ connected to V_S / 2 (unless otherwise noted)

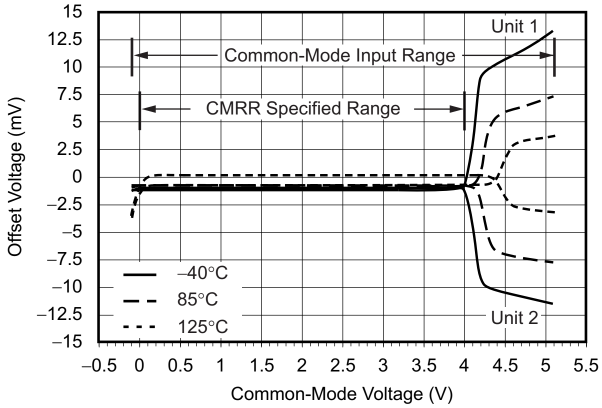


Figure 7. Offset Voltage vs Common-Mode Voltage and Temperature

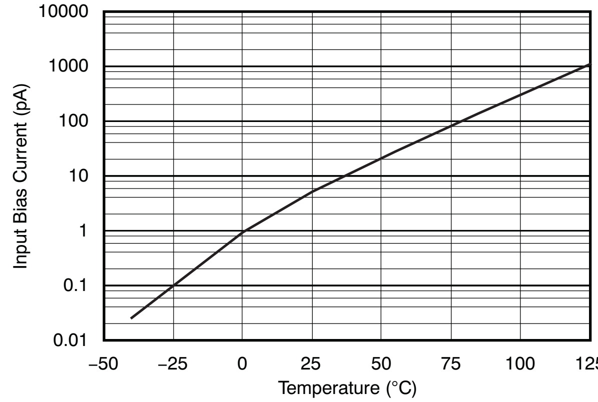


Figure 8. Input Bias Current vs Temperature

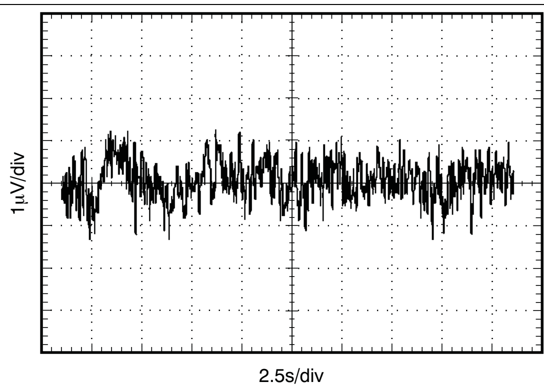


Figure 9. 0.1-Hz to 10-Hz Noise

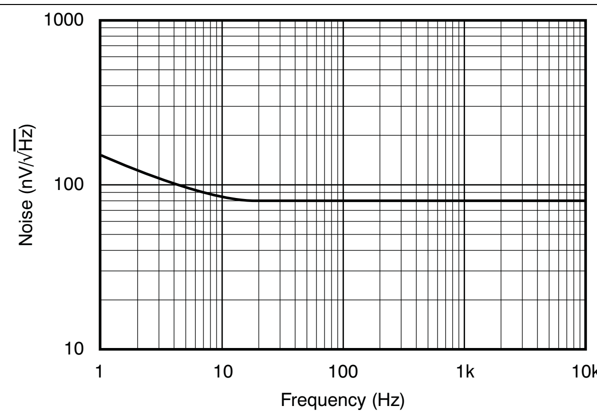


Figure 10. Noise vs Frequency

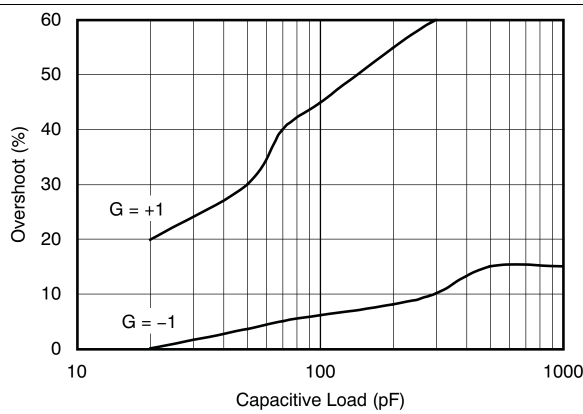


Figure 11. Small-Signal Overshoot vs Capacitive Load

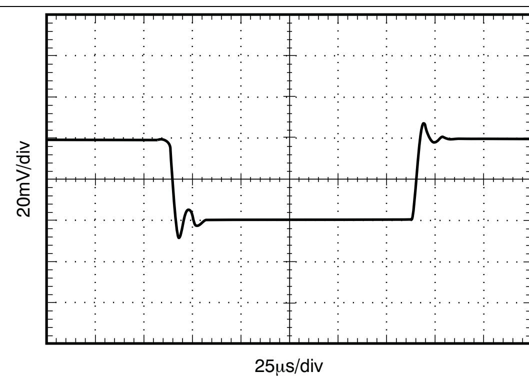


Figure 12. Small-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and R_L = 25 kΩ connected to V_S / 2 (unless otherwise noted)

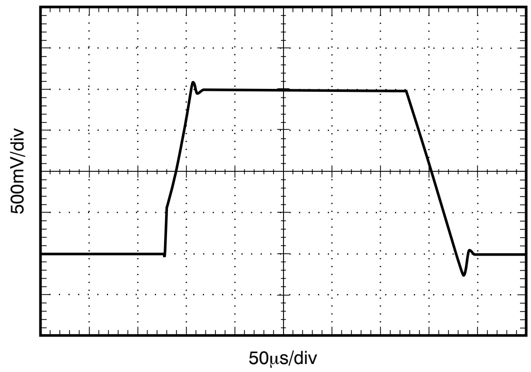


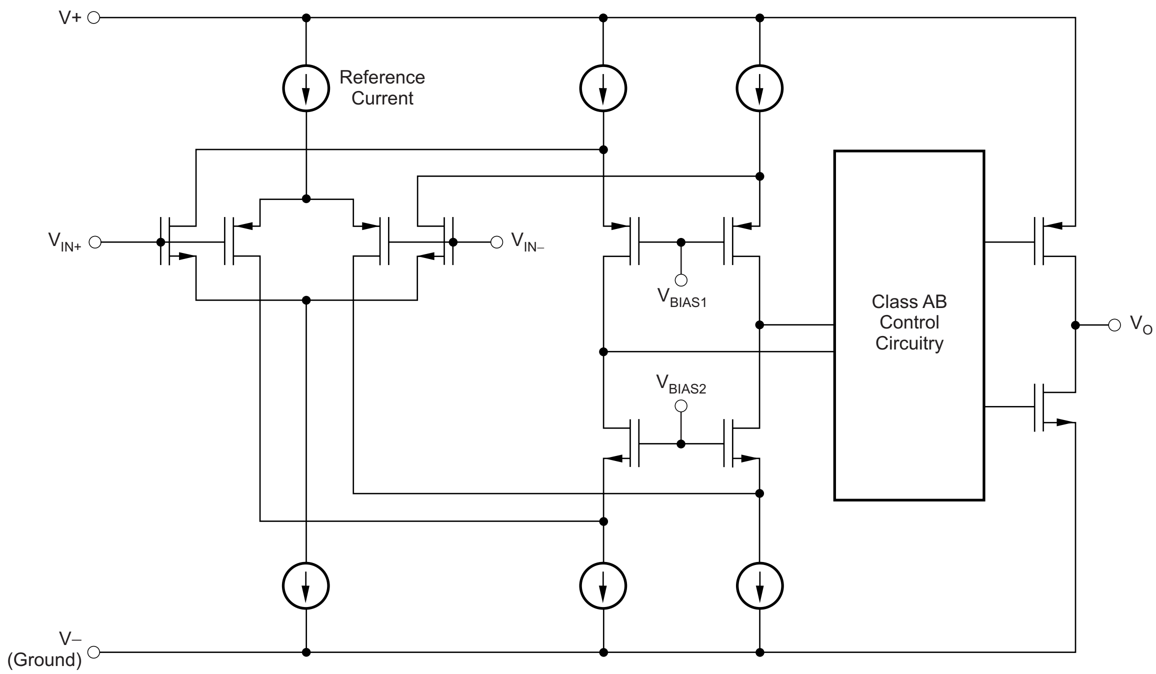
Figure 13. Large-Signal Step Response

8 Detailed Description

8.1 Overview

The TLV379 devices are a family of micropower, low-voltage, rail-to-rail input and output operational amplifiers designed for battery-powered applications. This family of amplifiers features impressive bandwidth (90 kHz), low bias current (5 pA), low noise (83 nV/√Hz), and consumes very low quiescent current of only 12 µA (maximum) per channel.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Voltage

The TLV379 series is fully specified and tested from 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary with supply voltage are illustrated in the *Typical Characteristics* section.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV379 family typically extends 100 mV beyond each supply rail. This rail-to-rail input is achieved using a complementary input stage. CMRR is specified from the negative rail to 1 V below the positive rail. Between (V+) – 1 V and (V+) + 0.1 V, the amplifier operates with higher offset voltage because of the transition region of the input stage. See the typical characteristic graph, *Offset Voltage vs Common-Mode Voltage vs Temperature* (Figure 7).

Feature Description (continued)

8.3.3 Rail-to-Rail Output

Designed as a micropower, low-noise operational amplifier, the TLV379 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 25 kΩ, the output typically swings to within 5 mV of either supply rail, regardless of the power-supply voltage applied.

8.3.4 Capacitive Load and Stability

Follower configurations with load capacitance in excess of 30 pF can produce extra overshoot (see the typical characteristic graph, *Small-Signal Overshoot vs Capacitive Load*, Figure 11) and ringing in the output signal. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10 Ω to 20 Ω) resistor, R_S, in series with the output as shown in Figure 14. This resistor significantly reduces ringing and maintains direct current (dc) performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio of R_S / R_L and is generally negligible.

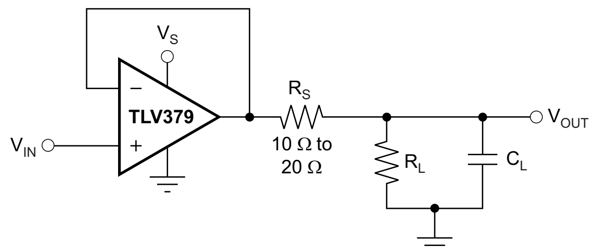


Figure 14. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the operational amplifier (op amp) input and the gain-setting resistors. Best performance is achieved by using smaller-value resistors. However, when large-value resistors cannot be avoided, a small (4 pF to 6 pF) capacitor (C_{FB}) can be inserted in the feedback, as shown in Figure 15. This configuration significantly reduces overshoot by compensating the effect of capacitance (C_{IN}) that includes the amplifier input capacitance (3 pF) and printed circuit board (PCB) parasitic capacitance.

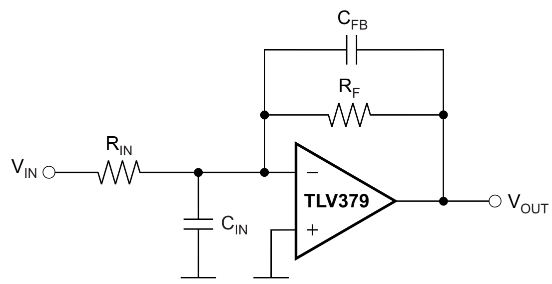


Figure 15. Improving Stability for Large R_F and R_{IN}

8.4 Device Functional Modes

The TLV379 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing for ultra-low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors can react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. Use of a feedback capacitor assures stability and limits overshoot or gain peaking.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 16. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor R_I and the feedback resistor R_F.

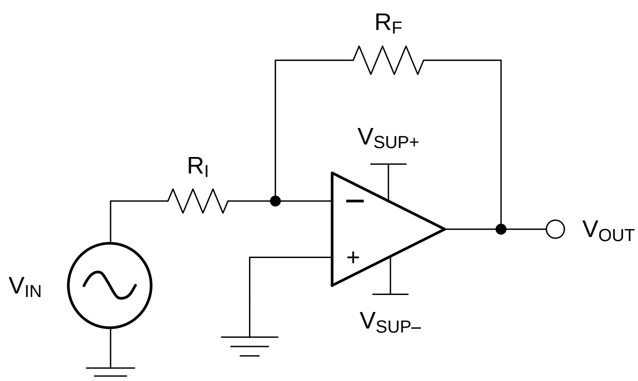


Figure 16. Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Typical Application (continued)

When the desired gain is determined, choose a value for R_I or R_F. Choosing a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of kilohms) draw the smallest current but generate the highest noise. Very small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 kΩ for R_I, meaning 36 kΩ is used for R_F. These values are determined by Equation 3:

$$A_V = -\frac{R_F}{R_I} \tag{3}$$

9.2.3 Application Curve

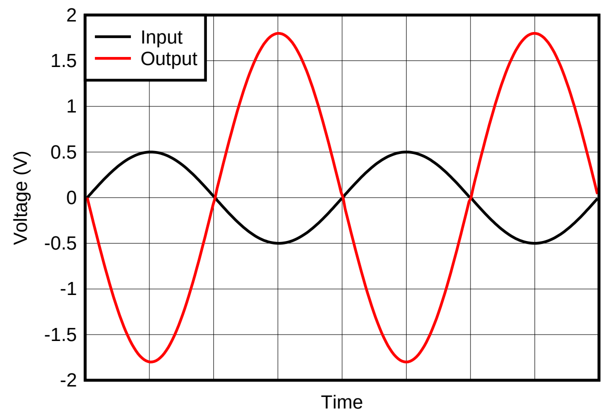


Figure 17. Inverting Amplifier Input and Output

9.3 System Examples

Figure 18 shows the basic configuration for a bridge amplifier using the TLV379.

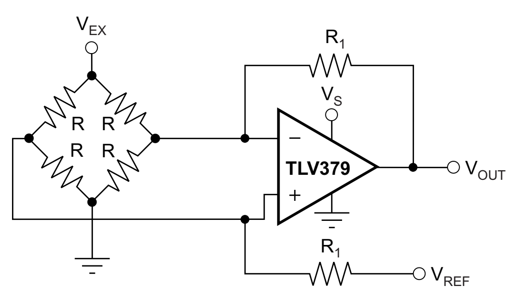


Figure 18. Single Op Amp Bridge Amplifier

System Examples (continued)

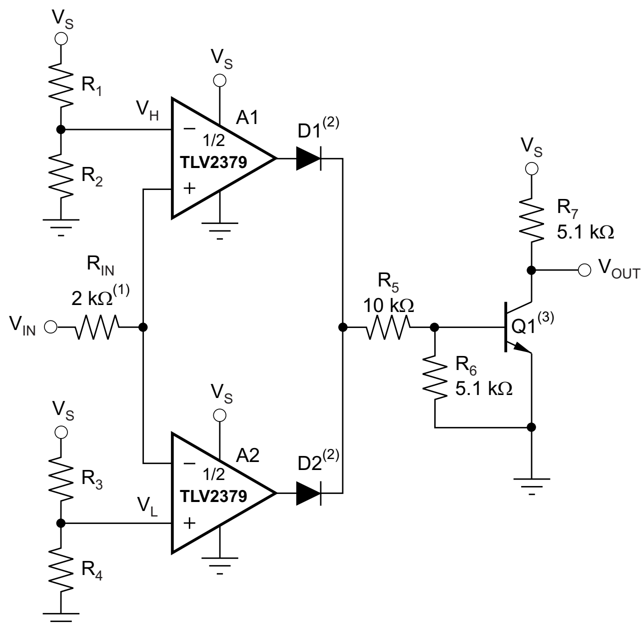
Figure 19 shows the TLV2379 used as a window comparator. The threshold limits are set by V_H and V_L, with $V_H > V_L$. When $V_{IN} < V_H$, the output of A1 is low. When $V_{IN} > V_L$, the output of A2 is low. Therefore, both op amp outputs are at 0 V as long as V_{IN} is between V_H and V_L. This architecture results in no current flowing through either diode, Q1 in cutoff, with the base voltage at 0 V, and V_{OUT} forced high.

If V_{IN} falls below V_L, the output of A2 is high, current flows through D2, and V_{OUT} is low. Likewise, if V_{IN} rises above V_H, the output of A1 is high, current flows through D1, and V_{OUT} is low.

The window comparator threshold voltages are set using Equation 4 and Equation 5.

$$V_H = \frac{R_2}{R_1 + R_2} \times V_S \tag{4}$$

$$V_L = \frac{R_4}{R_3 + R_4} \times V_S \tag{5}$$



(1) R_{IN} protects A1 and A2 from possible excess current flow.
(2) IN4446 or equivalent diodes.
(3) 2N2222 or equivalent NPN transistor.

Figure 19. TLV2379 as a Window Comparator

10 Power Supply Recommendations

The TLV379 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Layout Guidelines* section.

10.1 Input and ESD Protection

The TLV379 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 20 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input that must be kept to a minimum in noise-sensitive applications.

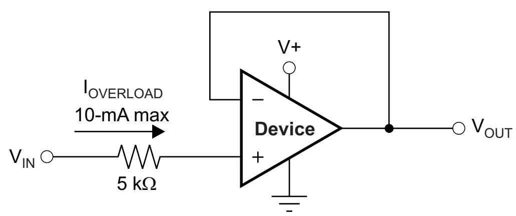


Figure 20. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close as possible to the device. Keep R_F and R_G close to the inverting input in order to minimize parasitic capacitance, as shown in Figure 21.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

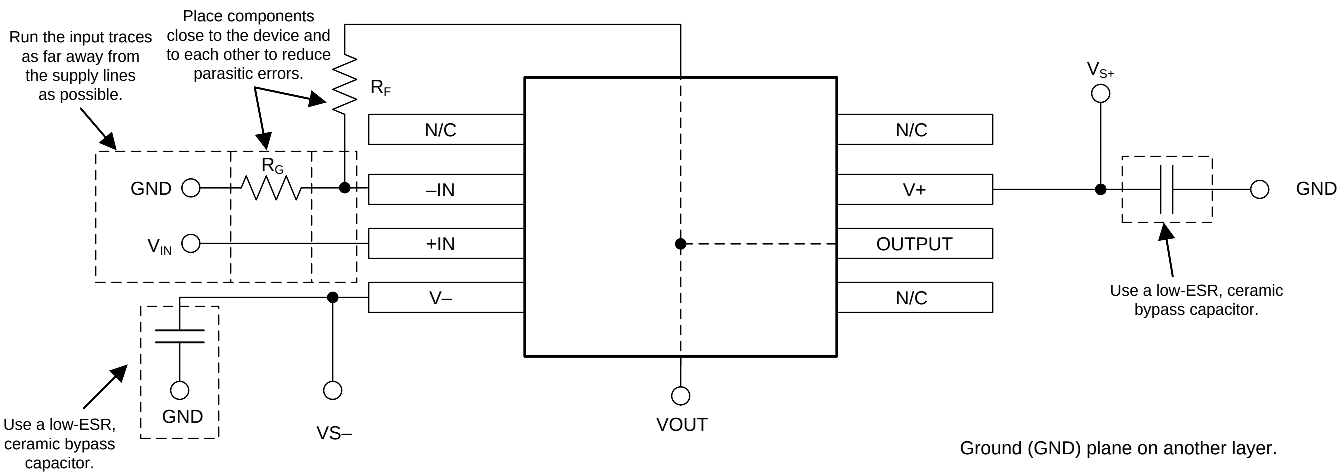


Figure 21. Operational Amplifier Board Layout for Noninverting Configuration

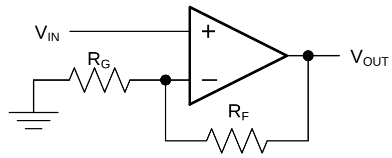


Figure 22. Schematic Representation of Figure 21

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers* (SBOA128)
- *Circuit Board Layout Techniques* (SLOA089)
- *QFN/SON PCB Attachment* (SLUA271)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)

12.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV379	Click here	Click here	Click here	Click here	Click here
TLV2379	Click here	Click here	Click here	Click here	Click here
TLV4379	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2379IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V2379	Samples
TLV379IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12N	Samples
TLV379IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12N	Samples
TLV379IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12O	Samples
TLV379IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12O	Samples
TLV379IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 379	Samples
TLV4379IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4379	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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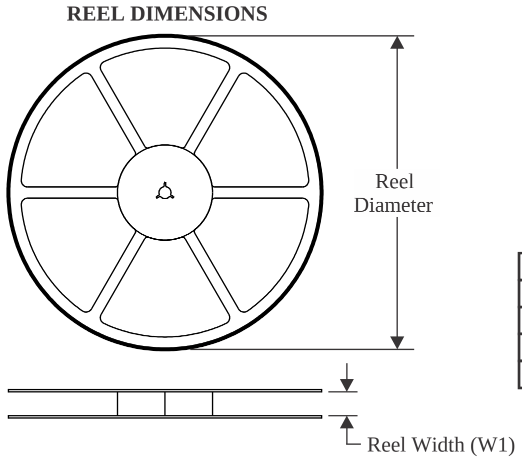
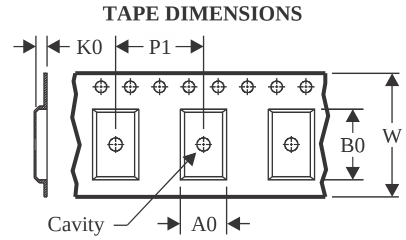
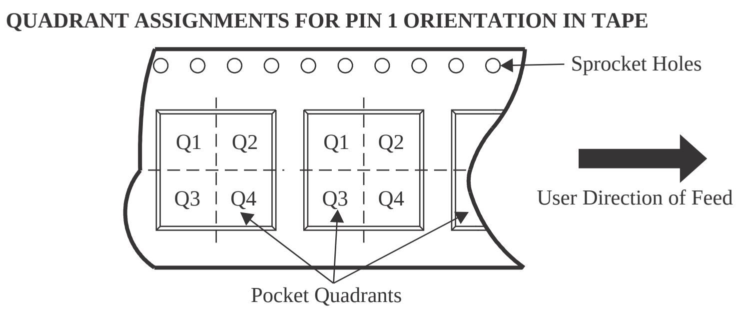
TAPE AND REEL INFORMATION





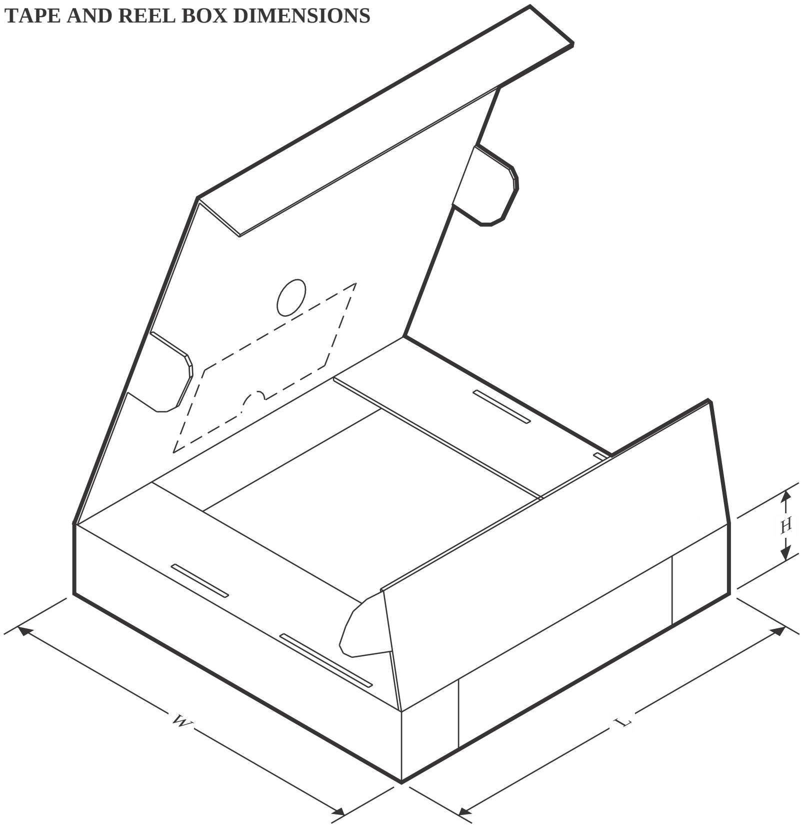
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2379IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV379IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV379IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV379IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV379IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV379IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV4379IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

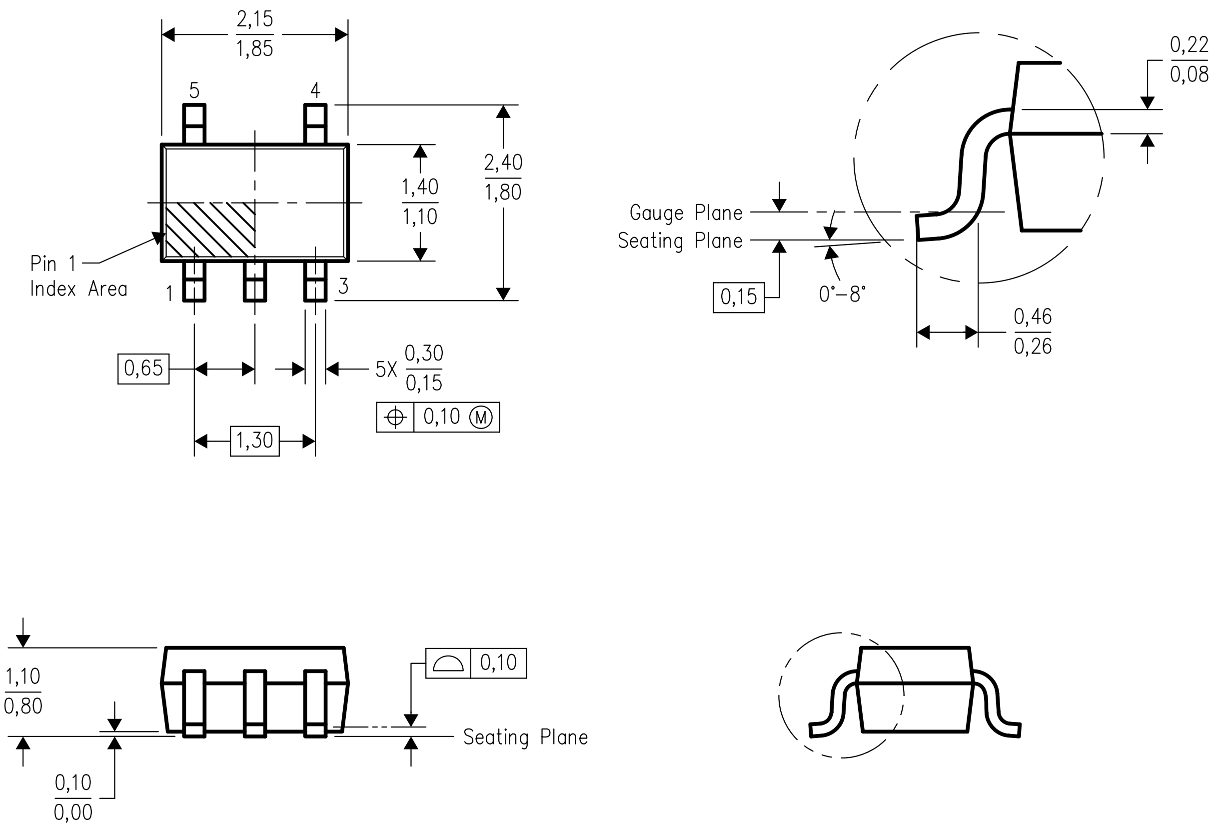
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2379IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV379IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV379IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV379IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV379IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV379IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV4379IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

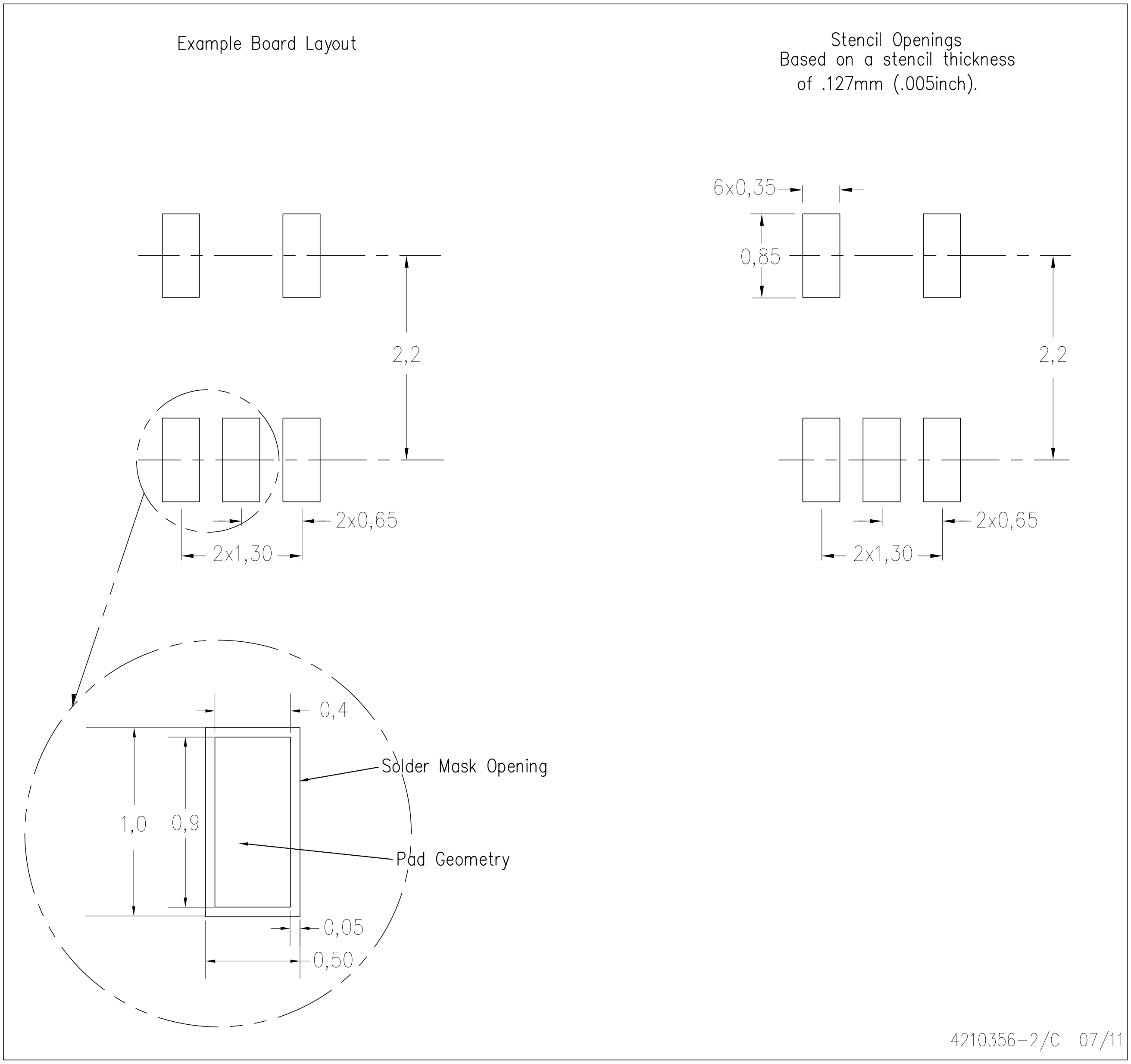
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

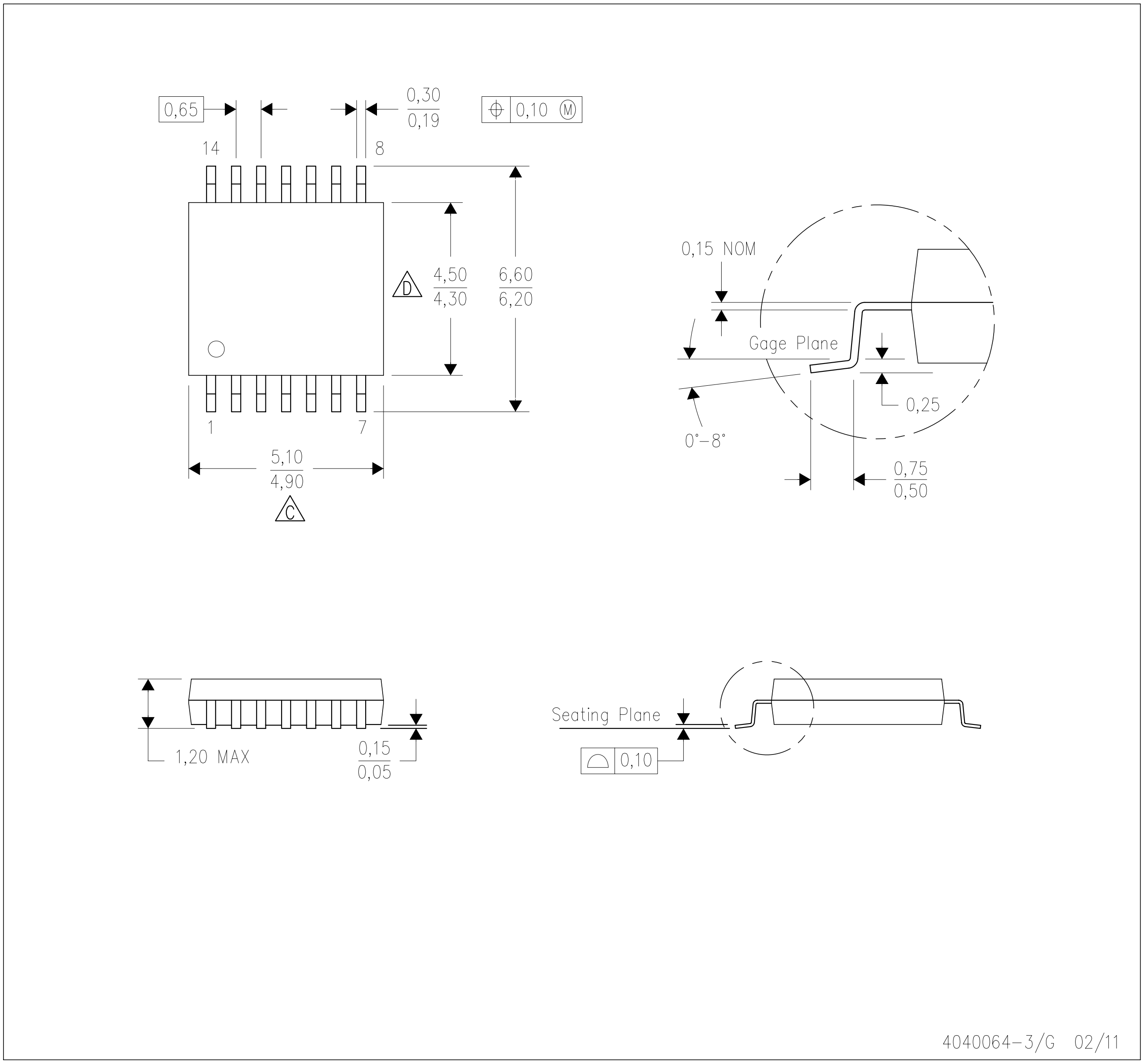
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



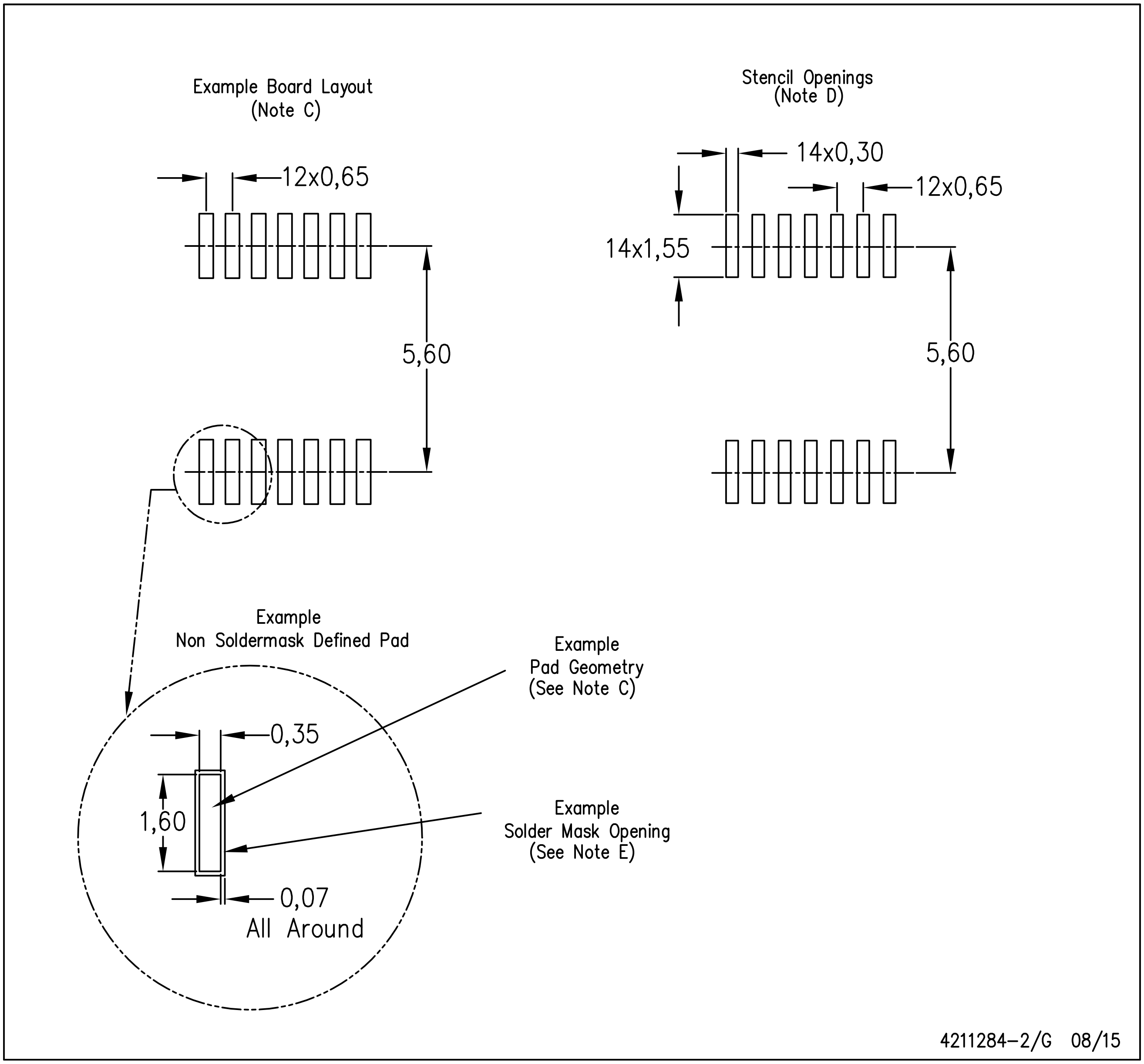
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE

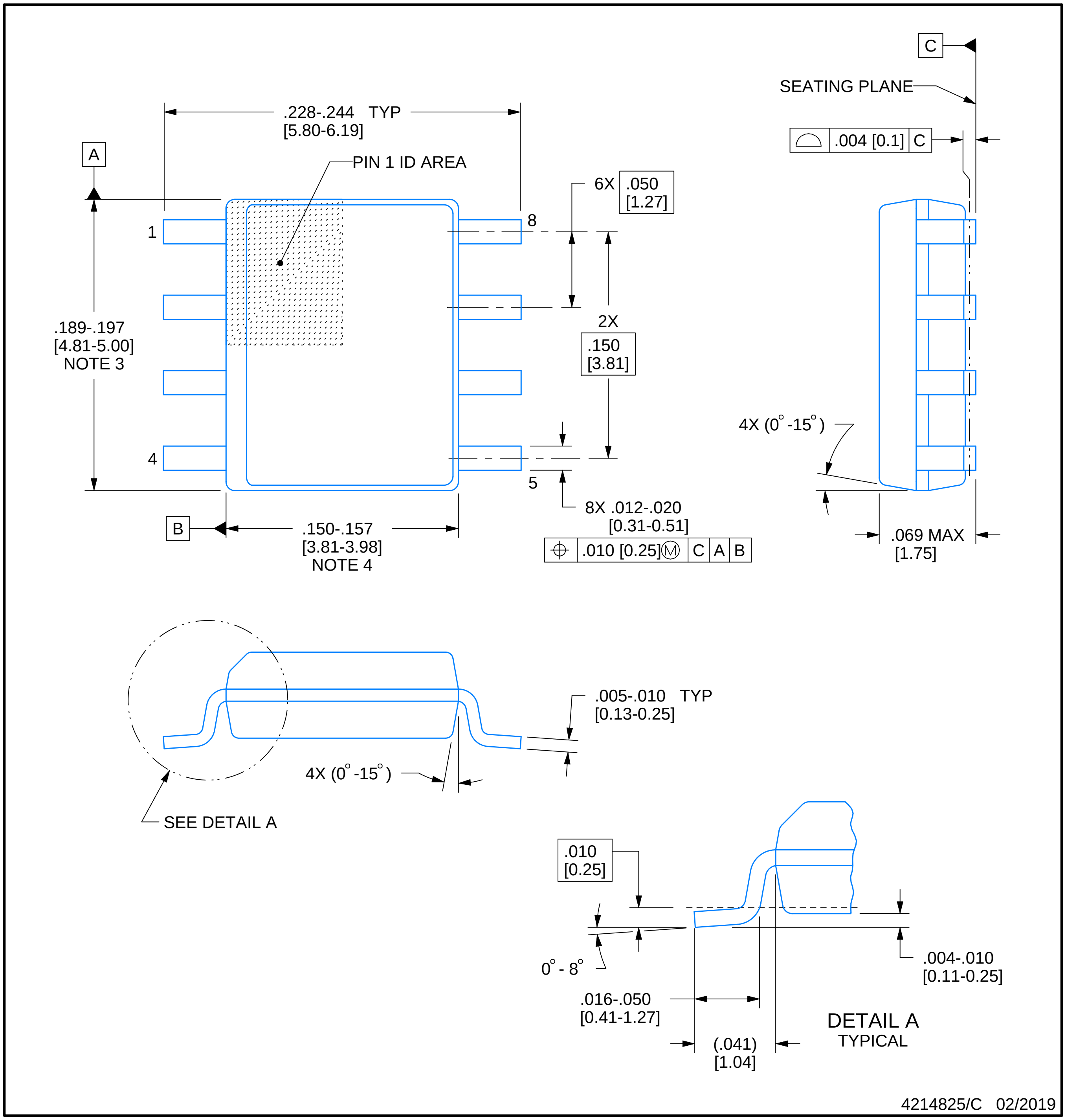


NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

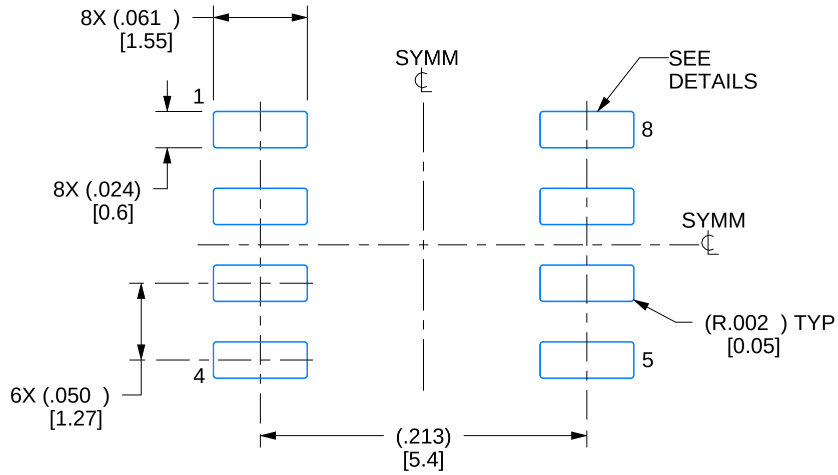


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

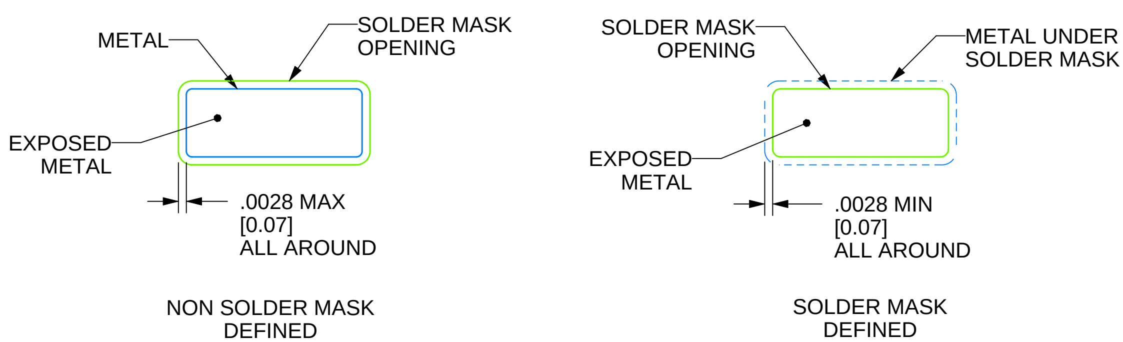


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

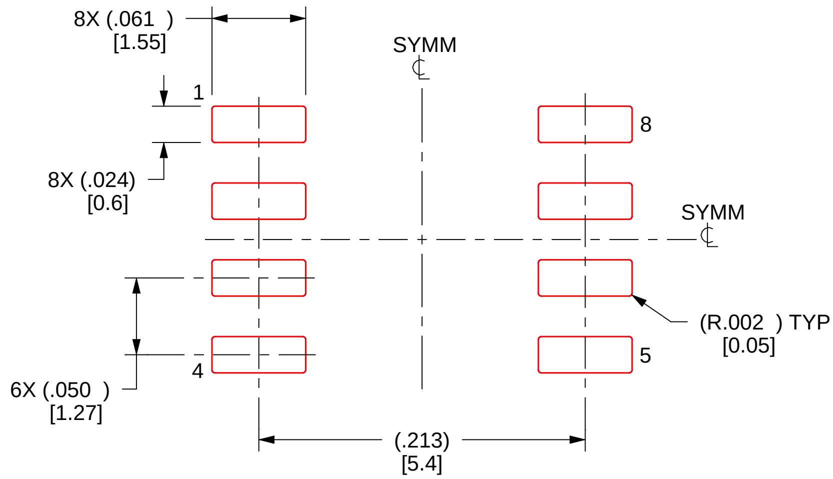


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

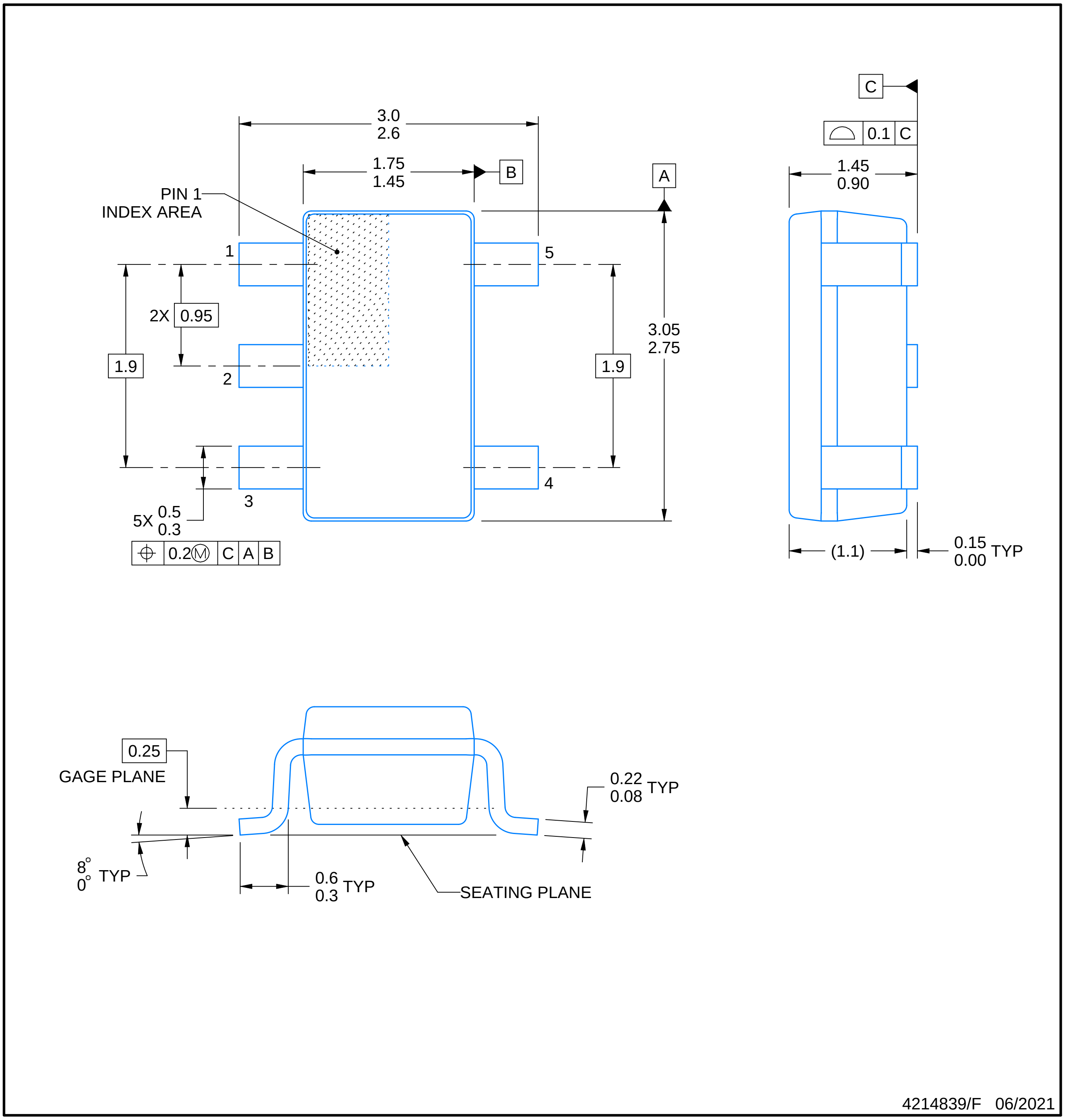
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

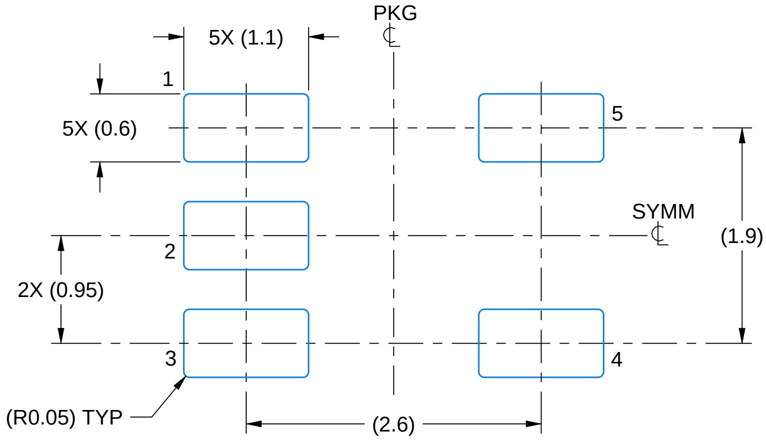
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

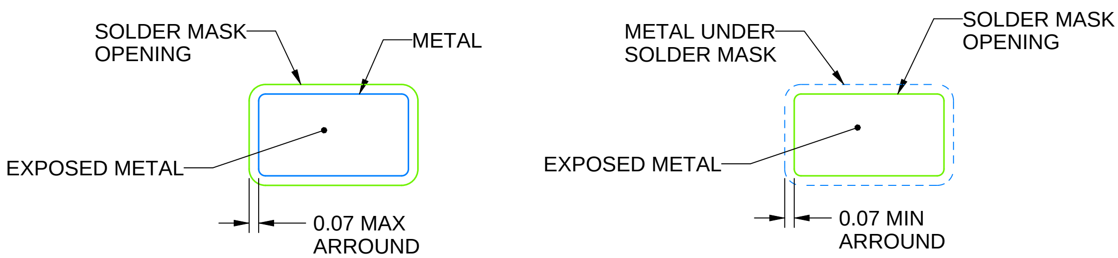


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

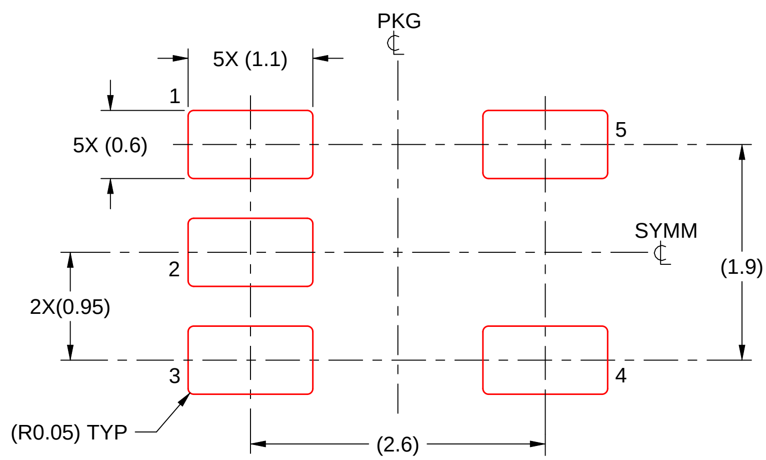
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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