QUAD PRECISION OPERATIONAL AMPLIFIER

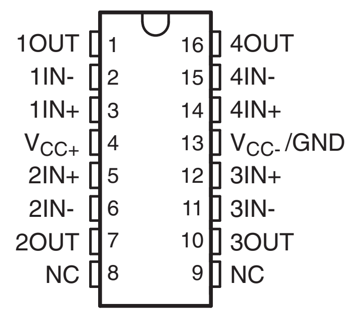
FEATURES

- Single-Supply Operation: Input Voltage Range Extends to Ground, and Output Swings to Ground While Sinking Current
- Input Offset Voltage 300 mV Max at 25°C
- Offset Voltage Temperature Coefficient 2.5 µV/°C Max
- Input Offset Current 1.5 nA Max at 25°C
- High Gain 1.2 V/µV Min (R_L = 2 kΩ), 0.5 V/µV Min (R_L = 600 Ω)
- Low Supply Current 2.2 mA Max at 25°C
- Low Peak-to-Peak Noise Voltage 0.55 µV Typ
- Low Current Noise 0.07 pA/$\sqrt{Hz}$ Typ

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C) Temperature Range[(1)]
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

DW PACKAGE
(TOP VIEW)



(1) Additional temperature ranges are available - contact factory

DESCRIPTION

The LT1014D is a quad precision operational amplifier with 14-pin industry-standard configuration. It features low offset-voltage temperature coefficient, high gain, low supply current, and low noise.

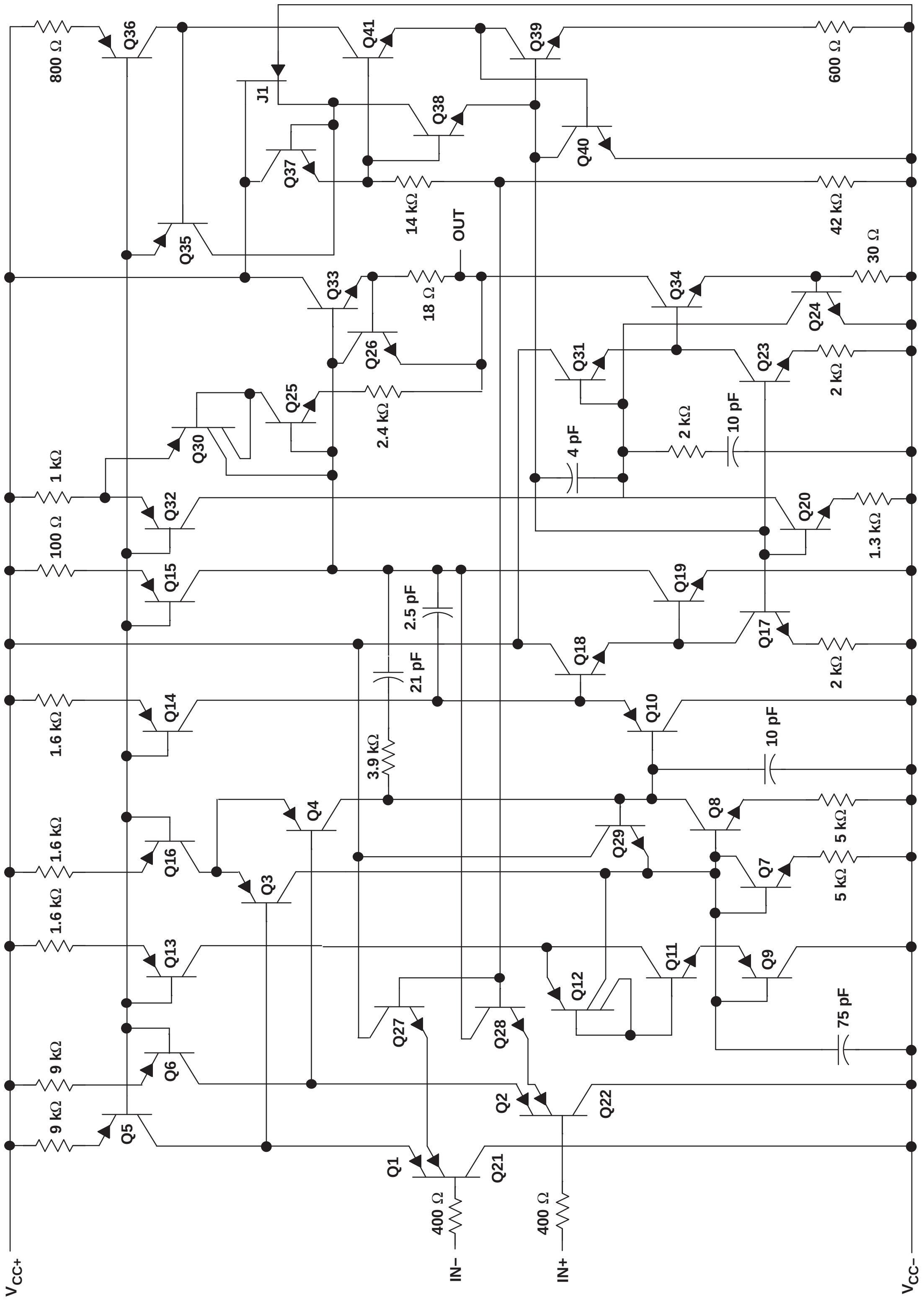
The LT1014D can be operated with both dual ±15-V and single 5-V power supplies. The common-mode input voltage range includes ground, and the output voltage can also swing to within a few milivolts of ground. Crossover distortion is eliminated.

ORDERING INFORMATION[(1)]

T_A	PACKAGE[(2)]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SIOC-DW	Reel of 2000	LT1014DMDWREP	LT1014DMEP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SCHEMATIC (EACH AMPLIFIER)



Component values are nominal.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	supply voltage (2)		–22	22	V
	Differential input voltage (3)		–30	30	V
V_I	Input voltage range (any input) (2)		V_{CC-} – 5	V_{CC+}	V
	Duration of short-circuit current (4)	T_A ≤ 25°C	Unlimited		
	Continuous total power dissipation		See Dissipation Ratings Table		
T_A	Operating temperature range		–55	125	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1,6 mm, at distance 1/16 inch from case for 10s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at the noninverting input with respect to the inverting input.
(4) The output may be shorted to either supply.

DISSIPATION RATINGS

PACKAGE	T_A ≤ 25°c POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 105°C POWER RATING	T_A = 125°C POWER RATING
DW	1025 mV	8.2 mW/°C	656 mW	369 mW	205 mW

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450	µV
			Full range		400	1500	
		R_S = 50 Ω, V_{IC} = 0.1 V	125°C		200	750	
I_{IO}	Input offset current		25°C		0.2	2	nA
			Full range			10	
I_{IB}	Input bias current		25°C		-15	-50	nA
			Full range			-120	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	-0.3 to 3.8		V
			Full range	0.1 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, no load	25°C		15	25	mV
		Ouput low, R_L = 600 Ω to GND	25°C		5	10	
			Full range			18	
		Output low, I_{SINK} = 1 mA	25°C		220	350	
		Output high, no load	25°C	4	4.4		V
		Output high	25°C	3.4	4		
		R_L = 600 Ω to GND	Full range	3.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1		V/µV
I_{CC}	Supply current per amplifier		25°C		0.3	0.5	mA
			Full range			0.65	

(1) Full range is -55°C to 125°C.

OPERATING CHARACTERISTICS

over operating free-air temperature range, $V_{CC\pm}$ = 15 V, V_{IC} = 0, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage vs balanced source resistance		Figure 2
V_{IO}	Input offset voltage vs free-air temperature		Figure 3
ΔV_{IO}	Warm-up change in input offset voltage vs elapsed time		Figure 4
I_{IO}	Input offset current vs Input offset current vs free-air temperature		Figure 5
I_{IB}	Input bias current vs free-air temperature		Figure 6
V_{IC}	Common-mode input voltage vs input bias current		Figure 7
A_{VD}	Differential voltage amplification	vs load resistance	Figure 8 Figure 9
		vs frequency	Figure 10 Figure 11
	Channel separation vs frequency		Figure 12
	Output saturation voltage vs free-air temperature		Figure 13
CMRR	Common-mode rejection ratio vs frequency		Figure 14
k_{SVR}	Supply-voltage rejection ratio vs frequency		Figure 15
I_{CC}	Supply current vs free-air temperature		Figure 16
I_{OS}	Short-circuit output current vs elapsed time		Figure 17
V_n	Equivalent input noise voltage vs frequency		Figure 18
I_n	Equivalent input noise current vs frequency		Figure 18
$V_{N(PP)}$	Peak-to-peak input noise voltage vs time		Figure 19
	Pulse response (small signal) vs time		Figure 20 Figure 22
	Pulse response (large signal) vs time		Figure 21 Figure 23 Figure 24
	Phase shift vs frequency		Figure 10

INPUT OFFSET VOLTAGE
vs
BALANCED SOURCE RESISTANCE

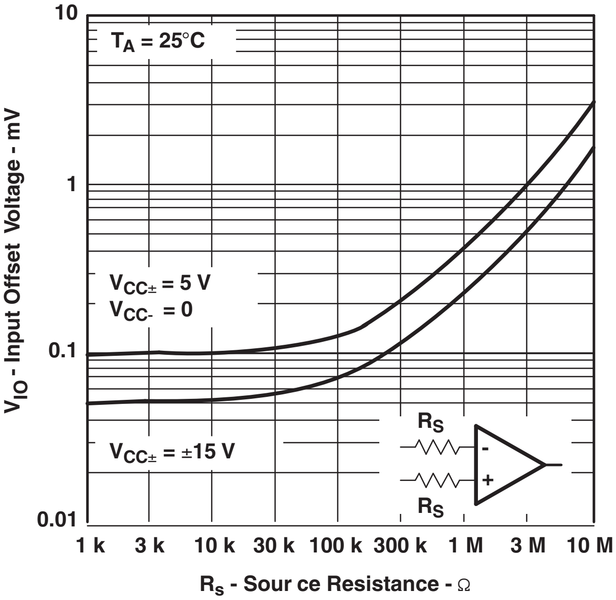


Figure 2.

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

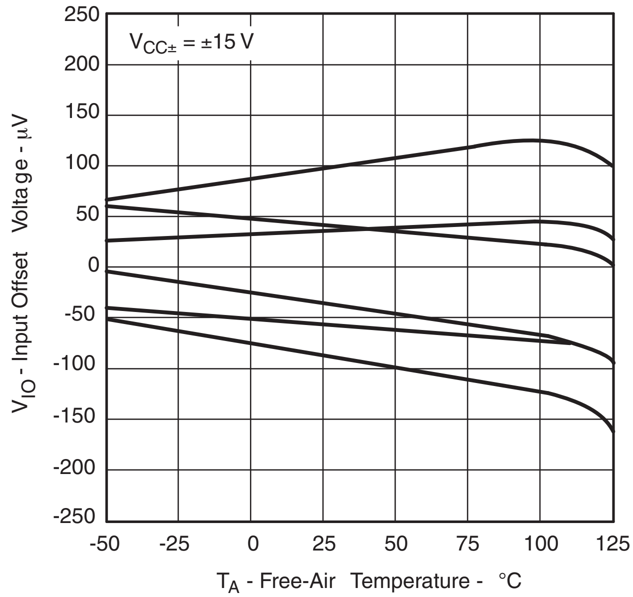


Figure 3.

WARM-UP CHANGE IN INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

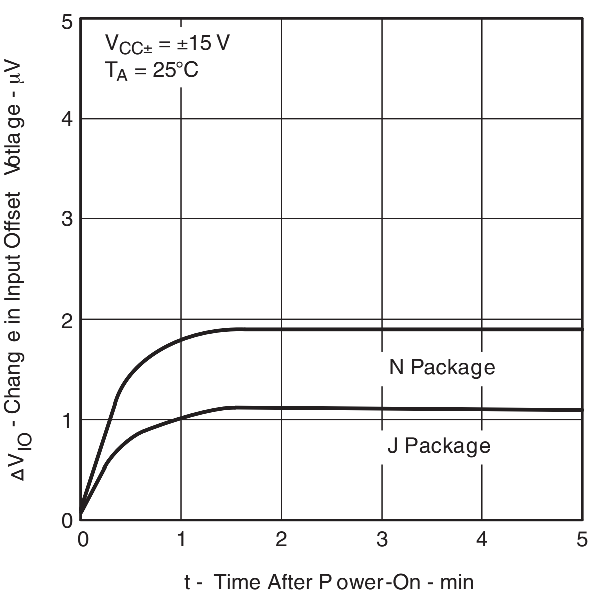


Figure 4.

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

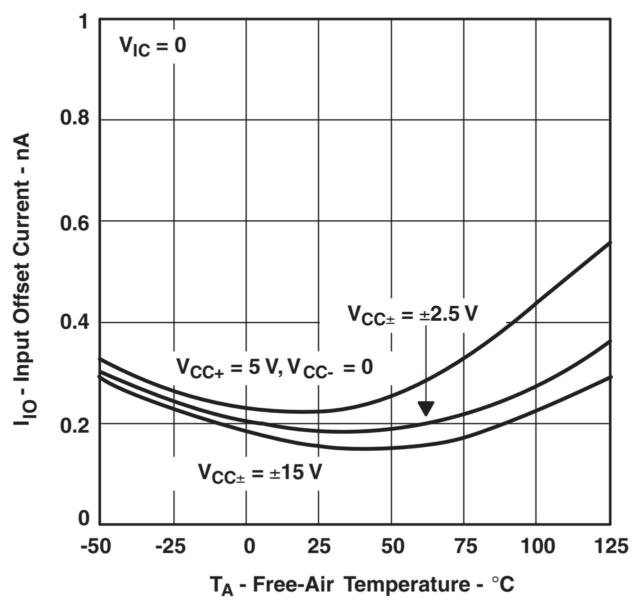


Figure 5.

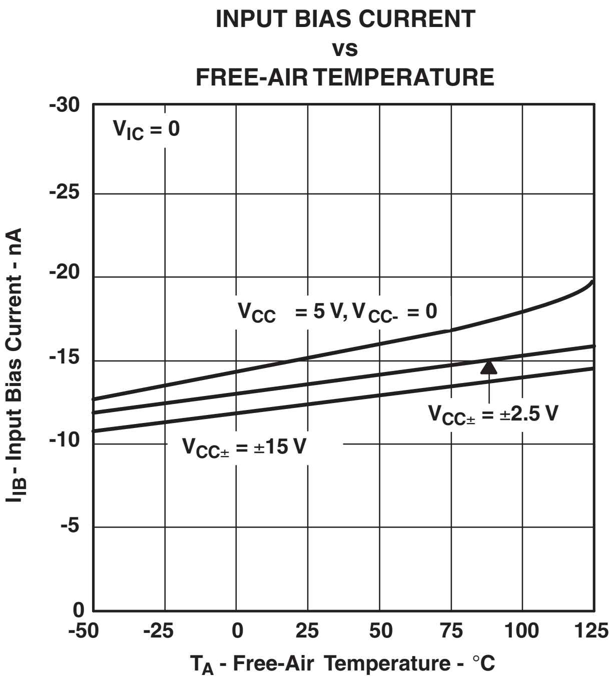


Figure 6.

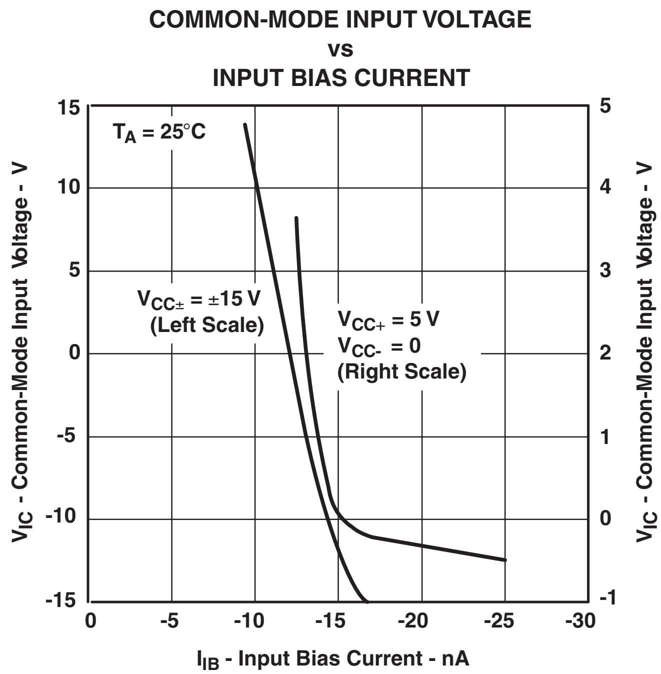


Figure 7.

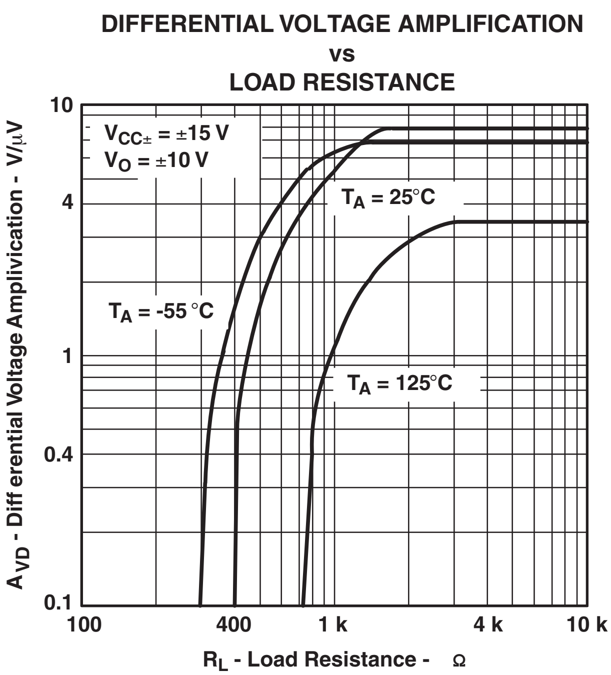


Figure 8.

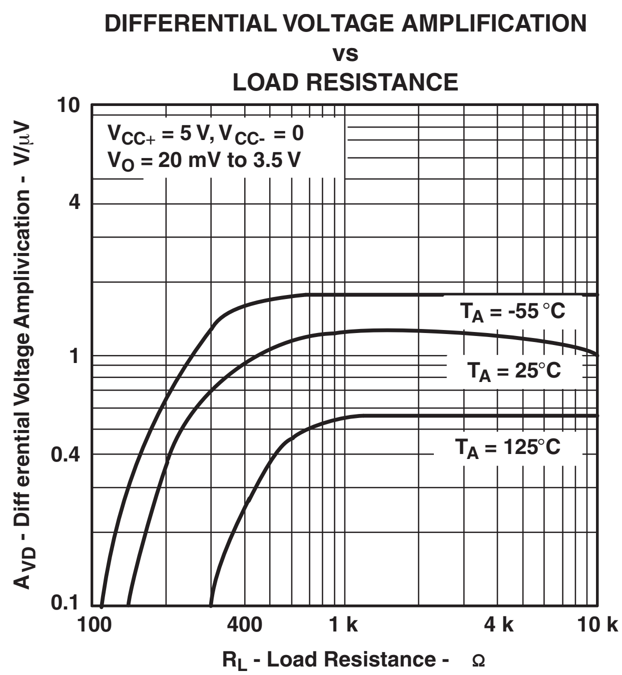


Figure 9.

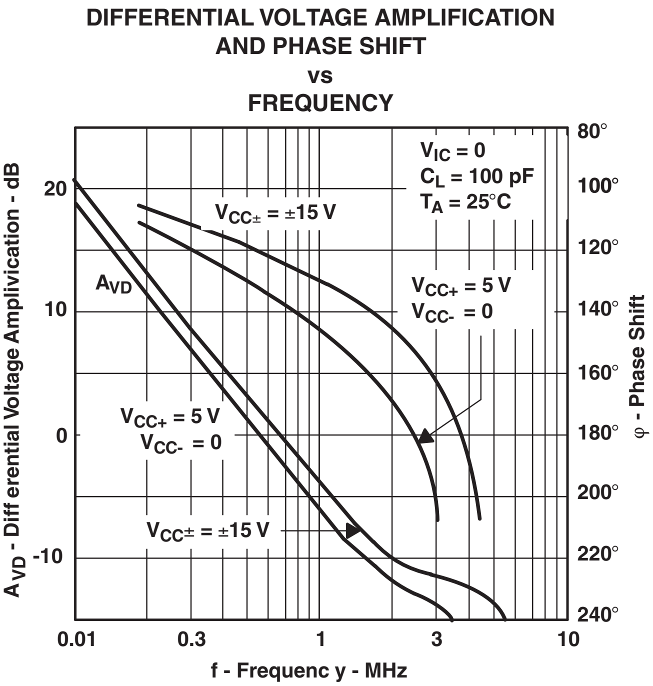


Figure 10.

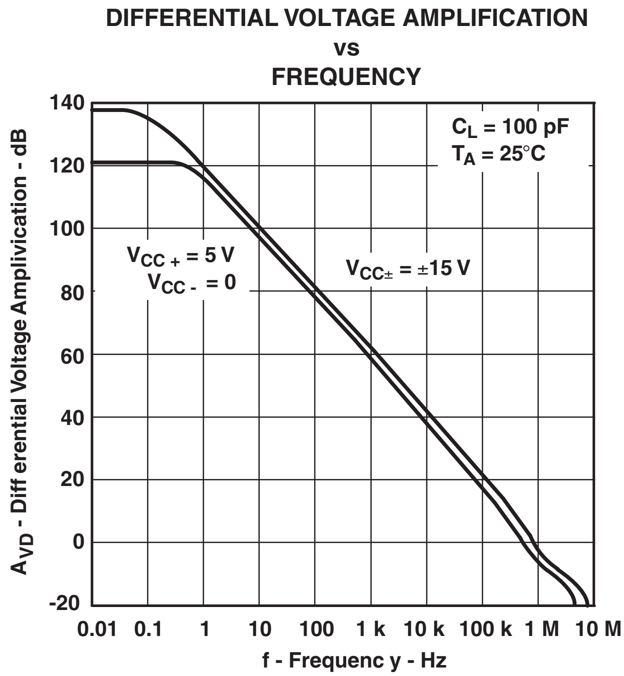


Figure 11.

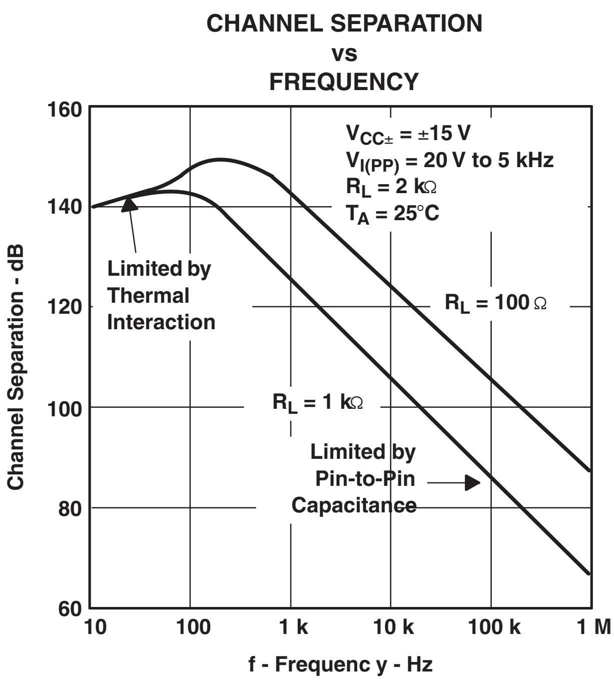


Figure 12.

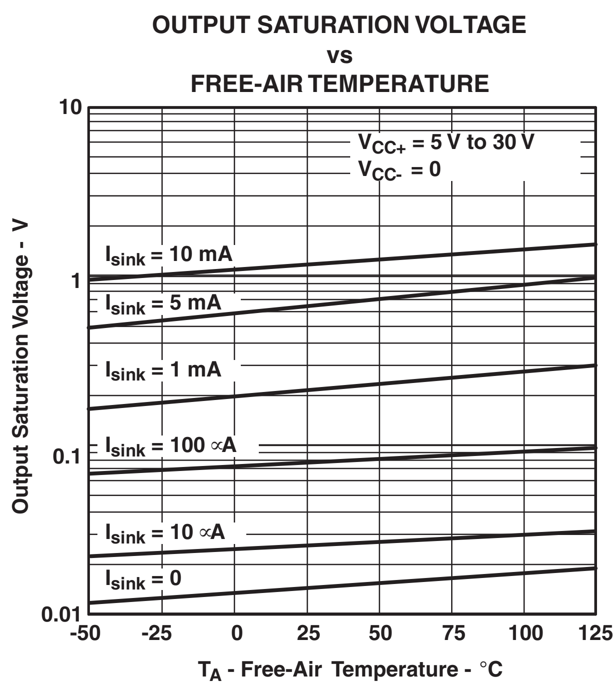


Figure 13.

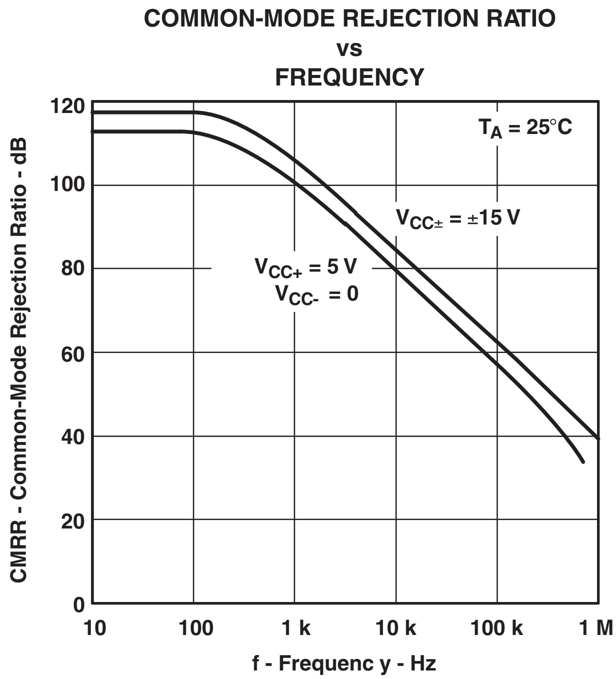


Figure 14.

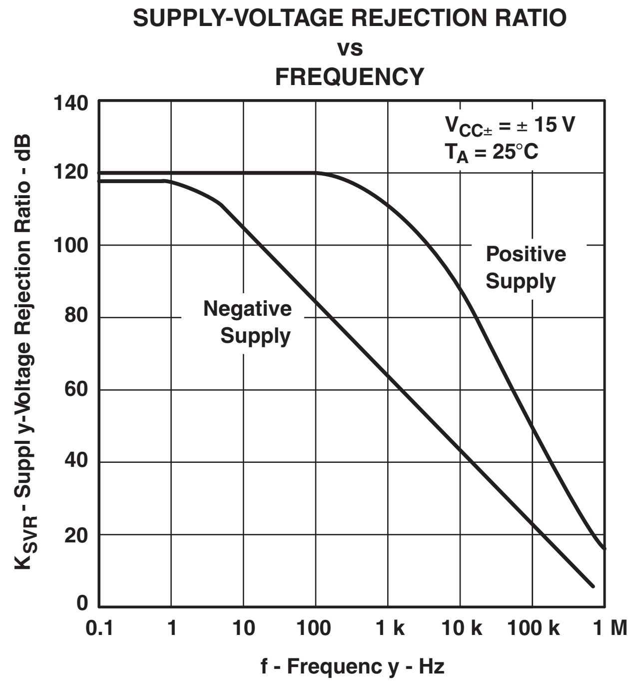


Figure 15.

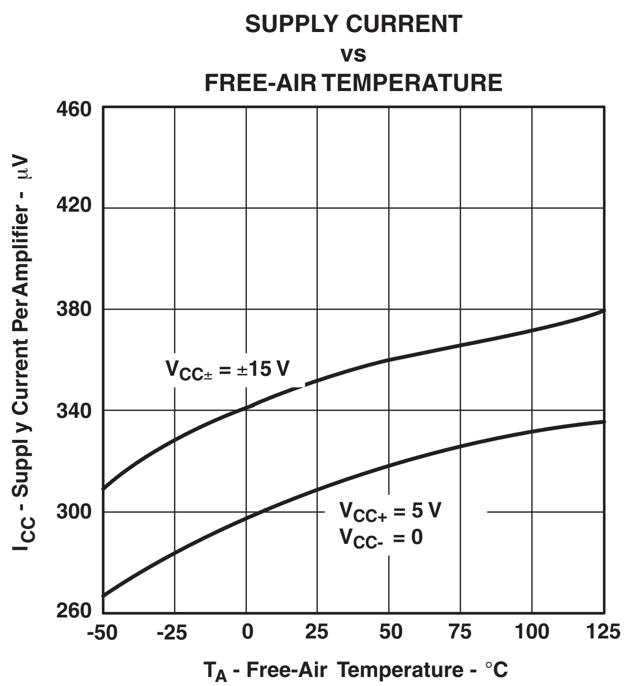


Figure 16.

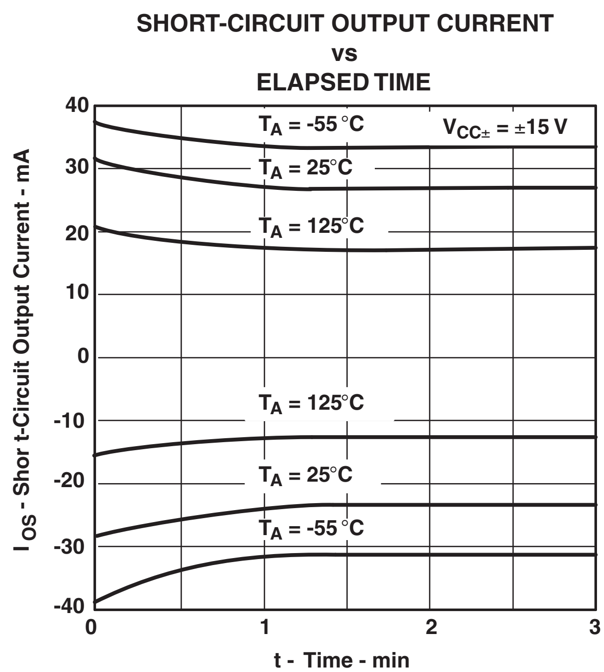


Figure 17.

EQUIVALENT INPUT NOISE VOLTAGE AND EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

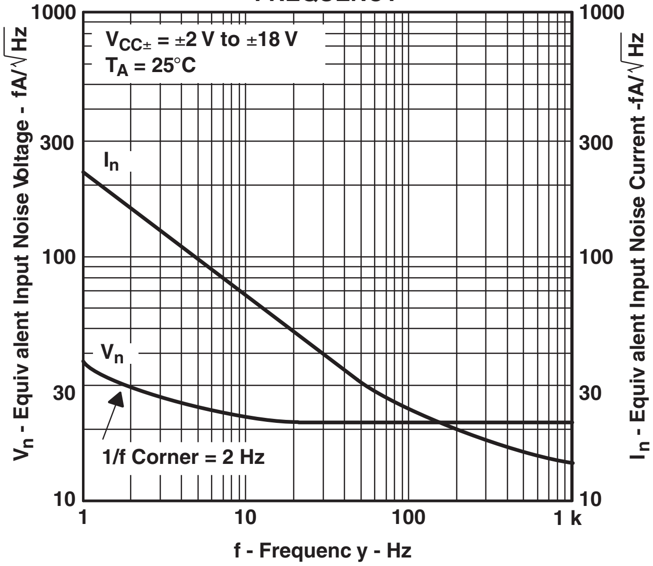


Figure 18.

PEAK-TO-PEAK INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD vs TIME

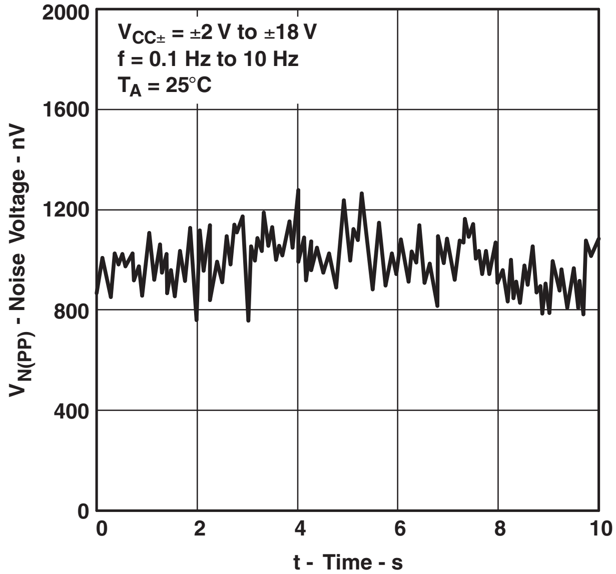


Figure 19.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE vs TIME

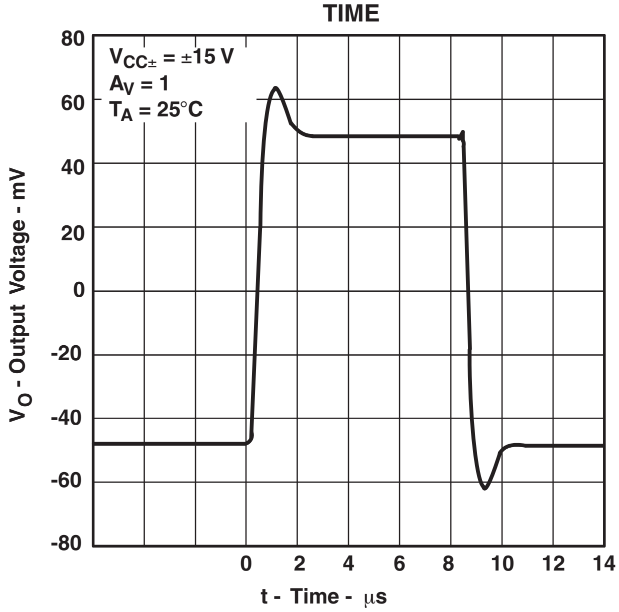


Figure 20.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE vs TIME

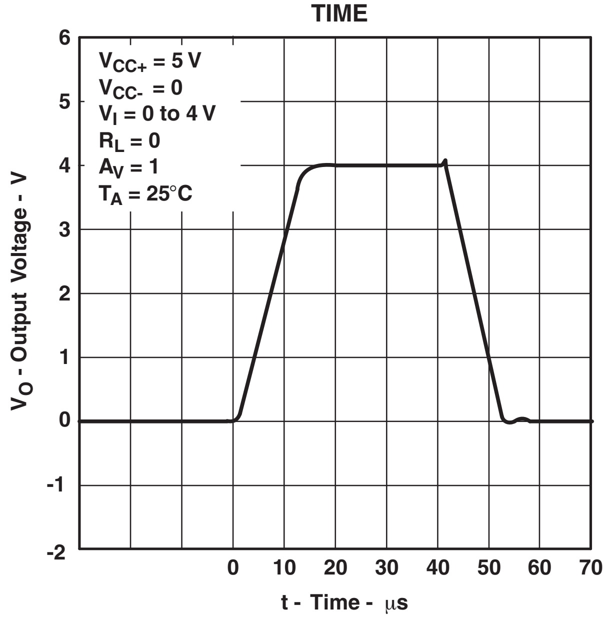


Figure 21.

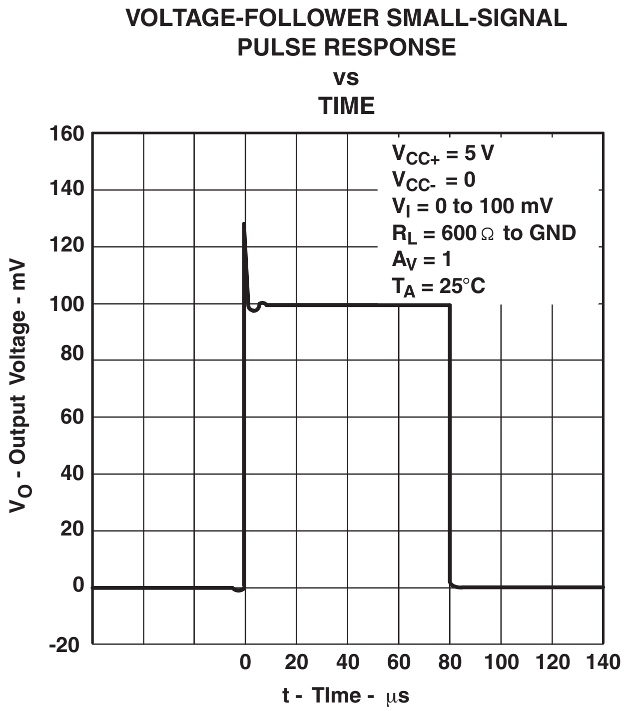


Figure 22.

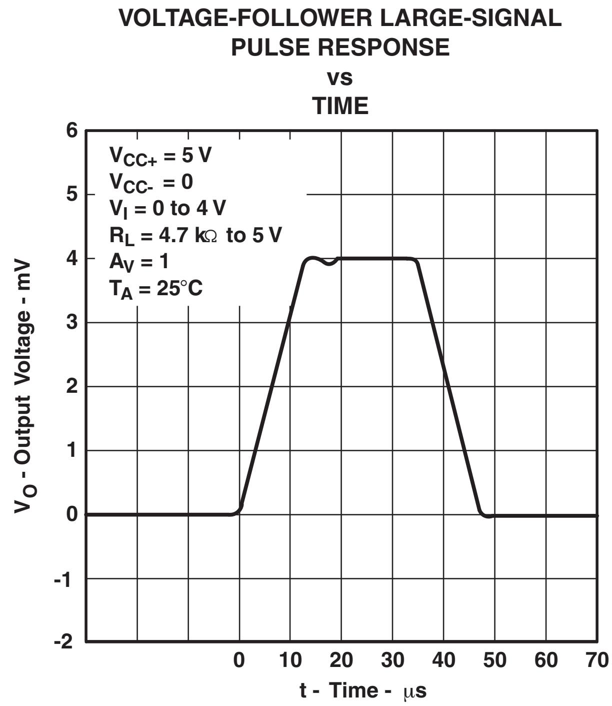


Figure 23.

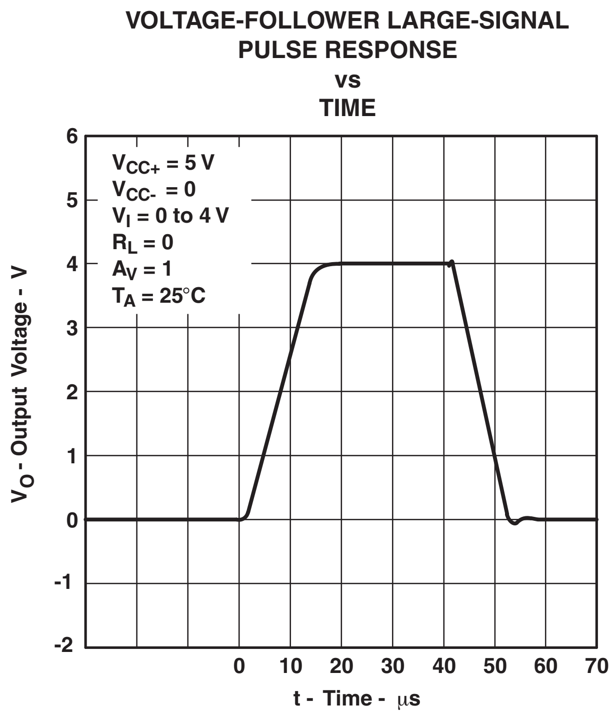


Figure 24.

APPLICATION INFORMATION

SINGLE-SUPPLY OPERATION

The LT1014D is fully specified for single-supply operation (V_{CC-} = 0). The common-mode input voltage range includes ground, and the output swings within a few millivolts of ground.

Furthermore, the LT1014D has specific circuitry that addresses the difficulties of single-supply operation, both at the input and at the output. At the input, the driving signal can fall below 0 V, either inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, the LT1014D is designed to deal with the following two problems that can occur:

1. On many other operational amplifiers, when the input is more than a diode drop below ground, unlimited current flows from the substrate (V_{CC-} terminal) to the input, which can destroy the unit. On the LT1014D, the 400-Ω resistors in series with the input (see schematic) protect the device even when the input is 5 V below ground.
2. When the input is more than 400 mV below ground (at T_A = 25°C), the input stage of similar type operational amplifiers saturates, and phase reversal occurs at the output. This can cause lockup in servo systems. Because of unique phase-reversal protection circuitry (Q21, Q22, Q27, and Q28), the LT1014D outputs do not reverse, even when the inputs are at -1.5 V (see Figure 25).

However, this phase-reversal protection circuitry does not function when the other operational amplifier on the LT1014D is driven hard into negative saturation at the output. Phase-reversal protection does not work on an amplifier:

- When 4's output is in negative saturation (the outputs of 2 and 3 have no effect)
- When 3's output is in negative saturation (the outputs of 1 and 4 have no effect)
- When 2's output is in negative saturation (the outputs of 1 and 4 have no effect)
- When 1's output is in negative saturation (the outputs of 2 and 3 have no effect)

At the output, other single-supply designs either cannot swing to within 600 mV of ground or cannot sink more than a few microproamperes while swinging to ground. The all-npn output stage of the LT1014D maintains its low output resistance and high gain characteristics until the output is saturated. In dual-supply operations, the output stage is free of crossover distortion.

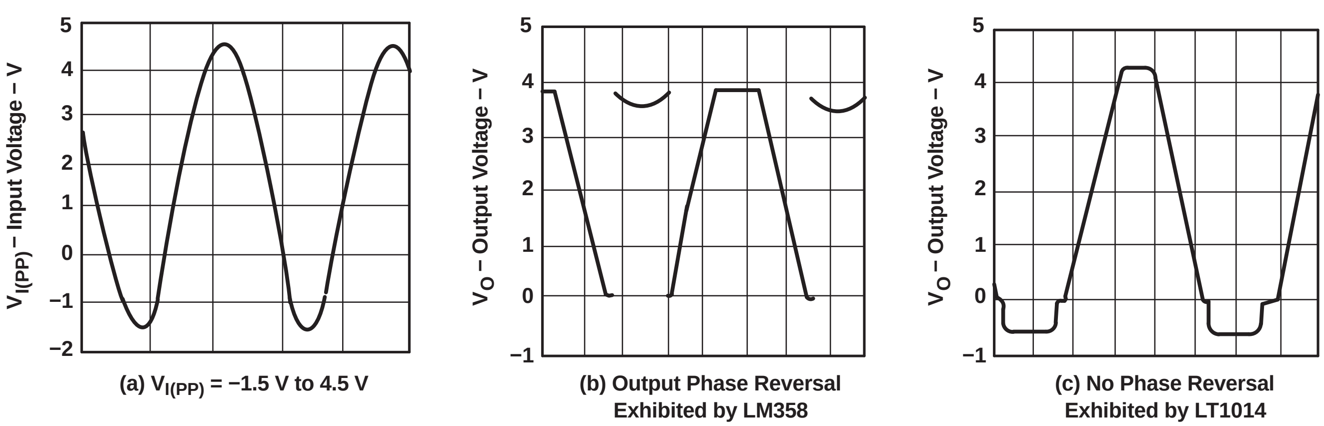


Figure 25. Voltage-Follower Response With Input Exceeding the Negative Common-Mode Input Voltage Range

COMPARATOR APPLICATIONS

The single-supply operation of the LT1014D can be used as a precision comparator with TTL-compatible output. In systems using both operational amplifiers and comparators, the LT1014D can perform multiple duties (see Figure 26 and Figure 27).

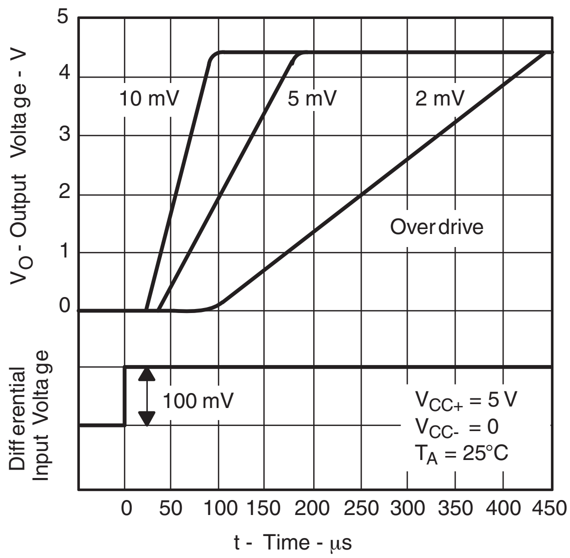


Figure 26. Low-to-High-Level Output Response for Various Input Overdrives

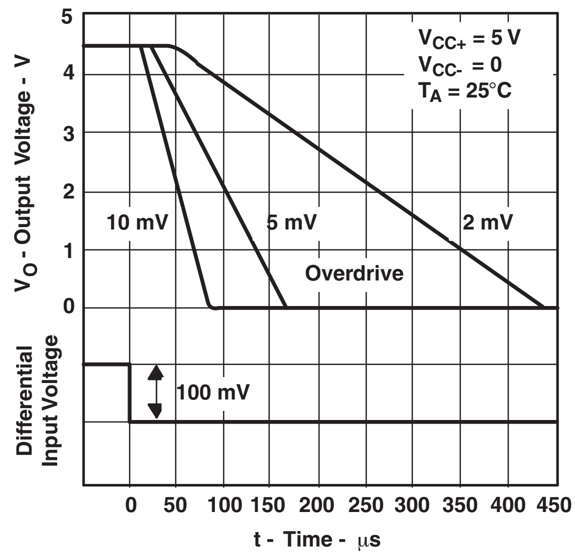


Figure 27. High-to-Low-Level Output Response for Various Input Overdrives

LOW-SUPPLY OPERATION

The minimum supply voltage for proper operation of the LT1014D is 3.4 V (three Ni-Cad batteries). Typical supply current at this voltage is 290 µA; therefore, power dissipation is only 1 mW per amplifier.

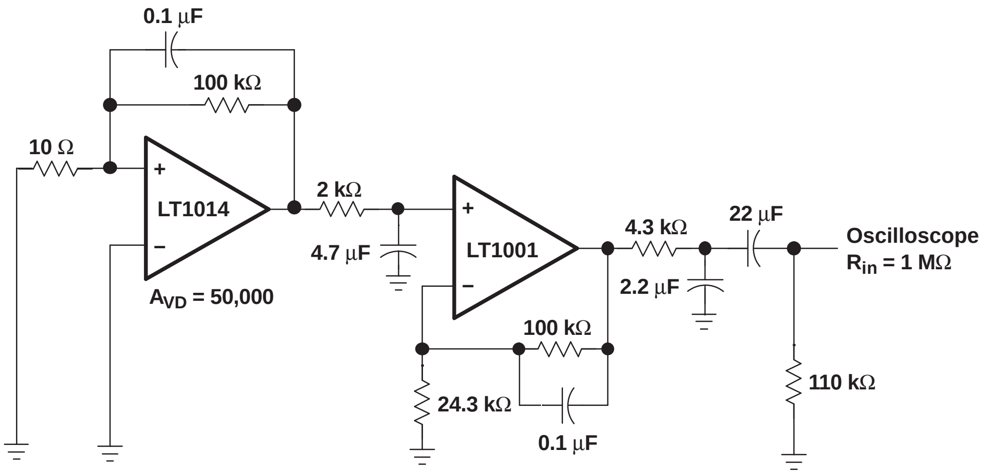
OFFSET VOLTAGE AND NOISE TESTING

Figure 31shows the test circuit for measuring input offset voltage and its temperature coefficient. This circuit with supply voltages increased to ±20 V is also used as the burn-in configuration.

The peak-to-peak equivalent input noise voltage of the LT1014D is measured using the test circuit shown in Figure 28. The frequency response of the noise tester indicates that the 0.1-Hz corner is defined by only one zero. The test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contribution from the frequency band below 0.1 Hz.

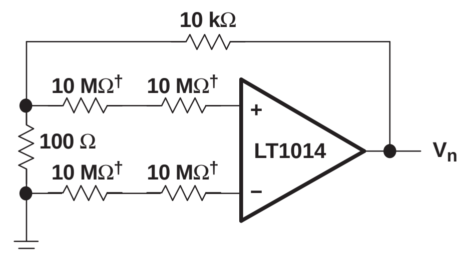
An input noise-voltage test is recommended when measuring the noise of a large number of units. A 10-Hz input noise-voltage measurement correlates well with a 0.1-Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.

Noise current is measured by the circuit and formula shown in Figure 29. The noise of the source resistors is subtracted.



NOTE A: All capacitor values are for nonpolarized capacitors only.

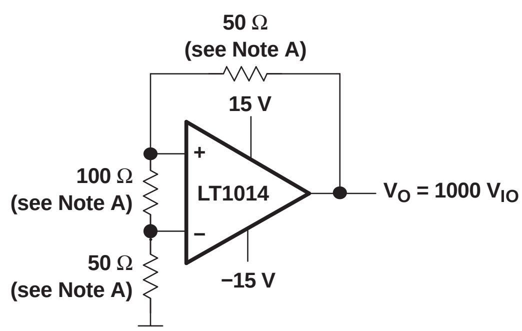
Figure 28. 0.1-Hz to 10-Hz Peak-to-Peak Noise Test Circuit



$$I_n = \frac{\left[V_{no}{}^2 - (820\ \text{nV})^2\right]^{1/2}}{40\ \text{M}\Omega \times 100}$$

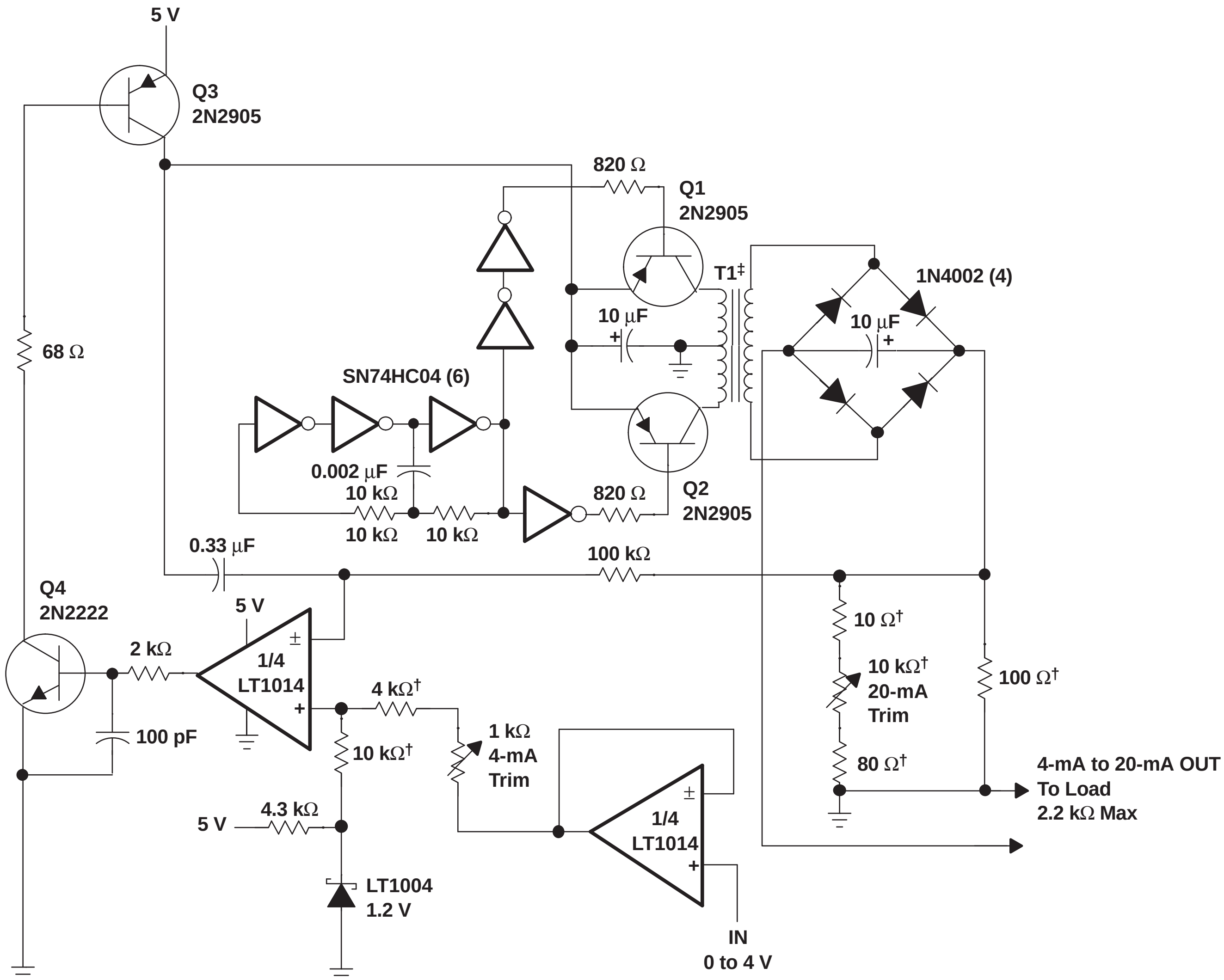
† Metal-film resistor

Figure 29. Noise-Current Test Circuit and Formula



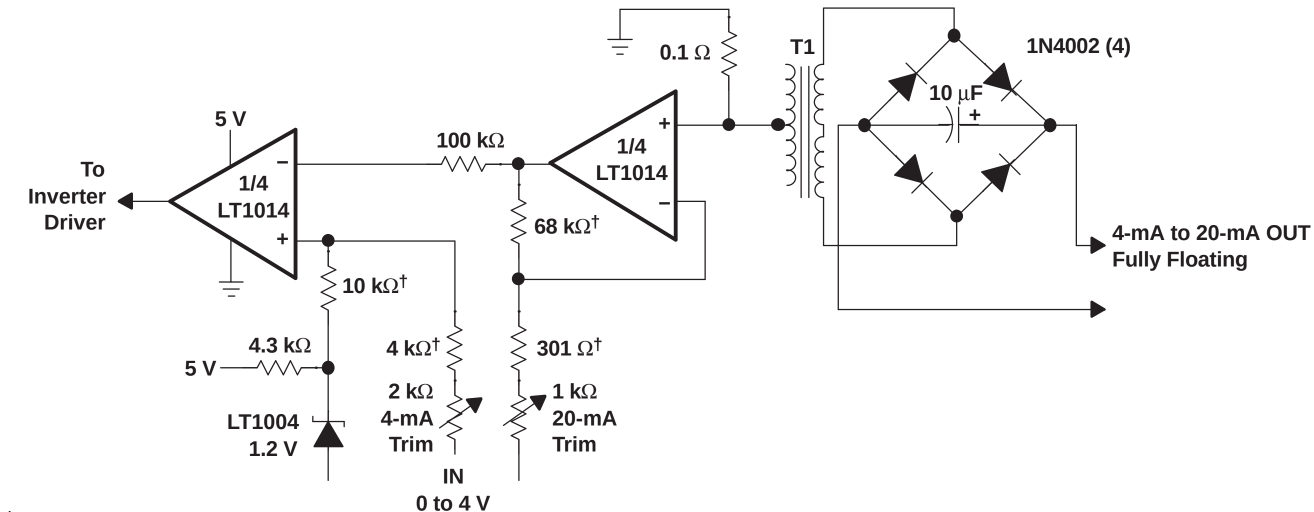
NOTE A: Resistors must have low thermoelectric potential.

Figure 30. Test Circuit for V_{IO} and αV_{IO}



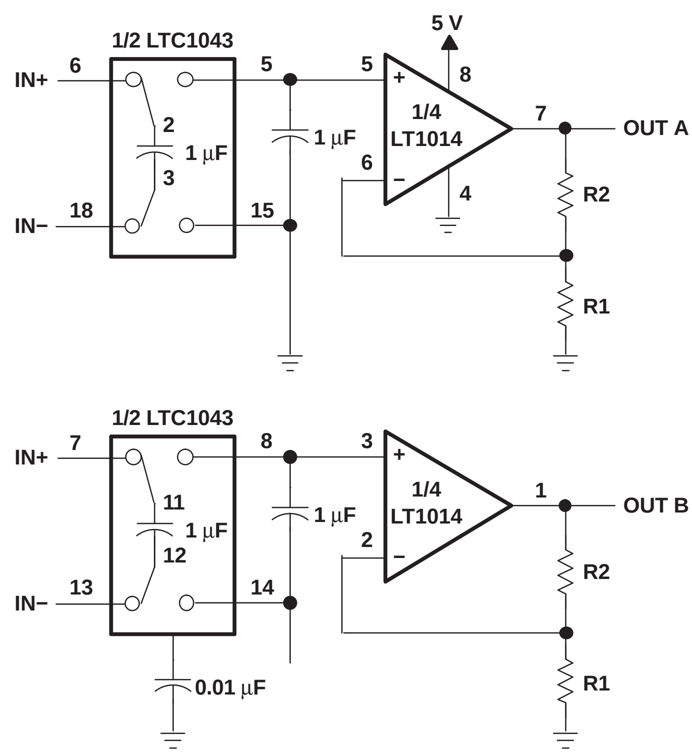
† 1% film resistor. Match 10-kΩ resistors 0.05%.
‡ T1 = PICO-31080

Figure 31. 5-V Powered, 4-mA to 20-mA Current-Loop Transmitter With 12-Bit Accuracy



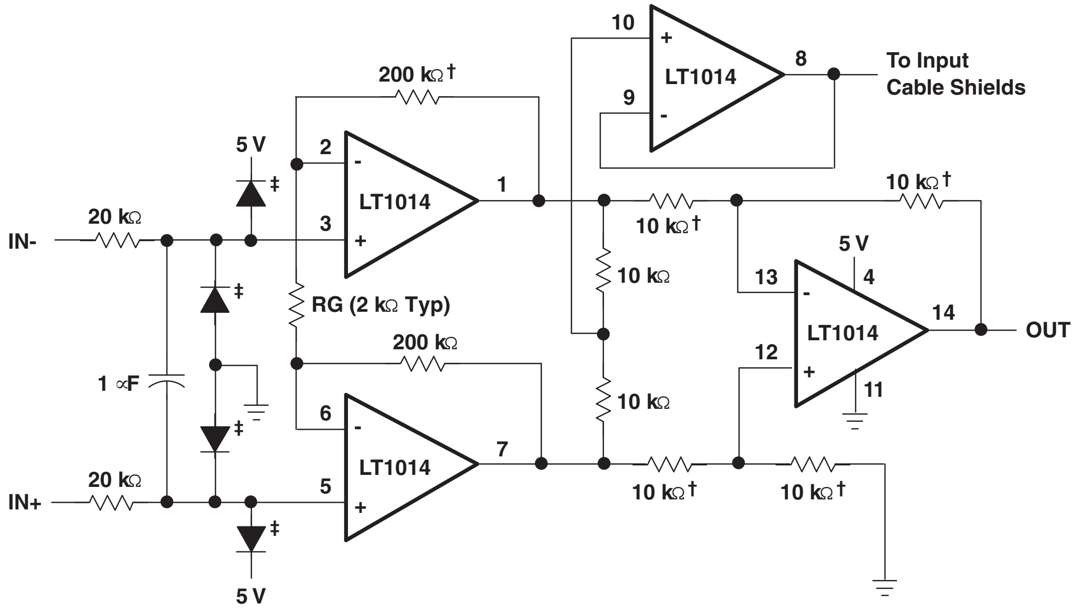
† 1% film resistor

Figure 32. Fully Floating Modification to 4-mA to 20-mA Current-Loop Transmitter With 8-Bit Accuracy



NOTE A: V_{IO} = 150 µV, A_{VD} = (R1/R2) + 1, CMRR = 120 dB, V_{ICR} = 0 to 5 V

Figure 33. 5-V Single-Supply Dual Instrumentation Amplifier



† 1% film resistor. Match 10-kΩ resistors 0.05%.
‡ For high source impedances, use 2N2222 as diodes (with collector connected to base).
NOTE A: A_{VD} = (400,000/RG) + 1

Figure 34. 5-V Powered Precision Instrumentation Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LT1014DMDWREP	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LT1014DMEP	Samples
V62/09614-01XE	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LT1014DMEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LT1014D-EP :

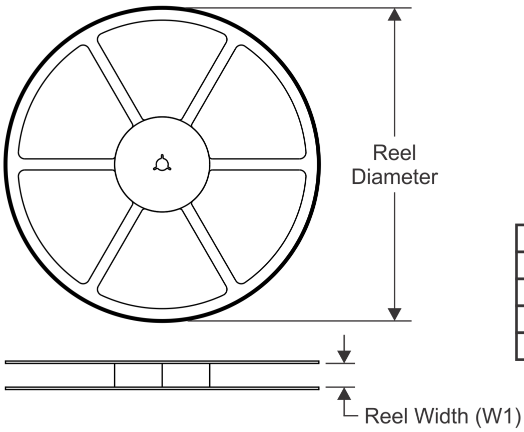
- Catalog: LT1014D

NOTE: Qualified Version Definitions:

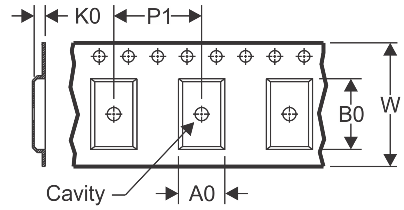
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

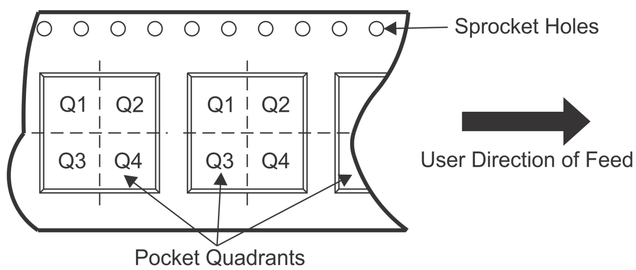


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

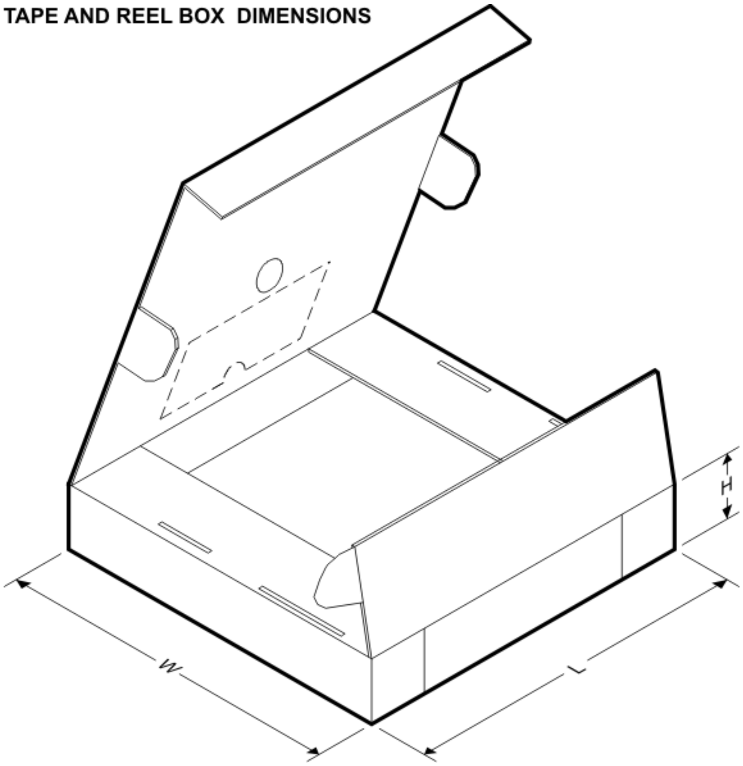
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1014DMDWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

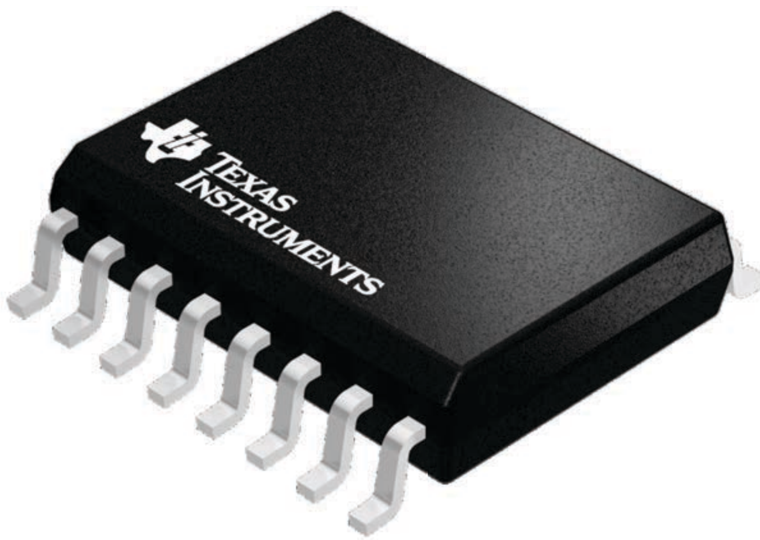
TAPE AND REEL BOX DIMENSIONS

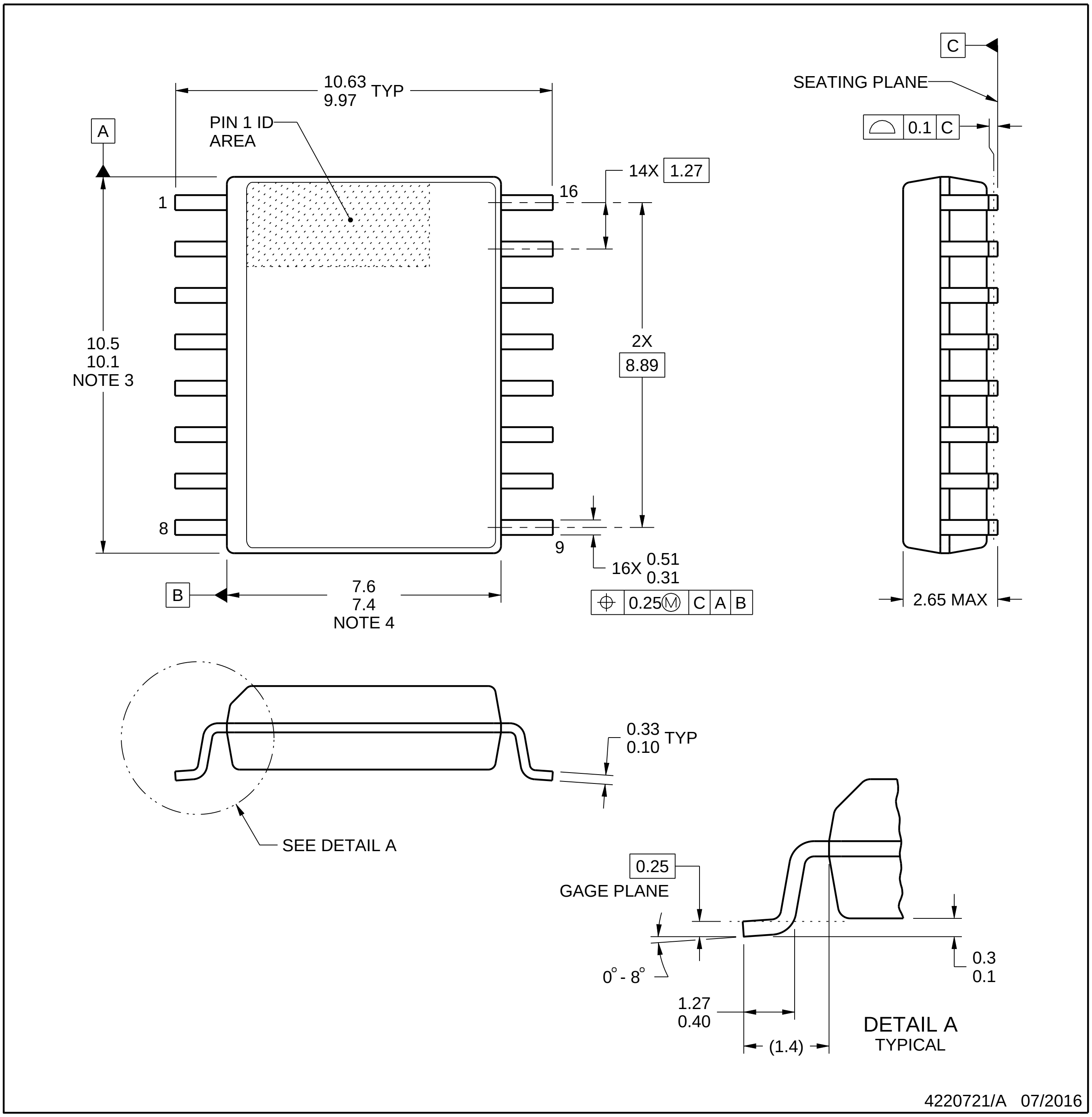


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1014DMDWREP	SOIC	DW	16	2000	350.0	350.0	43.0

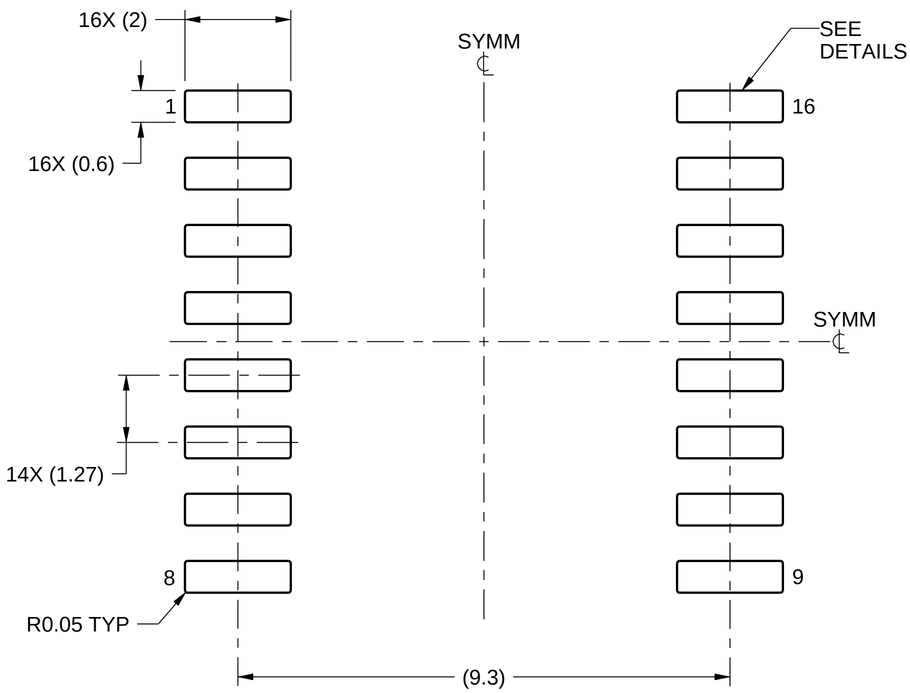
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



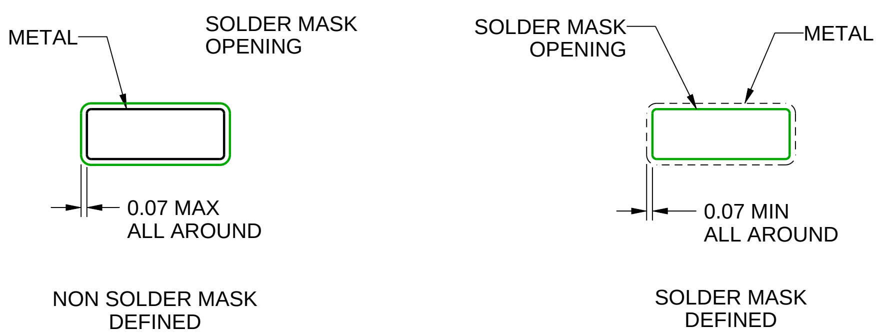


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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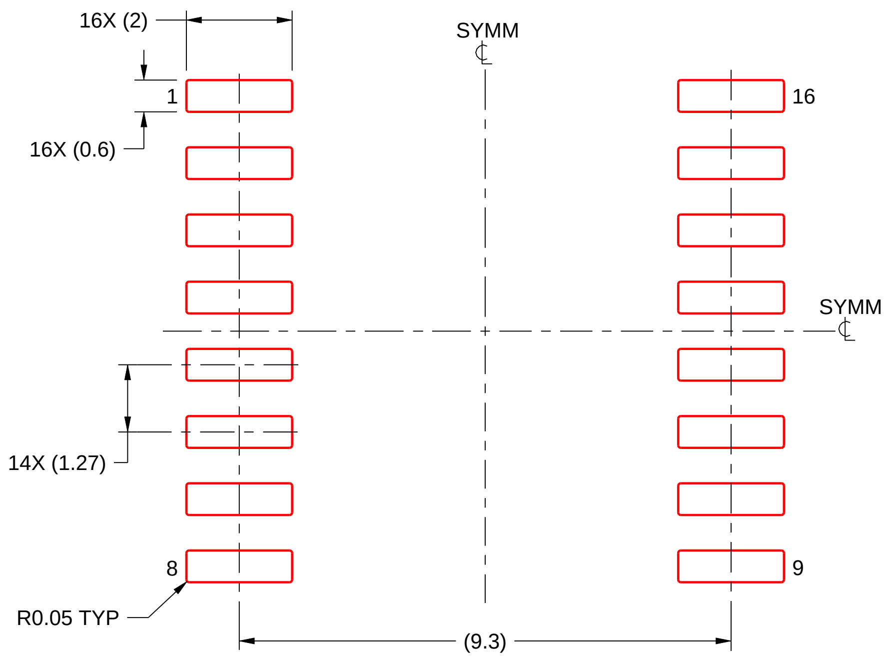
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.