

## LMH6514 600 MHz, Digital Controlled, Variable Gain Amplifier

Check for Samples: [LMH6514](#)

### FEATURES

- Adjustable Gain with a 42 dB Range
- Precise 6.02 dB Gain Steps
- Parallel 3 Bit Gain Control
- On Chip Register Gain Setting
- Fully Differential Signal Path
- Single Ended to Differential Capable
- 200Ω Input Impedance
- Small Footprint (4 mm x 4 mm) WQFN Package

### APPLICATIONS

- Cellular Base Stations
- IF Sampling Receivers
- Instrumentation
- Modems
- Imaging
- Differential Line Receiver

### KEY SPECIFICATIONS

- 600 MHz bandwidth at 100Ω load
- 39 dBm OIP3 at 75 MHz, 200Ω load
- 26 dB to 38 dB maximum gain
- Selectable output impedance of 200Ω or 400Ω.
- 8.3 dB noise figure
- 5 ns gain step switching time
- 100 mA supply current

### DESCRIPTION

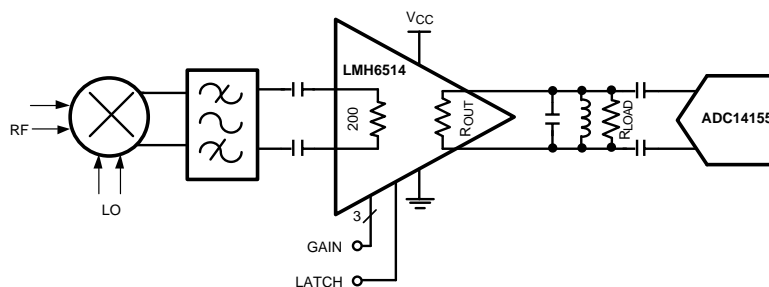
The LMH6514 is a high performance, digitally controlled variable gain amplifier (DVGA). It combines precision gain control with a low noise, ultra-linear, differential amplifier. Typically, the LMH6514 drives a high performance ADC in a broad range of mixed signal and digital communication applications such as mobile radio and cellular base stations where automatic gain control (AGC) is required to increase system dynamic range. When used in conjunction with a high speed ADC, system dynamic range can be extended by up to 42 dB.

The LMH6514 has a differential input and output allowing large signal swings on a single 5V supply. It is designed to accept signals from RF elements and maintain a terminated impedance environment. The input impedance is 200Ω resistive. The output impedance is either 200Ω or 400Ω and is user selectable. A unique internal architecture allows use with both single ended and differential input signals.

Input signals to the LMH6514 are scaled by a highly linear, digitally controlled attenuator with seven accurate 6 dB steps. The attenuator output provides the input signal for a high gain, ultra linear differential transconductor. The transconductor differential output current can be converted into a voltage by using the on-chip 200Ω or 400Ω loads. The transconductance gain is 0.1 Amp/Volt resulting in a maximum voltage gain of +32 dB when driving a 200Ω load, or 38 dB when driving the 400Ω load.

The LMH6514 operates over the industrial temperature range of -40°C to +85°C. The LMH6514 is available in a 16-Pin, thermally enhanced, WQFN package.

### Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	
Human Body Model	2 kV
Machine Model	150V
Positive Supply Voltage (Pin 3)	-0.6V to 5.5V
Output Voltage (Pin 14,15)	-0.6V to 6.8V
Differential Voltage between Any Two Grounds	<200 mV
Analog Input Voltage Range	-0.6V to V <sub>CC</sub>
Digital Input Voltage Range	-0.6V to 3.6V
Output Short Circuit Duration (one pin to ground)	Infinite
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

### Operating Ratings<sup>(1)</sup>

Supply Voltage (Pin 3)	4V to 5.25V
Output Voltage Range (Pin 14, 15)	1.4V to 6.4V
Differential Voltage Between Any Two Grounds	<10 mV
Analog Input Voltage Range, AC Coupled	±1.4V
Temperature Range <sup>(2)</sup>	-40°C to +85°C
Package Thermal Resistance ( $\theta_{JA}$ )	
16-Pin WQFN	47°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) /  $\theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

## 5V Electrical Characteristics<sup>(1)</sup>

The following specifications apply for single supply with  $V_{CC} = 5V$ , Maximum Gain,  $R_L = 100\Omega$  ( $200\Omega$  external ||  $200\Omega$  internal),  $V_{OUT} = 2 V_{PP}$ ,  $f_{in} = 150$  MHz. Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
<b>Dynamic Performance</b>						
SSBW	-3 dB Bandwidth	Average of all Gain Settings		600		MHz
<b>Noise and Distortion</b>						
	Third Order Intermodulation Products	$f = 75$ MHz, $V_{OUT} = 2 V_{PP}$		-70		dBc
		$f = 150$ MHz, $V_{OUT} = 2 V_{PP}$		-66		
		$f = 250$ MHz, $V_{OUT} = 2 V_{PP}$		-60		
		$f = 450$ MHz, $V_{OUT} = 2 V_{PP}$		-52		
OIP3	Output Third Order Intercept Point	$f = 75$ MHz, $V_{OUT} = 2 V_{PP}$ , Tone Spacing = 0.5 MHz		35		dBm
		$f = 150$ MHz, $V_{OUT} = 2 V_{PP}$ , Tone Spacing = 2 MHz		33		
		$f = 250$ MHz, $V_{OUT} = 2 V_{PP}$ , Tone Spacing = 2 MHz		31		
		$f = 75$ MHz, $R_L = 200\Omega$ , $V_{OUT} = 2 V_{PP}$ Tone Spacing = 0.5 MHz		39		
		$f = 150$ MHz, $R_L = 200\Omega$ , $V_{OUT} = 2 V_{PP}$ , Tone Spacing = 2 MHz		37		
		$f = 250$ MHz, $R_L = 200\Omega$ , $V_{OUT} = 2 V_{PP}$ , Tone Spacing = 2 MHz		34		
P1 dB	Output Level for 1 dB Gain Compression	$f = 75$ MHz, $R_L = 200\Omega$		16.7		dBm
		$f = 250$ MHz, $R_L = 200\Omega$		14.7		
		$f = 75$ MHz		14.5		
		$f = 450$ MHz		13.2		
VNI	Input Noise Voltage	Maximum Gain, $f = 40$ MHz		1.8		nV/ $\sqrt{Hz}$
VNO	Output Noise Voltage	Maximum Gain, $f = 40$ MHz		36		nV/ $\sqrt{Hz}$
NF	Noise Figure	Maximum Gain		8.3		dB
<b>Analog I/O</b>						
	Differential Input Resistance		165 <b>158</b>	188	220 <b>230</b>	$\Omega$
	Input Common Mode Resistance		825 <b>785</b>	955	1120 <b>1160</b>	$\Omega$
	Differential Output Resistance	Low Gain Option		186		$\Omega$
		High Gain Option	330 <b>325</b>	370	420 <b>425</b>	
	Internal Load Resistors	Between Pins 13, 14 and Pins 15, 16	165 <b>158</b>	187	215 <b>225</b>	$\Omega$
	Input Signal Level (AC Coupled)	Max Gain, $V_O = 2 V_{PP}$ , $R_L = 1$ k $\Omega$		63		mV $_{PP}$
	Maximum Differential Input Signal	AC Coupled		5.6		V $_{PP}$
	Input Common Mode Voltage	Self Biased	1.3 <b>1.1</b>	1.4	1.5 <b>1.7</b>	V
	Input Common Mode Voltage Range	Driven Externally		0.9 to 2.0		V
	Minimum Input Voltage	DC		0		V
	Maximum Input Voltage	DC		3.3		V

- Electrical Table values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested
- Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

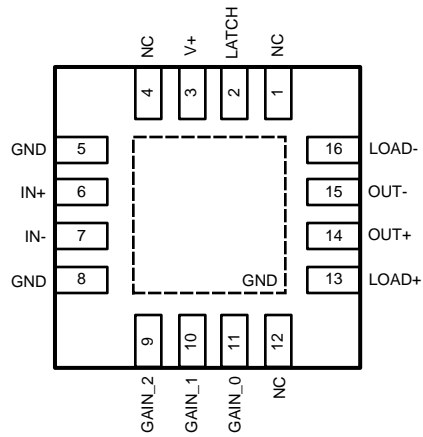
### 5V Electrical Characteristics<sup>(1)</sup> (continued)

The following specifications apply for single supply with  $V_{CC} = 5V$ , Maximum Gain,  $R_L = 100\Omega$  ( $200\Omega$  external ||  $200\Omega$  internal),  $V_{OUT} = 2 V_{PP}$ ,  $f_{in} = 150$  MHz. Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
	Maximum Differential Output Voltage Swing	$V_{CC} = 5V$ , Output Common Mode = 5V		5.5		$V_{PP}$
$V_{OS}$	Output Offset Voltage	All Gain Settings		-21		mV
CMRR	Common Mode Rejection Ratio	Maximum Gain		81		dB
PSRR	Power Supply Rejection Ratio	Maximum Gain	63 61	81		dB
<b>Gain Parameters</b>						
	Maximum Gain	DC, Internal $R_L = 186\Omega$ , External $R_L = 1280\Omega$	29.3 28.7	30	30.3 30.9	dB
	Minimum Gain	DC, Internal $R_L = 186\Omega$ , External $R_L = 1280\Omega$	-12.75 -13.15	-12	-11.85 -11.45	dB
	Gain Step Size	DC		6.02		dB
	Gain Step Error	DC		0.02		dB
		$f = 150$ MHz		0.07		
	Cumulative Gain Step Error	DC, Gain Step 7 to Gain Step 0	-0.35 -0.50	0.02	0.30 0.45	dB
	Gain Step Switching Time			5		ns
<b>Digital Inputs/Timing</b>						
	Logic Compatibility	CMOS Logic		3.3		V
$V_{IL}$	Logic Input Low Voltage				0.8	V
$V_{IH}$	Logic Input High Voltage		2.0			V
$I_{IH}$	Logic Input High Input Current <sup>(4)</sup>	Digital Input Voltage = 3.3V		33	40	$\mu A$
TSU	Setup Time			3		ns
THOLD	Hold Time			3		ns
TPW	Minimum Latch Pulse Width			10		ns
<b>Power Requirements</b>						
ICC	Total Supply Current	$V_{OUT} = 0V$ Differential, $V_{OUT}$ Common Mode = 5V		107	124 134	mA
	Amplifier Supply Current	Pin 3 Only		56	66 74	mA
	Output Stage Bias Currents	Pins 13, 14 and Pins 15, 16; $V_{OUT}$ Common Mode = 5 V		51	58 60	mA

(4) Negative input current implies current flowing out of the device.

**Connection Diagram**



**Figure 1. 16-Pin WQFN (Top View)**

**Gain Control Pins**

Pin Number	Pin Name	Gain Step Size
11	GAIN_0	6.02 dB
10	GAIN_1	12.04 dB
9	GAIN_2	24.08 dB

**PIN DESCRIPTIONS**

Pin Number	Symbol	Description
<b>Analog I/O</b>		
6	IN+	Non-inverting analog input. Internally biased to 1.4V. Input voltage should not exceed $V_{CC}$ or go below GND by more than 0.5V.
7	IN-	Inverting analog input. Internally biased to 1.4V. Input voltage should not exceed $V_{CC}$ or go below GND by more than 0.5V. If using amplifier single ended this input should be capacitively coupled to ground.
15	OUT-	Open collector inverting output. This pin is an output that also requires a power source. This pin should be connected to 5V through either an RF choke or an appropriately sized inductor that can form part of a filter. See <a href="#">Application Information</a> for details.
14	OUT+	Open collector non-inverting output. This pin is an output that also requires a power source. This pin should be connected to 5V through either an RF choke or an appropriately sized inductor that can form part of a filter. See <a href="#">Application Information</a> for details.
16	LOAD-	Internal 200 $\Omega$ resistor connection to pin 15. This pin can be left floating for higher gain or shorted to pin 13 for lower gain and lower effective output impedance. See <a href="#">Application Information</a> for details.
13	LOAD+	Internal 200 $\Omega$ resistor connection to pin 14. This pin can be left floating for higher gain or shorted to pin 16 for lower gain and lower effective output impedance. See <a href="#">Application Information</a> for details.
<b>Power</b>		
3	$V_{CC}$	5V power supply pin. Use ceramic, low ESR bypass capacitors. This pin powers everything except the output stage.
5,8	GND	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is also a ground connection.
<b>Digital Inputs</b>		
11,10,9	GAIN_0 to GAIN_2	Gain setting pins. See above table for gain step sizes for each pin. These pins are 3.3V CMOS logic compatible. 5V inputs may cause damage.
2	LATCH	This pin controls the function of the gain setting pins mentioned above. With LATCH in the logic HIGH state the gain is fixed and will not change. With the LATCH in the logic LOW state the gain is set by the state of the gain control pins. Any changes in gain made with the LATCH pin in the LOW state will take effect immediately. This pin is 3.3V CMOS logic compatible. 5V inputs may cause damage.
1,4,12	NC	These pins are not connected. They can be grounded or left floating.

Typical Performance Characteristics  
 $V_{CC} = 5V$

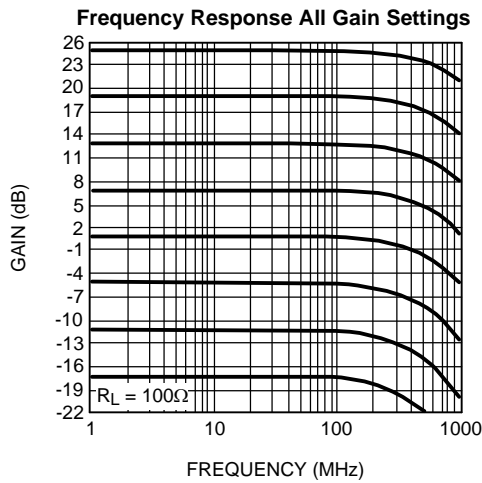


Figure 2.

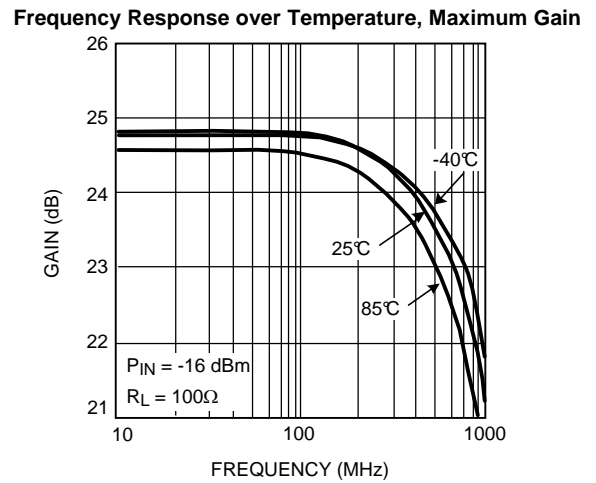


Figure 3.

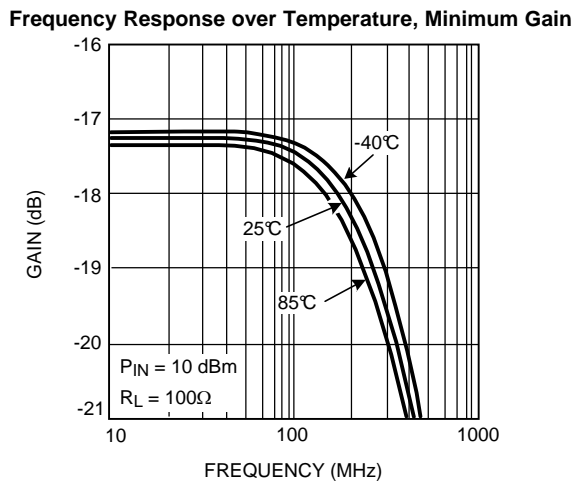


Figure 4.

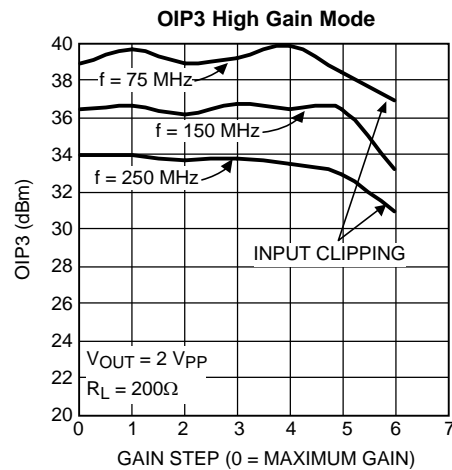


Figure 5.

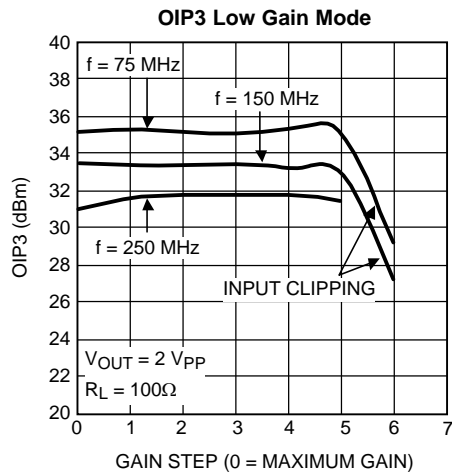


Figure 6.

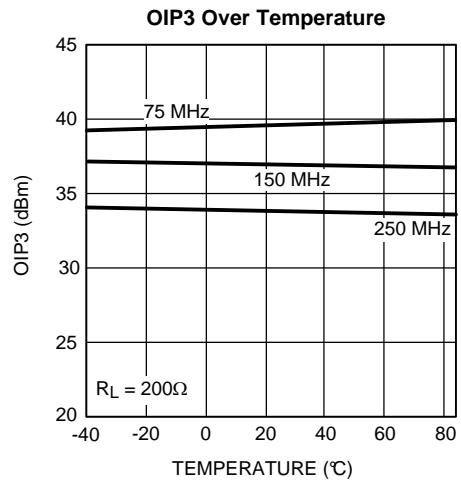


Figure 7.

**Typical Performance Characteristics**  
**V<sub>CC</sub> = 5V (continued)**

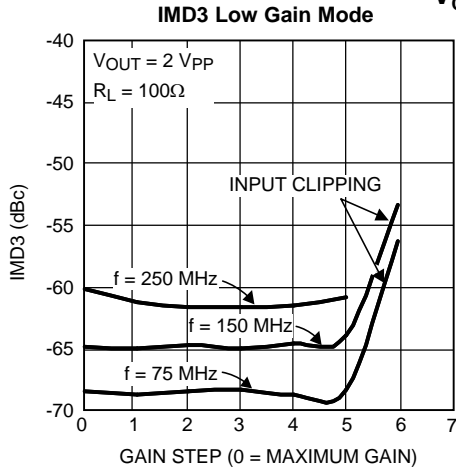


Figure 8.

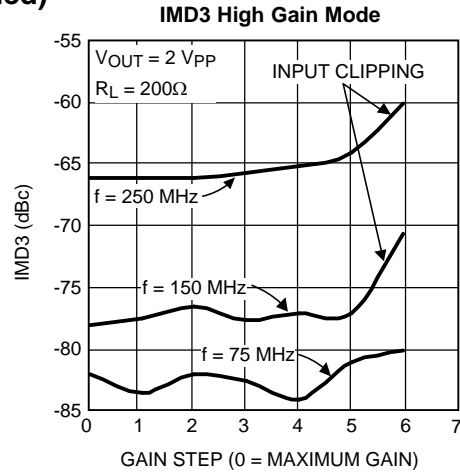


Figure 9.

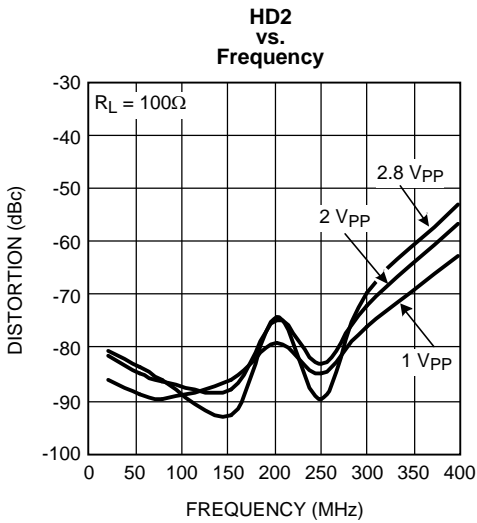


Figure 10.

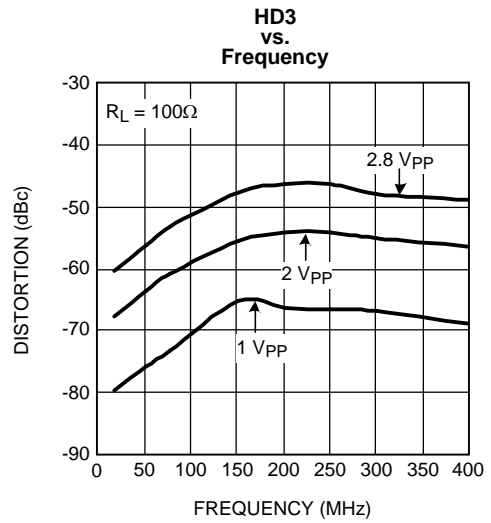


Figure 11.

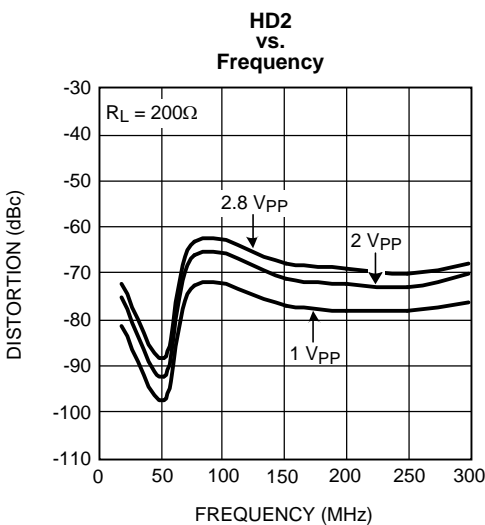


Figure 12.

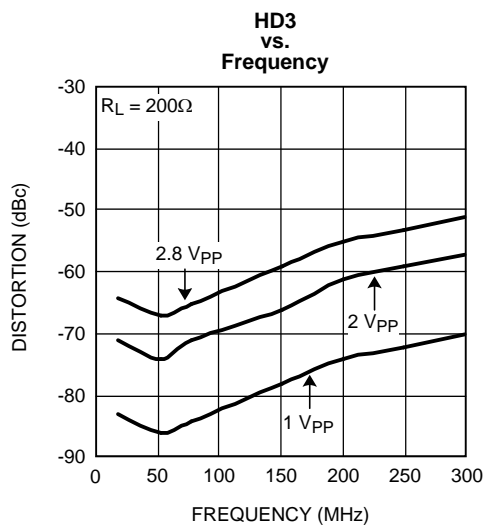


Figure 13.



Typical Performance Characteristics

V<sub>CC</sub> = 5V (continued)

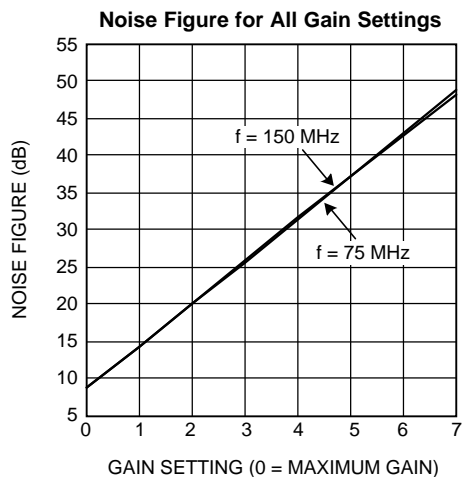


Figure 14.

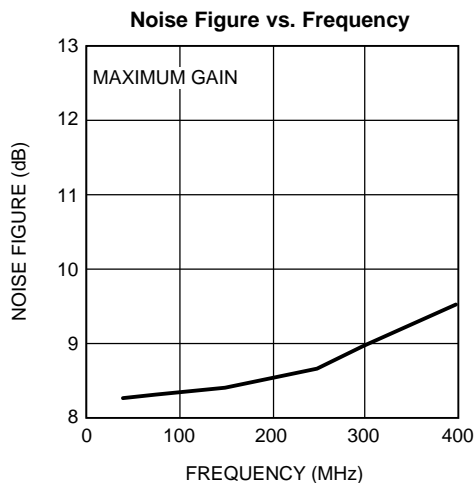


Figure 15.

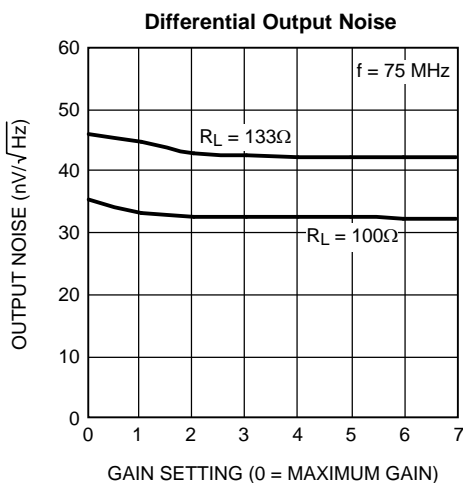


Figure 16.

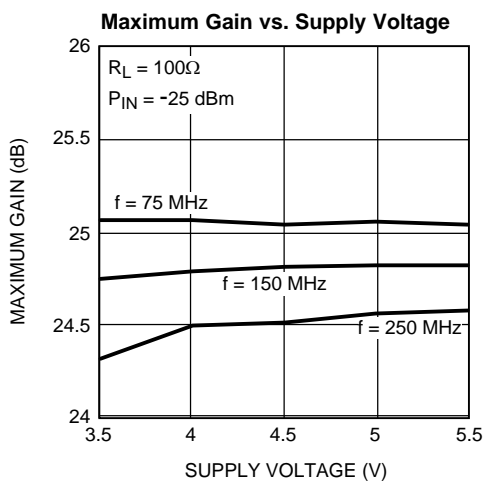


Figure 17.

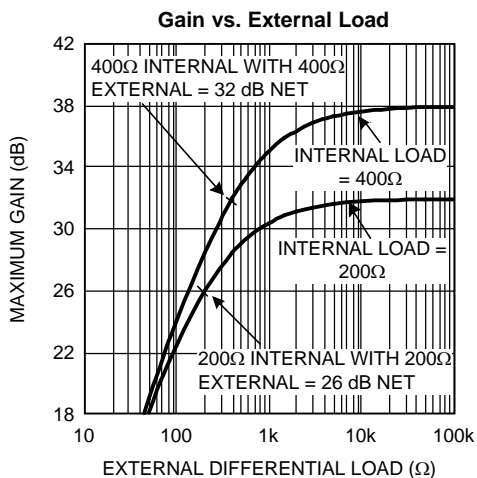


Figure 18.

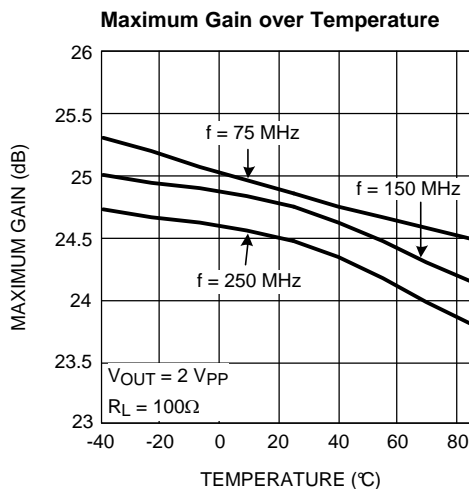


Figure 19.

Typical Performance Characteristics

$V_{CC} = 5V$  (continued)

Worst Case Gain Step Error vs Frequency

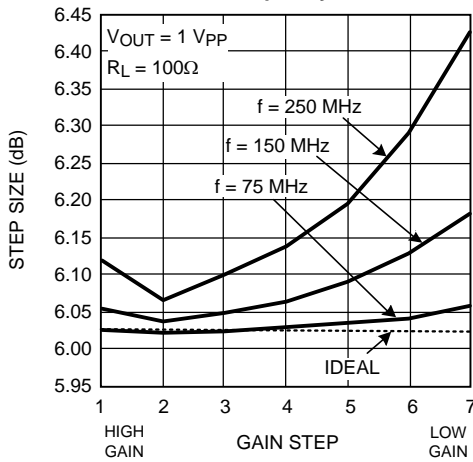


Figure 20.

Gain Steps over Temperature

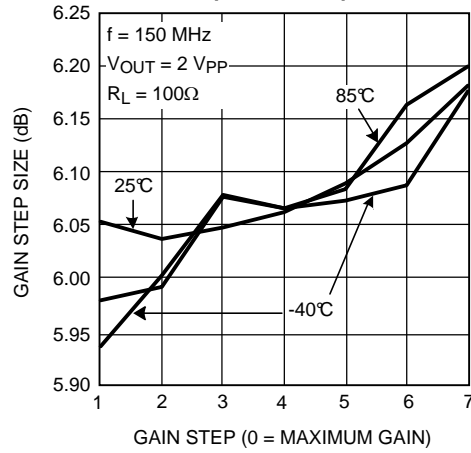


Figure 21.

Worst Case Gain Step Error over Temperature

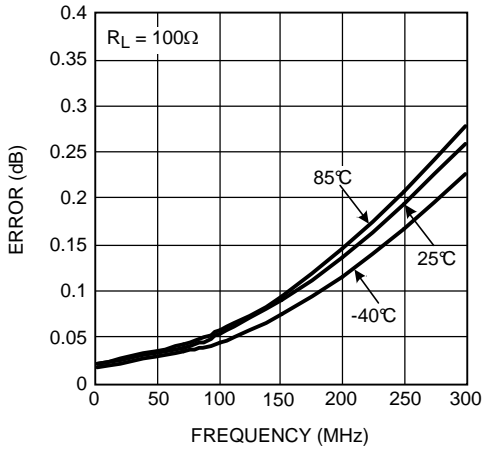


Figure 22.

Input Impedance (S11) at Maximum Gain

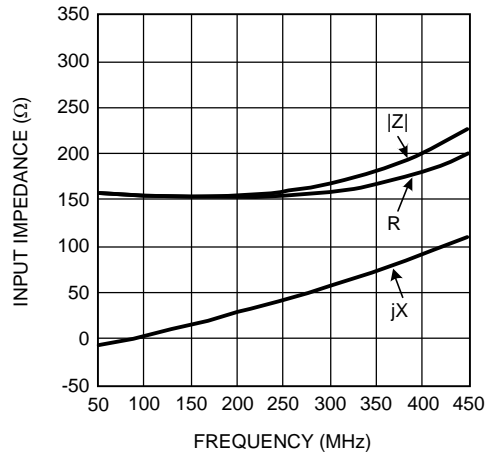


Figure 23.

Input Impedance (S11) at Minimum Gain

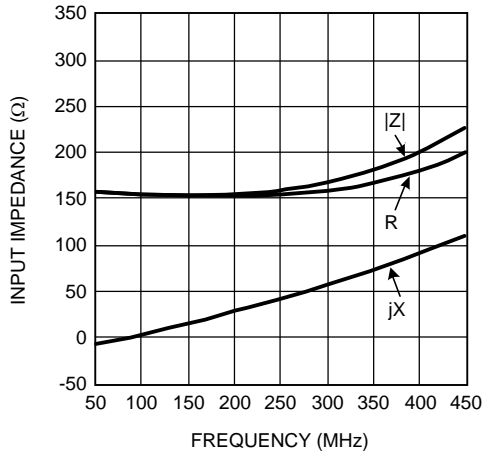


Figure 24.

Output Impedance (S22) at Maximum Gain Low Gain Mode

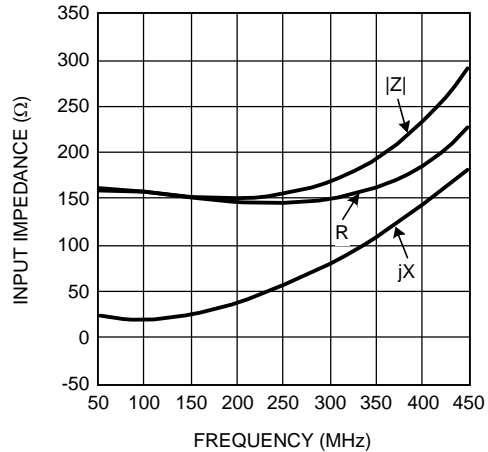


Figure 25.

Typical Performance Characteristics

$V_{CC} = 5V$  (continued)

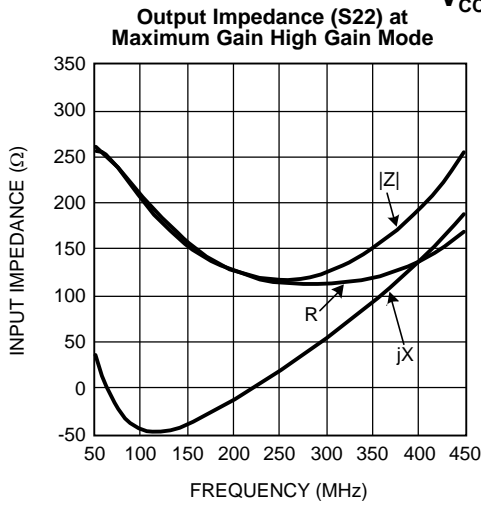


Figure 26.

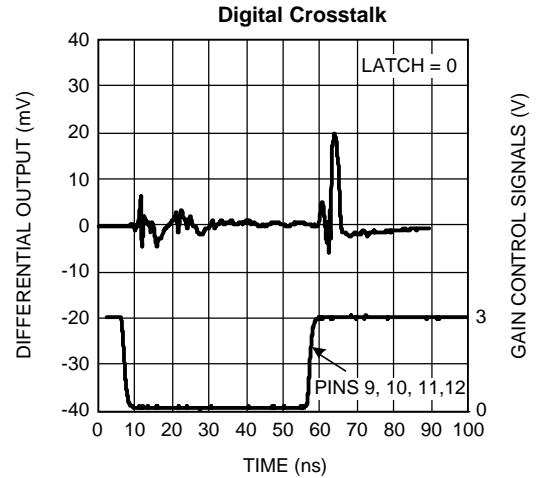


Figure 27.

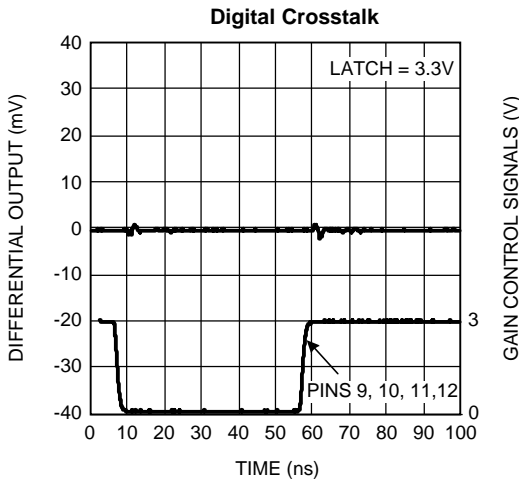


Figure 28.

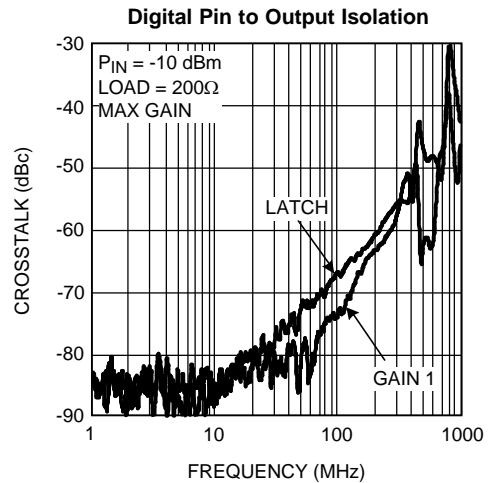


Figure 29.

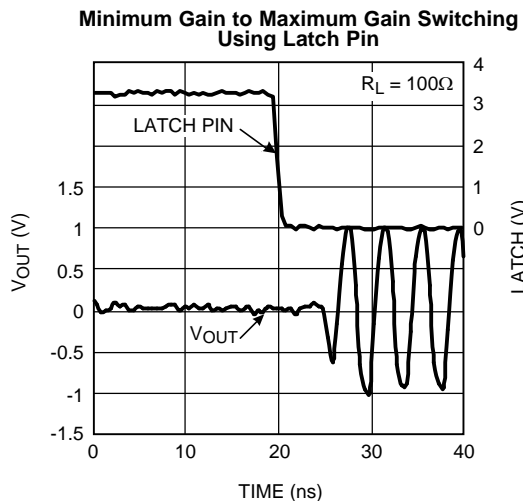


Figure 30.

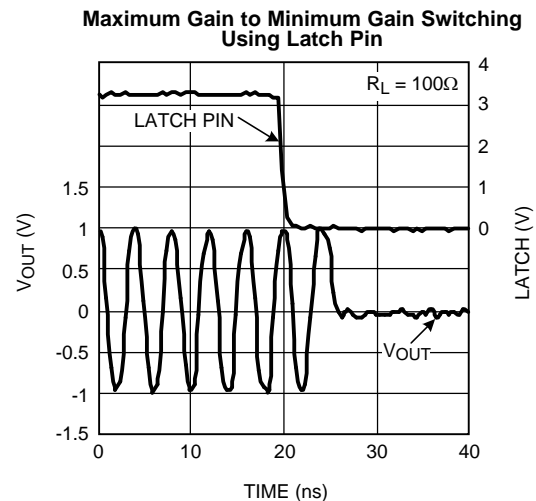


Figure 31.

**Typical Performance Characteristics**  
**V<sub>CC</sub> = 5V (continued)**

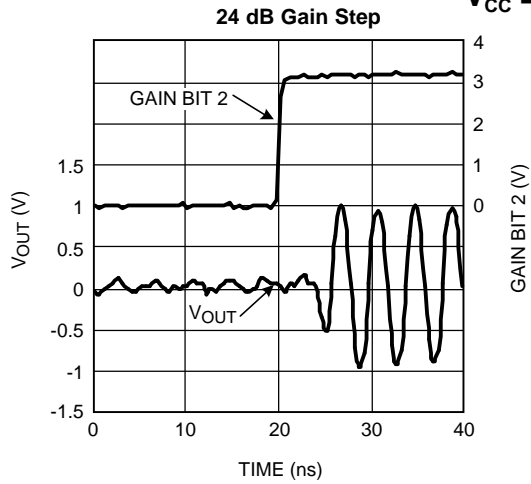


Figure 32.

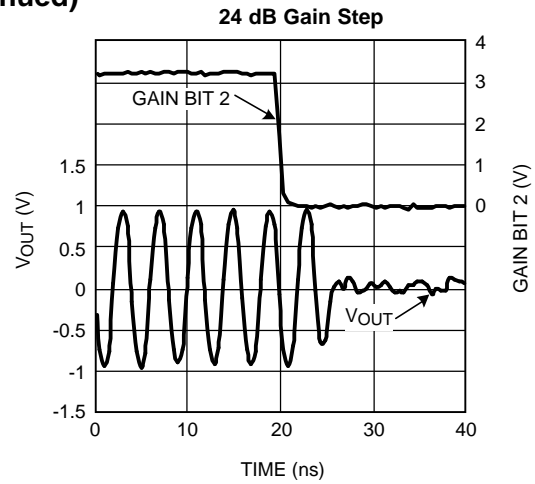


Figure 33.

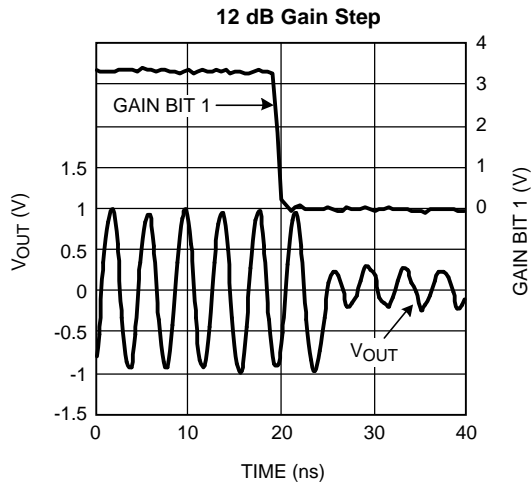


Figure 34.

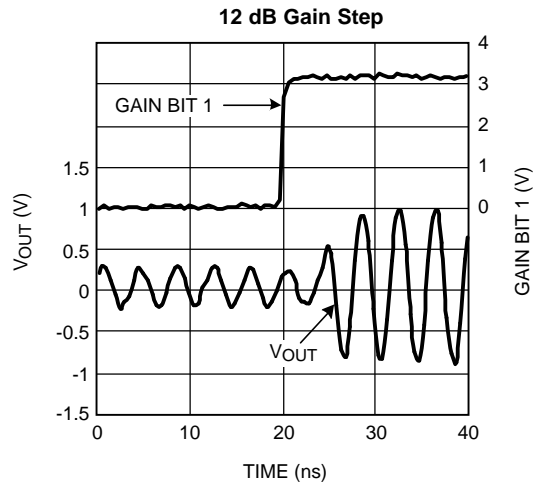


Figure 35.

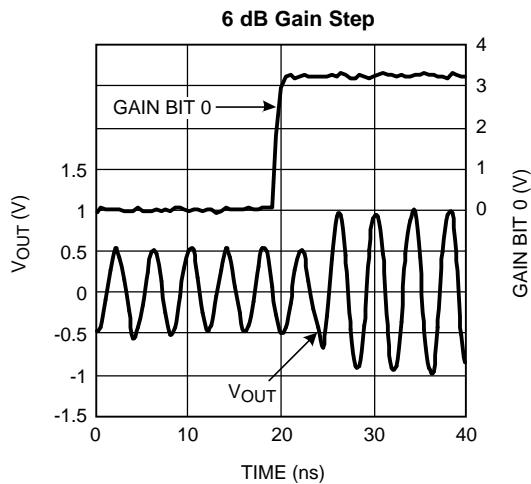


Figure 36.

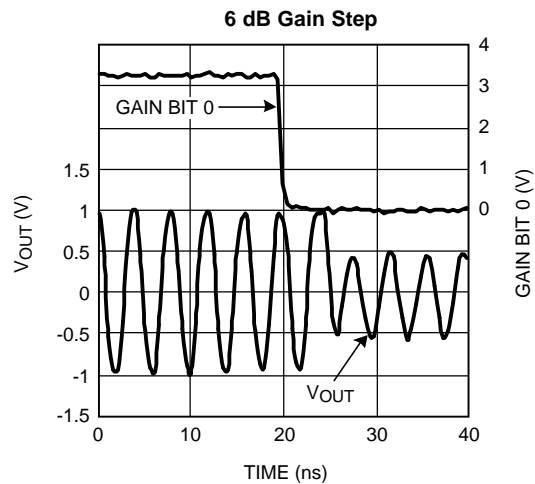


Figure 37.

Typical Performance Characteristics

V<sub>CC</sub> = 5V (continued)

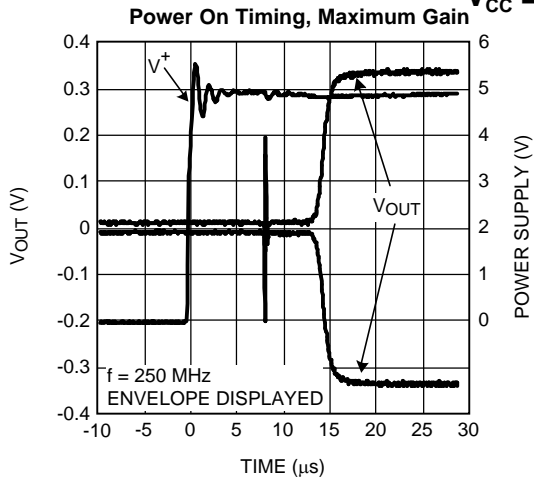


Figure 38.

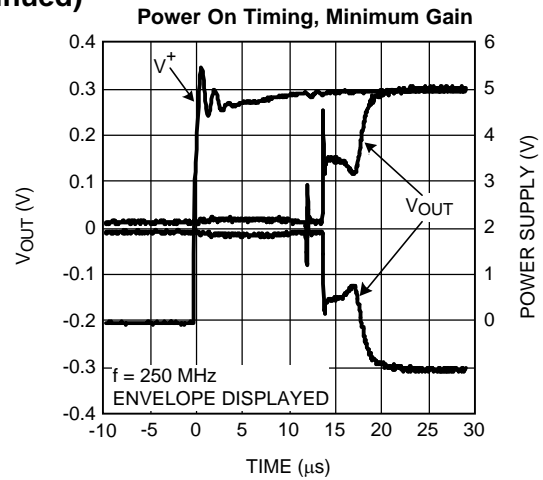


Figure 39.

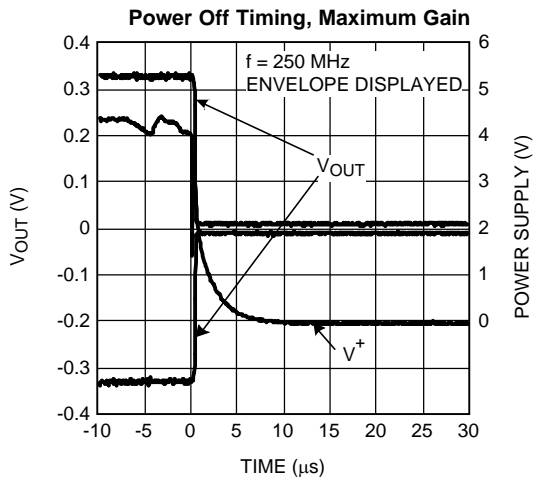


Figure 40.

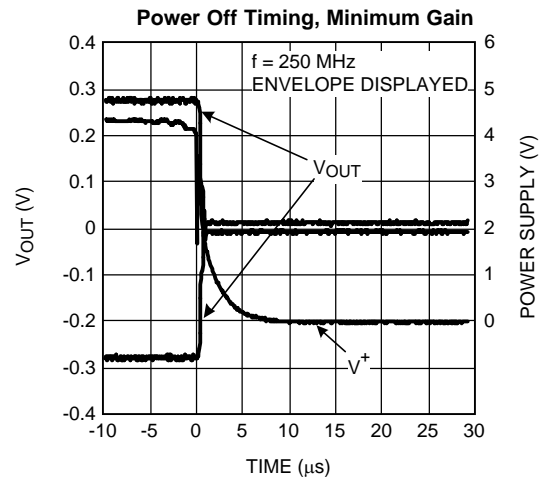
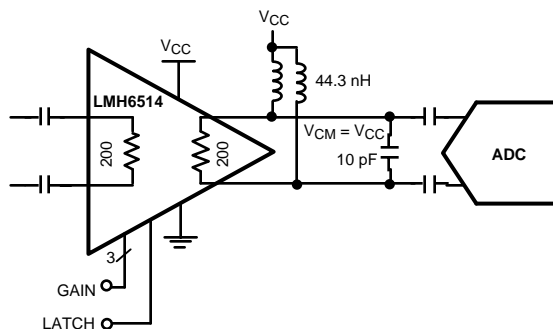


Figure 41.

## APPLICATION INFORMATION

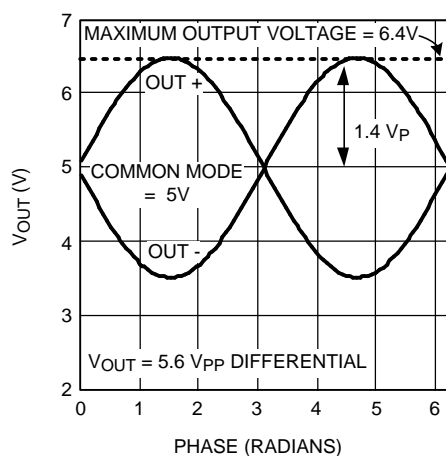
The LMH6514 is a fully differential amplifier optimized for signal path applications up to 400 MHz. The LMH6514 has a 200Ω input. The absolute gain is load dependent, however the gain steps are always 6 dB. The LMH6514 output stage is a class A amplifier. This class A operation results in excellent distortion and linearity characteristics. This makes the LMH6514 ideal for voltage amplification and an ideal ADC driver where high linearity is necessary.



**Figure 42. LMH6514 Typical Application**

The LMH6514 output common mode should be set carefully. Using inductors to set the output common mode is one preferred method and will give maximum output swing. AC coupling of the output is recommended. The inductors mentioned above will shift the idling output common mode to the positive supply. Also, with the inductors, the output voltage can exceed the supply voltage. Other options for setting the output common mode require supply voltages above 5V. If using a supply higher than 5V care should be taken to make sure the output common mode does not exceed the 5.25V supply rating.

It is also important to note the maximum voltage limits for the OUT+ and OUT– pins, which is 6.4V. When using inductors these pins will experience voltage swings beyond the supply voltage. With a 5V output common mode operating point this makes the effective maximum swing 5.6 V<sub>PP</sub> differential. System calibration and automatic gain control algorithms should be tailored to avoid exceeding this limit. Figure 43 shows how output voltage and output common mode add together and approach the maximum output voltage.



**Figure 43. Output Voltage with Respect to the Output Common Mode**

In order to help with system design Texas Instruments offers the ADC14V155KDRB High IF Receiver reference design board. This board combines the LMH6514 DVGA with the ADC14V155 ADC and provides a ready made solution for many IF receiver applications. Using an IF frequency of 169 MHz it achieves a small signal SNR of 72 dBFS and an SFDR of greater than 90 dBFS. Large signal measurements show an SNR of 68 dBFS and an SFDR of 77 dBFS. The High IF Receiver board also features the LMK03000 low-jitter precision clock conditioner.

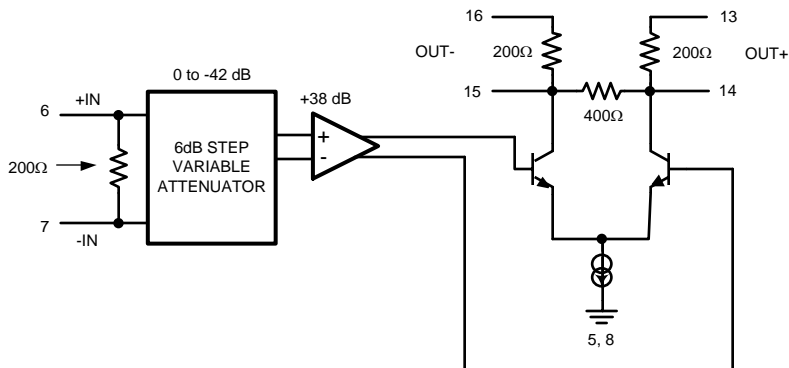


Figure 44. LMH6514 Block Diagram

### INPUT CHARACTERISTICS

The LMH6514 input impedance is set by internal resistors to a nominal 200Ω. Process variations will result in a range of values as shown in the [Electrical Characteristics](#) table. At higher frequencies parasitics will start to impact the impedance. This characteristic will also depend on board layout and should be verified on the customer's system board.

At maximum gain the digital attenuator is set to 0 dB and the input signal will be much smaller than the output. At minimum gain the output is 4 dB or more smaller than the input. In this configuration the input signal size may limit the amplifier output amplitude, depending on the output configuration and the desired output signal voltage. The input signal cannot swing more than 0.5V below the negative supply voltage (normally 0V) nor should it exceed the positive supply voltage. The input signal will clip and cause severe distortion if it is too large. Because the input stage self biases to approximately 1.4V the lower supply voltage will impose the limit for input voltage swing. To drive larger input signals the input common mode can be forced higher than 1.4V to allow for more swing. An input common mode of 2.0V will allow an 8 V<sub>PP</sub> maximum input signal. The trade off for input signal swing is that as the input common mode is shifted away from the 1.4V internal bias point the distortion performance will suffer slightly.

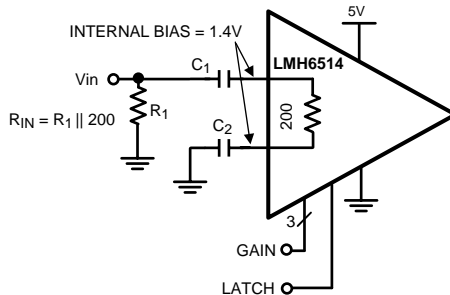
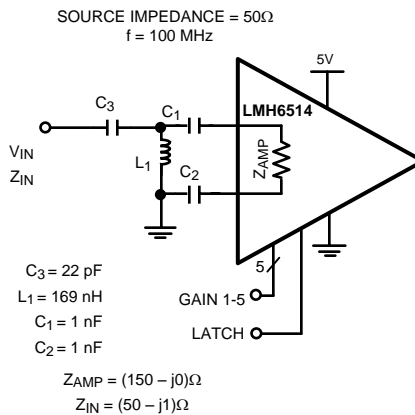


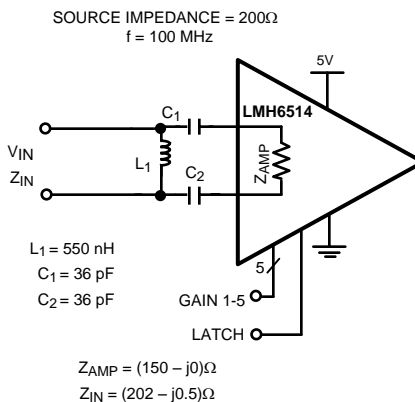
Figure 45. Single Ended Input  
(Note capacitor on grounded input)

At the frequencies where the LMH6514 is the most useful the input impedance is not 200 Ω and it may not be purely resistive. For many AC coupled applications the impedance can be easily changed using LC circuits to transform the actual impedance to the desired impedance.



**Figure 46. Single Ended Input with LC Matching**

As shown in Figure 46 a single ended  $50\Omega$  source is matched to the LMH6514 input at 100 MHz. The loss in this circuit is related to the parasitic resistance in the inductor and capacitor and the bandwidth is related to the loaded Q of the circuit. Since the Q, at 1.4 is quite low, the bandwidth is very wide. (59 MHz 0.3 dB bandwidth). The input match of this circuit is quite good. It converts the  $Z_{AMP}$  of the amplifier, which is  $(150 + j0)\Omega$  to  $(50 + j1)\Omega$ . The benefit of LC matching circuits over a transformer is the ability to match ratios that are not commonly found on transformers and also the ability to neutralize reactance to present a purely resistive load to the voltage source.



**Figure 47. Differential  $200\Omega$  LC Conversion Circuit**

In Figure 47 the input source resistance is  $200\Omega$  differential. Here the desired input impedance is higher than the amplifier input impedance, and is differential as well. The amplifier impedance of  $(150 - j0)\Omega$  is increased to  $(202 - j0.5)\Omega$ . For an easy way to calculate the L and C circuit values there are several options for online tools or down-loadable programs. The following tool might be helpful.

<http://www.circuitsage.com/matching/matcher2.html>

Excel can also be used for simple circuits; however, the “Analysis ToolPak” add-in must be installed to calculate complex numbers.



## OUTPUT CHARACTERISTICS

The LMH6514 has the option of two different output configurations. The LMH6514 is an open collector topology. As shown in [Figure 52](#) each output has an on chip  $200\Omega$  pull up resistor. In addition there is an internal  $400\Omega$  resistor between the two outputs. This results in a  $200\Omega$  or a  $400\Omega$  differential load in parallel with the external load. The  $400\Omega$  option is the high gain option and the  $200\Omega$  provides for less gain. The  $200\Omega$  configuration is recommended unless more gain is required.

The output common mode of the LMH6514 must be set by external components. Most applications will benefit from the use of inductors on the output stage. In particular, the  $400\Omega$  option as shown in [Figure 53](#) will require inductors in order to be able to develop an output voltage. The  $200\Omega$  option as shown in [Figure 54](#) or [Figure 55](#) will also require inductors since the voltage drop due to the on chip  $200\Omega$  resistors will saturate the output transistors. It is also possible to use resistors and high voltage power supplies to set the output common mode. This operation is not recommended, unless it is necessary to DC couple the output. If DC coupling is required the input common mode and output common mode voltages must be taken into account.

Maximum bandwidth with the LMH6514 is achieved by using the low gain, low impedance output option and using a low load resistance. With an effective load of  $67\Omega$  a bandwidth of nearly a 1 GHz can be realized. As the effective resistance on the output stage goes up the capacitance of the board traces and amplifier output stage limit bandwidth in a roughly linear fashion. At an output impedance of  $100\Omega$  the bandwidth is down to 600 MHz, and at  $200\Omega$  the bandwidth is 260 MHz. For this reason driving very high impedance loads is not recommended.

Although bandwidth goes down with higher values of load resistance, the distortion performance improves and gain increases. The LMH6514 has a common emitter Class A output stage and minimizing the amount of current swing in the output devices improves distortion substantially.

The LMH6514 output stage is powered through the collectors of the output transistors. Power for the output stage is fed through inductors and the reactance of the inductors allows the output voltage to develop. In [Figure 42](#) the inductors are shown with a value of  $44.4\text{ nH}$ . The value of the inductors used will be different for different applications. In [Figure 42](#) the inductors have been chosen to resonate with the ADC and the load capacitor to provide a weak band pass filter effect. For broad band applications higher value inductors will allow for better low frequency operation. However, large valued inductors will reduce high frequency performance, particularly inductors of small physical sizes like 0603 or smaller. Larger inductors will tend to perform better than smaller ones of the same value even for narrow band applications. This is because the larger inductors will have a lower DC resistance and less inter-winding capacitance and hence a higher Q and a higher self resonance frequency. The self resonance frequency should be higher than any desired signal content by at least a factor of 2. Another consideration is that the power inductors and the filter inductors need to be placed on the circuit board such that their magnetic fields do not cause coupling. Mutual coupling of inductors can compromise filter characteristics and lead to unwanted distortion products.

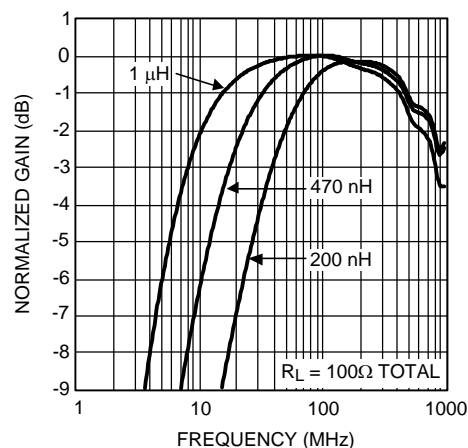
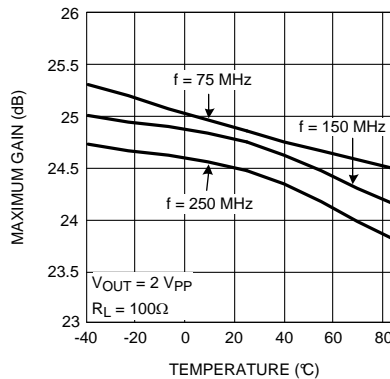


Figure 48. Bandwidth Changes Due to Different Inductor Values



**Figure 49. Gain vs. External Load**

## DIGITAL CONTROL

The LMH6514 has eight gain settings covering a range of 42 dB. To avoid undesirable signal transients the LMH6514 should be powered on at the minimum gain state (all logic input pins at 0V). The LMH6514 has a 3-bit gain control bus as well as a Latch pin. When the Latch pin is low, data from the gain control pins is immediately sent to the gain circuit (i.e. gain is changed immediately). When the Latch pin transitions high the current gain state is held and subsequent changes to the gain set pins are ignored. To minimize gain change glitches multiple gain control pins should not change while the latch pin is low. In order to achieve the very fast gain step switching time of 5 ns the internal gain change circuit is very fast. Gain glitches could result from timing skew between the gain set bits. This is especially the case when a small gain change requires a change in state of three or more gain control pins. If continuous gain control is desired the Latch pin can be tied to ground. This state is called transparent mode and the gain pins are always active. In this state the timing of the gain pin logic transitions should be planned carefully to avoid undesirable transients.

The LMH6514 was designed to interface with 3.3V CMOS logic circuits. If operation with 5V logic is required a simple voltage divider at each logic pin will allow for this. To properly terminate 100Ω transmission lines a divider with a 66.5Ω resistor to ground and a 33.2Ω series resistor will properly terminate the line as well as give the 3.3V logic levels. Care should be taken not to exceed the 3.6V absolute maximum voltage rating of the logic pins.

## EXPOSED PAD WQFN PACKAGE

The LMH6514 is packaged in a thermally enhanced package. The exposed pad is connected to the GND pins. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. In any case, the thermal dissipation of the device is largely dependent on the attachment of this pad. The exposed pad should be attached to as much copper on the circuit board as possible, preferably external copper. However, it is also very important to maintain good high speed layout practices when designing a system board. Please refer to the LMH6514 evaluation board for suggested layout techniques.

Package information is available on the TI web site.

<http://www.ti.com/packaging>

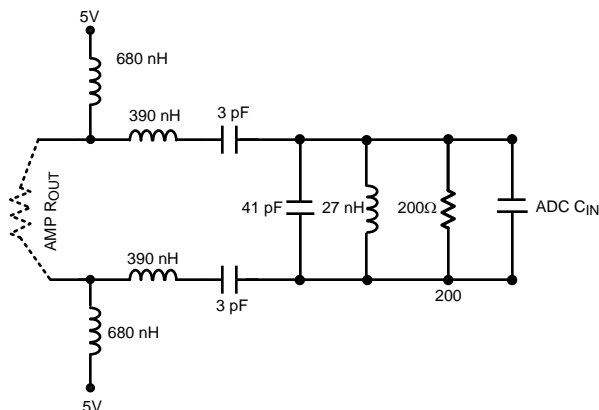
## INTERFACING TO ADC

The LMH6514 was designed to be used with high speed ADCs such as the ADC14155. As shown in the Typical Application on page 1, AC coupling provides the best flexibility especially for IF sub-sampling applications. Any resistive networks on the output will also cause a gain loss because the output signal is developed across the output resistors. The chart *Maximum Gain vs. External Load* shows the change in gain when an external load is added.

The inputs of the LMH6514 will self bias to the optimum voltage for normal operation. The internal bias voltage for the inputs is approximately 1.4V. In most applications the LMH6514 input will need to be AC coupled.

The output common mode voltage is not self biasing, it needs to be pulled up to the positive supply rail with external inductors as shown in [Figure 42](#). This gives the LMH6514 the capability for large signal swings with very low distortion on a single 5V supply. The internal load resistors provide the LMH6514 with very consistent gain.

A unique internal architecture allows the LMH6514 to be driven by either a differential or single ended source. If driving the LMH6514 single ended the unused input should be terminated to ground with a 0.01  $\mu$ F capacitor. Directly shorting the unused input to ground will disrupt the internal bias circuitry and will result in poor performance.



Center Frequency is 140 MHz with a 20 MHz Bandwidth  
Designed for 200 $\Omega$  Impedance

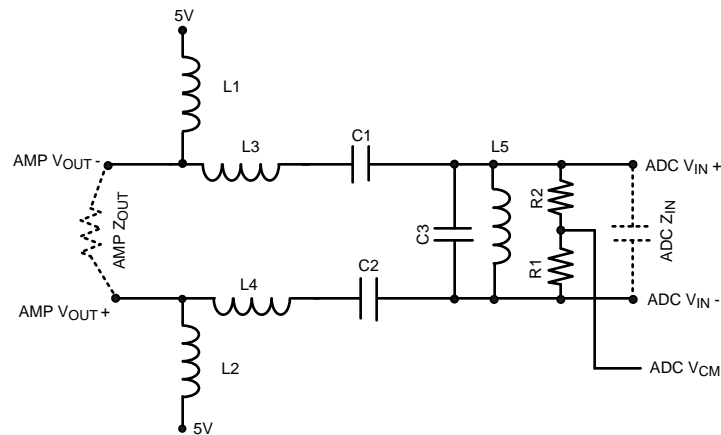
**Figure 50. Bandpass Filter**

**ADC Noise Filter**

Below is a filter schematic and a table of values for some common IF frequencies. The filter shown below offers a good compromise between bandwidth, noise rejection and cost. This filter topology is the same as is used on the ADC14V155KDRB High IF Receiver reference design board. This filter topology works best with the 12 and 14 bit sub-sampling analog to digital converters shown in the [Table 2](#) table.

**Table 1. Filter Component Values**

Filter Component Values					
	Fc	75 MHz	140 MHz	170 MHz	250 MHz
	BW	40 MHz	20 MHz	25 MHz	Narrow Band
Components	L1, L2	10 $\mu$ H	10 $\mu$ H	10 $\mu$ H	10 $\mu$ H
	L3, L4	390 nH	390 nH	560 nH	—
	C1, C2	10 pF	3 pF	1.4 pF	47 pF
	C3	22 pF	41 pF	32 pF	11 pF
	L5	220 nH	27 nH	30 nH	22 nH
	R1, R2	100	200	100	499



**Figure 51. Sample Filter**

## POWER SUPPLIES

As shown in [Figure 52](#), the LMH6514 has a number of options for power supply connections on the output pins. Pin 3 ( $V_{CC}$ ) is always connected. The output stage can be connected as shown in [Figure 53](#), [Figure 54](#), and [Figure 55](#). The supply voltage range for  $V_{CC}$  is 4V to 5.25V. A 5V supply provides the best performance while lower supplies will result in less power consumption. Power supply regulation of 2.5% or better is advised.

Of special note is that the digital circuits are powered from an internal supply voltage of 3.3V. The logic pins should not be driven above the absolute maximum value of 3.6V. See the [DIGITAL CONTROL](#) section for details.

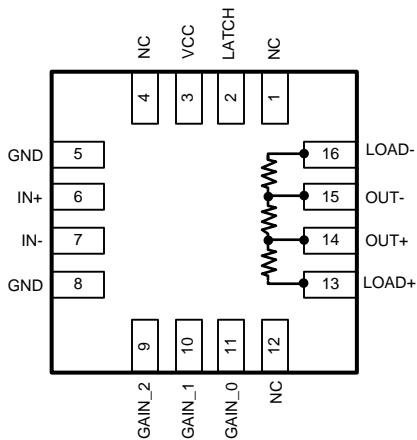


Figure 52. Internal Load Resistors

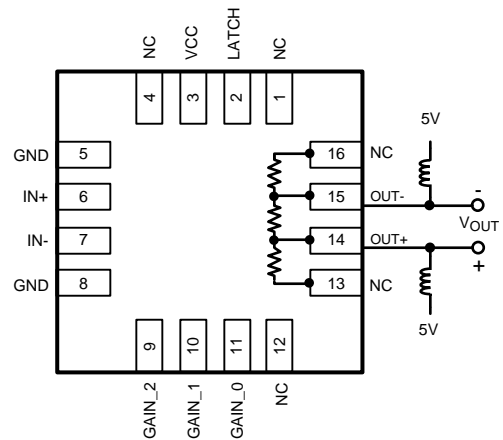


Figure 53. Using High Gain Mode (400Ω Load)

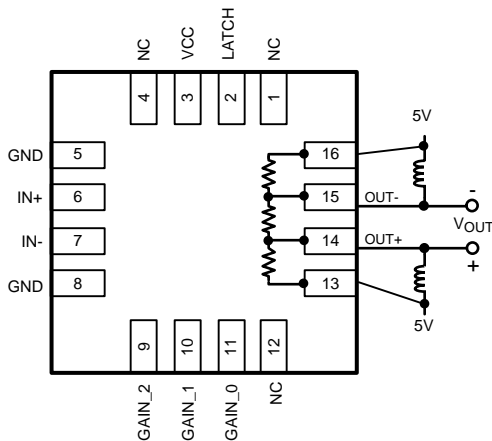


Figure 54. Using Low Gain Mode (200Ω Load)

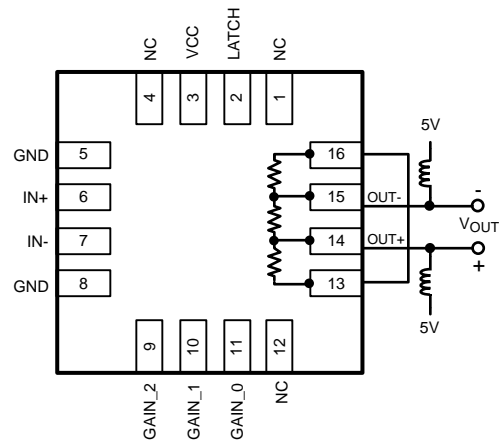


Figure 55. Alternate Connection for Low Gain Mode (200Ω Load)

**Table 2. Compatible High Speed Analog to Digital Converters**

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC12L063	62	12	SINGLE
ADC12DL065	65	12	DUAL
ADC12L066	66	12	SINGLE
ADC12DL066	66	12	DUAL
CLC5957	70	12	SINGLE
ADC12L080	80	12	SINGLE
ADC12DL080	80	12	DUAL
ADC12C080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C080	80	14	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14I55	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08060	60	8	SINGLE
ADC10DL065	65	10	DUAL
ADC10065	65	10	SINGLE
ADC10080	80	10	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

---

**REVISION HISTORY**

<b>Changes from Original (March 2013) to Revision A</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <a href="#">21</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6514SQ/NOPB	ACTIVE	WQFN	RGH	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6514SQ	<b>Samples</b>
LMH6514SQE/NOPB	ACTIVE	WQFN	RGH	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6514SQ	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

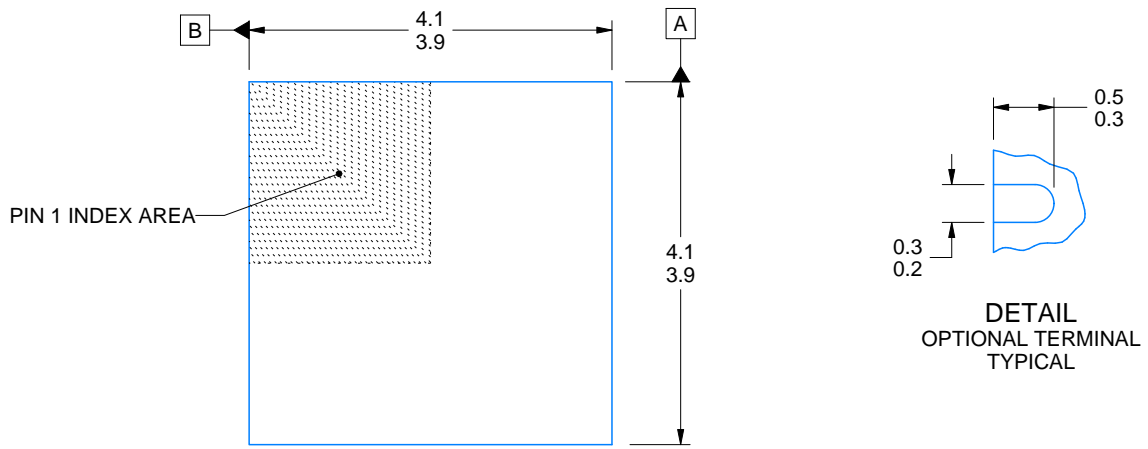
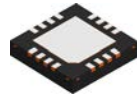

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6514SQ/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6514SQE/NOPB	WQFN	RGH	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

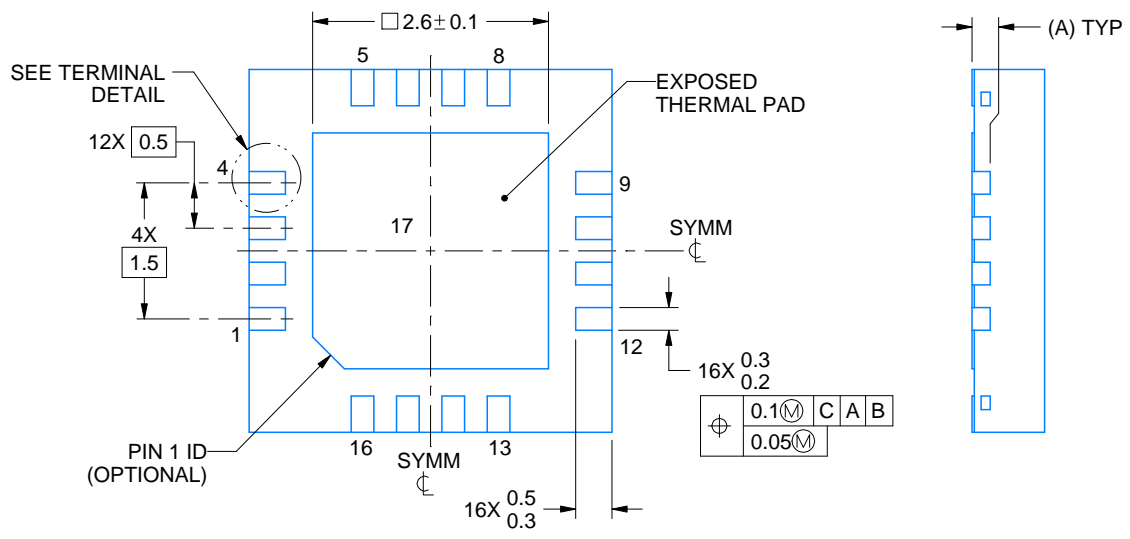
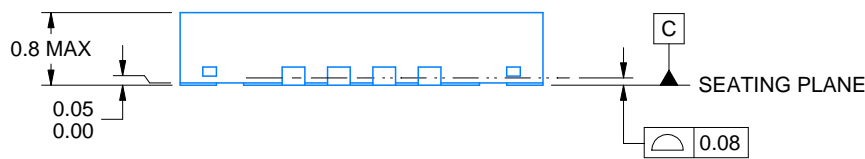
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6514SQ/NOPB	WQFN	RGH	16	1000	208.0	191.0	35.0
LMH6514SQE/NOPB	WQFN	RGH	16	250	208.0	191.0	35.0



DIM A	
OPT 1	OPT 1
(0.1)	(0.2)



4214978/B 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

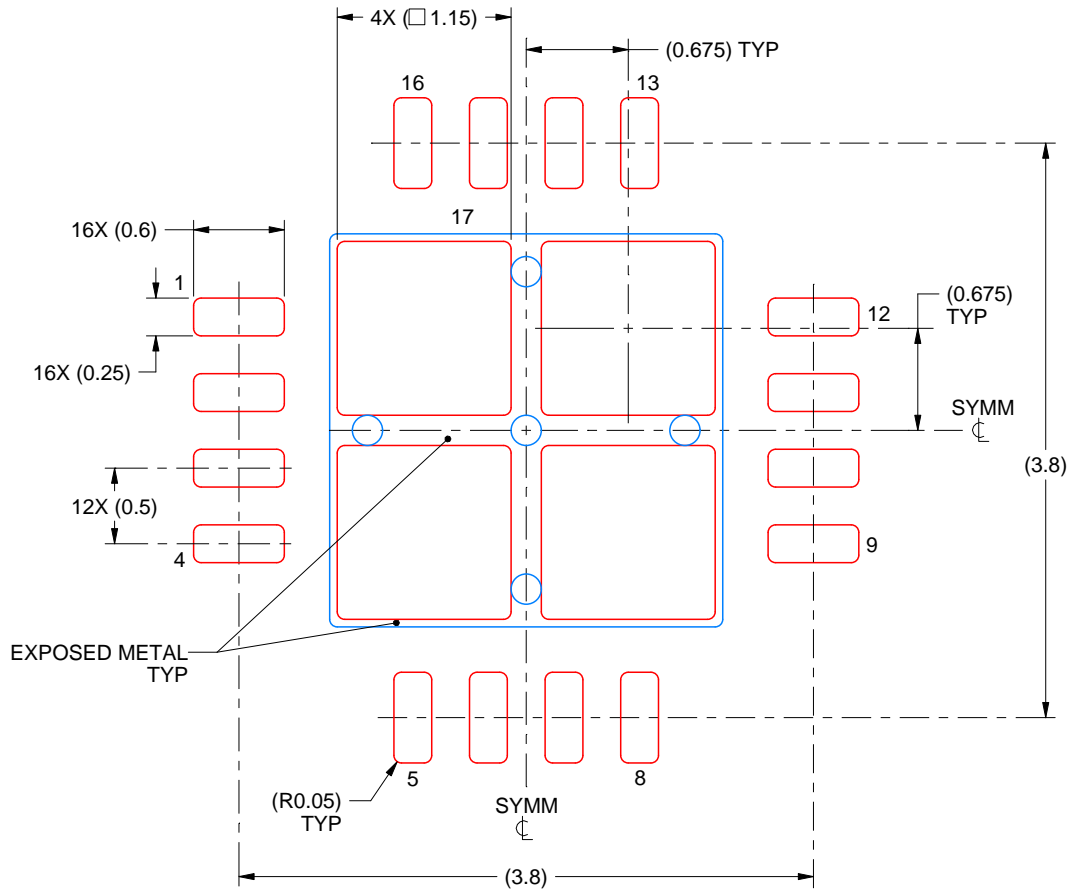


# EXAMPLE STENCIL DESIGN

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4214978/B 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated