

INA132

## Low Power, Single-Supply DIFFERENCE AMPLIFIER

### FEATURES

- LOW QUIESCENT CURRENT: 160 $\mu$ A
- WIDE SUPPLY RANGE  
Single Supply: 2.7V to 36V  
Dual Supplies:  $\pm 1.35$ V to  $\pm 18$ V
- LOW GAIN ERROR:  $\pm 0.075\%$  max
- LOW NONLINEARITY: 0.001% max
- HIGH CMR: 90dB
- HIGHLY VERSATILE CIRCUIT
- EASY TO USE
- LOW COST
- 8-PIN DIP AND SO-8 PACKAGES

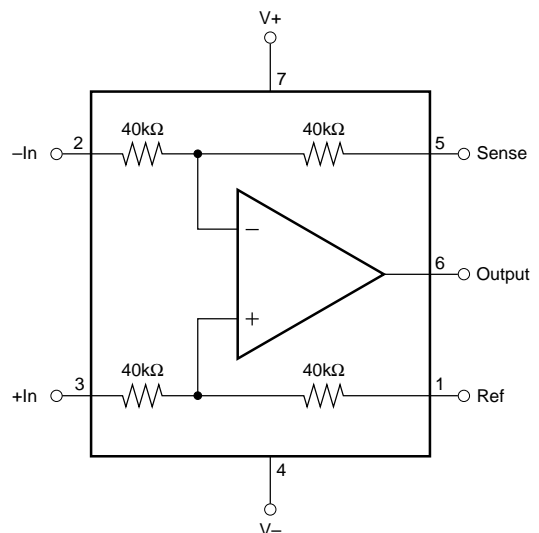
### APPLICATIONS

- DIFFERENTIAL INPUT AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- G = 1/2 AMPLIFIER
- G = 2 AMPLIFIER
- SUMMING AMPLIFIER
- DIFFERENTIAL CURRENT RECEIVER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- BATTERY-POWERED SYSTEMS
- GROUND LOOP ELIMINATOR

### DESCRIPTION

The INA132 is a low power, unity-gain differential amplifier consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The internal op amp's common-mode range extends to the negative supply—ideal for single-supply applications. It operates on single (2.7V to 36V) or dual supplies ( $\pm 1.35$ V to  $\pm 18$ V).

The differential amplifier is the foundation of many commonly used circuits. The INA132 provides this circuit function without using an expensive precision resistor network. The INA132 is available in 8-pin DIP and SO-8 surface-mount packages and is specified for operation over the extended industrial temperature range,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



# SPECIFICATIONS: $V_S = \pm 15V$

At  $T_A = +25^\circ C$ ,  $V_S = \pm 15V$ ,  $R_L = 10k\Omega$  connected to Ground, and Reference Pin connected to Ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA132P, U			INA132PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OFFSET VOLTAGE<sup>(1)</sup></b>	RTO							
Initial			±75	±250		*	±500	μV
vs Temperature			±1	±5		*	±10 <sup>(4)</sup>	μV/°C
vs Power Supply	$V_S = \pm 1.35V$ to $\pm 18V$		±5	±30		*	*	μV/V
vs Time			0.3			*		μV/mo
<b>INPUT IMPEDANCE<sup>(2)</sup></b>								
Differential			80			*		kΩ
Common-Mode			80			*		kΩ
<b>INPUT VOLTAGE RANGE</b>								
Common-Mode Voltage Range	$V_O = 0V$	(V-)		2(V+)-2	*		*	V
Common-Mode Rejection	$V_{CM} = -15V$ to $28V$ , $R_S = 0\Omega$	76	90		70	*		dB
<b>OUTPUT VOLTAGE NOISE<sup>(3)</sup></b>	RTO							
f = 0.1Hz to 10Hz			1.6			*		μVp-p
f = 1kHz			65			*		nV/√Hz
<b>GAIN</b>								
Initial			1			*		V/V
Error	$V_O = -14V$ to $13.5V$		±0.01	±0.075		*	±0.1	%
vs Temperature <sup>(4)</sup>			±1	±10		*	*	ppm/°C
vs Nonlinearity	$V_O = -14V$ to $13.5V$		±0.0001	±0.001		*	±0.002	% of FS
<b>OUTPUT</b>								
Voltage, Positive	$R_L = 100k\Omega$ to Ground	(V+)-1	(V+)-0.8		*	*		V
Negative	$R_L = 100k\Omega$ to Ground	(V-)+0.5	(V-)+0.15		*	*		V
Positive	$R_L = 10k\Omega$ to Ground	(V+)-1.5	(V+)-0.8		*	*		V
Negative	$R_L = 10k\Omega$ to Ground	(V-)+1	(V-)+0.25		*	*		V
Current Limit, Continuous to Common Capacitive Load (Stable Operation)			±12			*		mA
			10,000			*		pF
<b>FREQUENCY RESPONSE</b>								
Small Signal Bandwidth	-3dB		300			*		kHz
Slew Rate			0.1			*		V/μs
Settling Time: 0.1%	$V_O = 10V$ Step		85			*		μs
0.01%	$V_O = 10V$ Step		88			*		μs
Overload Recovery Time	50% Overdrive		7			*		μs
<b>POWER SUPPLY</b>								
Rated Voltage			±15			*		V
Voltage Range		±1.35		±18	*		*	V
Quiescent Current	$I_O = 0mA$		±160	±185		*	*	μA
<b>TEMPERATURE RANGE</b>								
Specification		-40		+85	*		*	°C
Operation		-55		+125	*		*	°C
Storage		-55		+125	*		*	°C
Thermal Resistance, $\theta_{JA}$								
8-Pin DIP			100			*		°C/W
SO-8 Surface-Mount			150			*		°C/W

\*Specifications the same as INA132P.

NOTES: (1) Includes effects of amplifier's input bias and offset currents. (2) 40kΩ resistors are ratio matched but have ±20% absolute value. (3) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network. (4) Guaranteed by wafer test to 95% confidence level.

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# SPECIFICATIONS: $V_S = +5V$

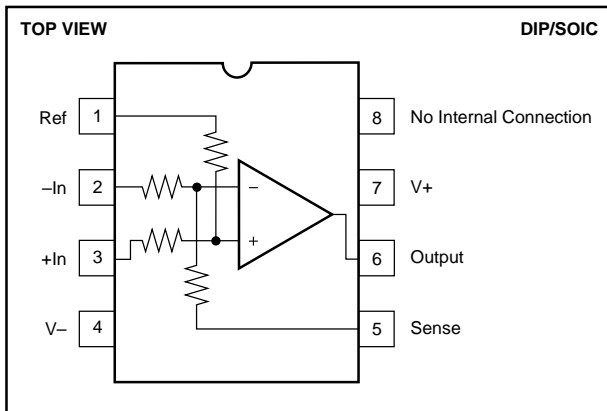
At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5V$ ,  $R_L = 10k\Omega$  connected to  $V_G/2$ , and Reference Pin connected to  $V_G/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	INA132P, U			INA132PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OFFSET VOLTAGE<sup>(1)</sup></b>	RTO							
Initial vs Temperature			$\pm 150$ $\pm 2$	$\pm 500$		*	$\pm 750$	$\mu\text{V}$ $\mu\text{V}/^\circ\text{C}$
<b>INPUT VOLTAGE RANGE</b>								
Common-Mode Voltage Range		0		$2(V+) - 2$	*		*	V
Common-Mode Rejection	$V_{CM} = 0V$ to $8V$ , $R_S = 0\Omega$	76	90		70	*		dB
<b>OUTPUT</b>								
Voltage, Positive	$R_L = 100k\Omega$	$(V+) - 1$	$(V+) - 0.75$		*	*		V
Negative	$R_L = 100k\Omega$	$+0.25$	$+0.06$		*	*		V
Positive	$R_L = 10k\Omega$	$(V+) - 1$	$(V+) - 0.8$		*	*		V
Negative	$R_L = 10k\Omega$	$+0.25$	$+0.12$		*	*		V
<b>POWER SUPPLY</b>								
Rated Voltage			+5		*	*		V
Voltage Range		+2.7		+36	*		*	V
Quiescent Current	$I_O = 0\text{mA}$		$\pm 155$	$\pm 185$		*	*	$\mu\text{A}$

\*Specifications the same as INA132P.

NOTE: (1) Include effects of amplifier's input bias and offset currents.

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V+$ to $V-$ .....	36V
Input Voltage Range .....	$\pm 80V$
Output Short-Circuit (to ground) .....	Continuous
Operating Temperature .....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Storage Temperature .....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature .....	$+150^\circ\text{C}$
Lead Temperature (soldering, 10s) .....	$+300^\circ\text{C}$

## ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	TEMPERATURE RANGE
INA132PA	8-Pin Plastic DIP	006	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
INA132P	8-Pin Plastic DIP	006	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
INA132UA	SO-8 Surface-Mount	182	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
INA132U	SO-8 Surface-Mount	182	$-40^\circ\text{C}$ to $+85^\circ\text{C}$

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

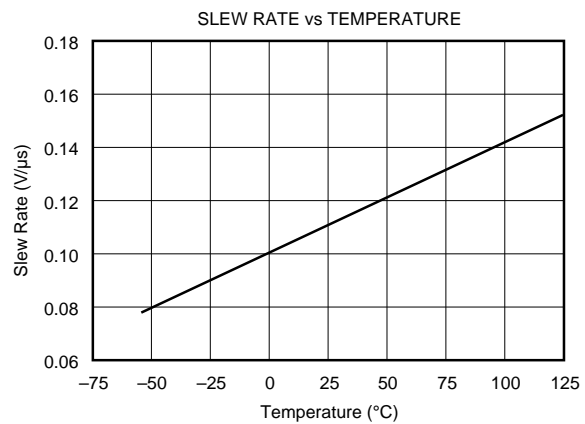
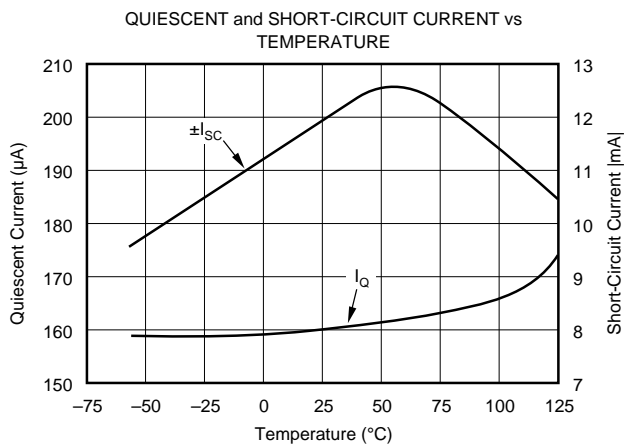
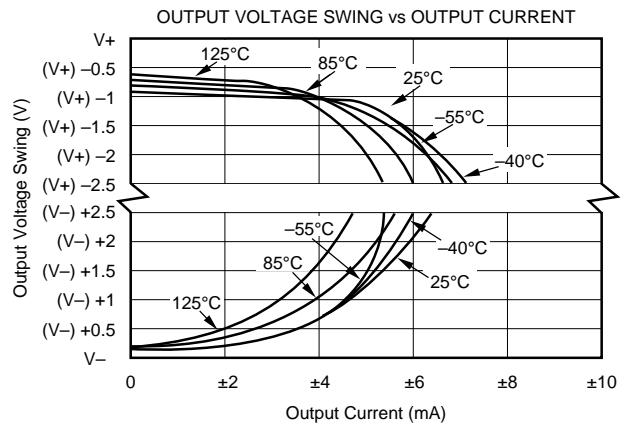
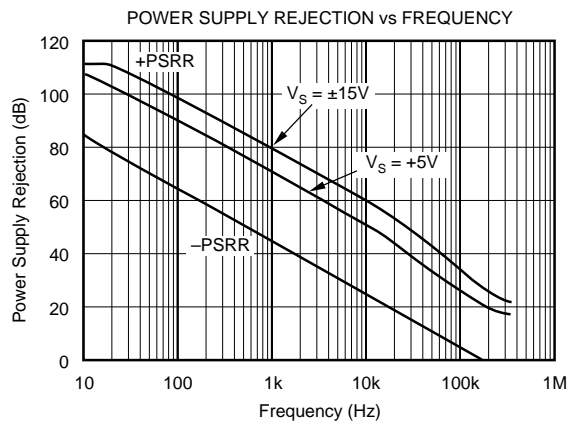
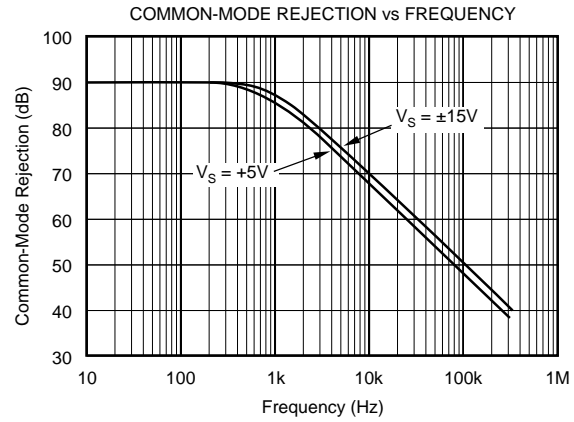
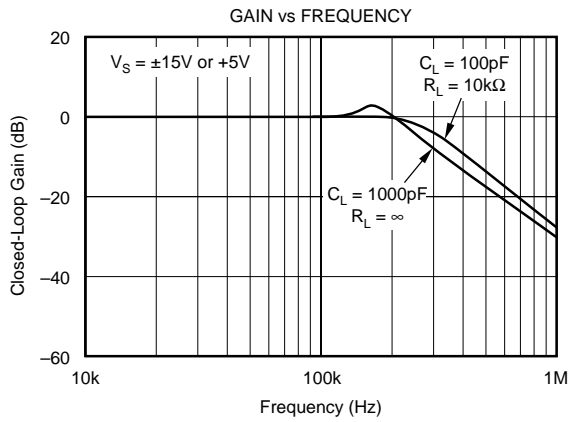
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# TYPICAL PERFORMANCE CURVES

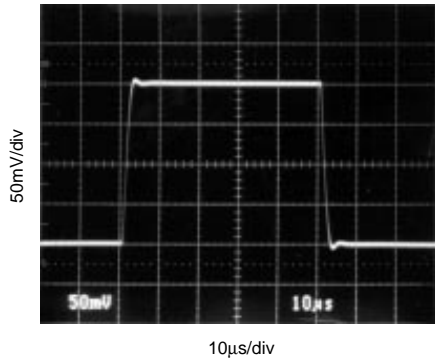
At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



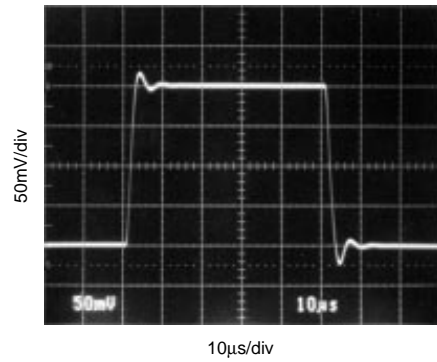
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

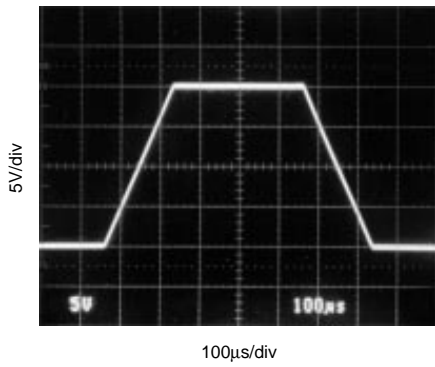
SMALL-SIGNAL STEP RESPONSE  
 $C_L = 200\text{pF}$



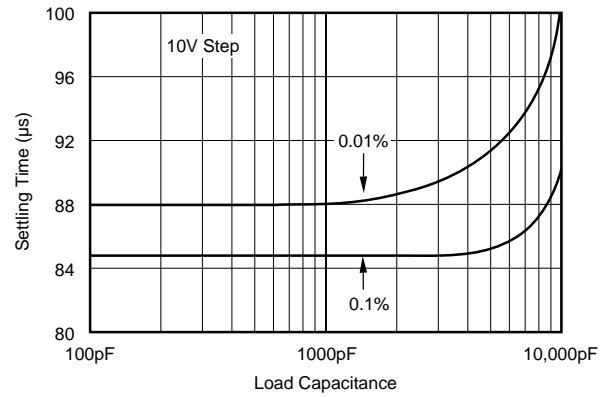
SMALL-SIGNAL STEP RESPONSE  
 $C_L = 1000\text{pF}$



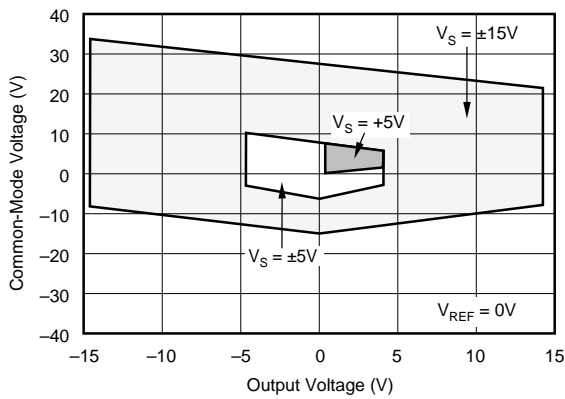
LARGE-SIGNAL STEP RESPONSE



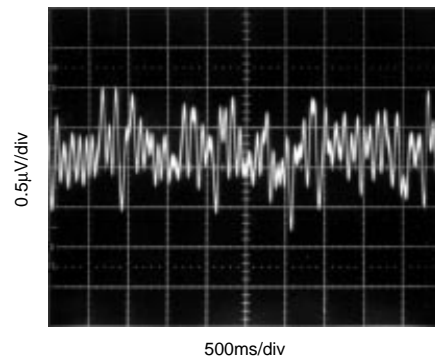
SETTLING TIME vs LOAD CAPACITANCE



INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE

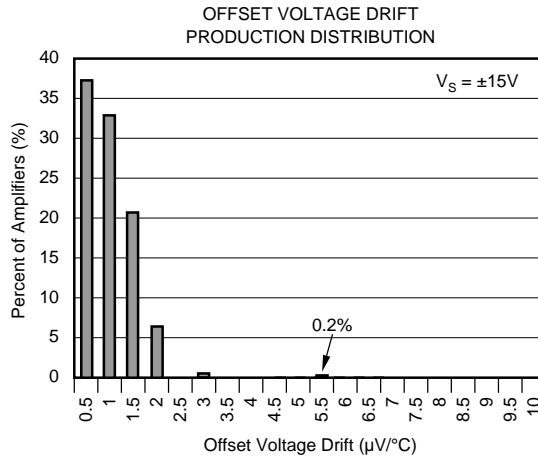
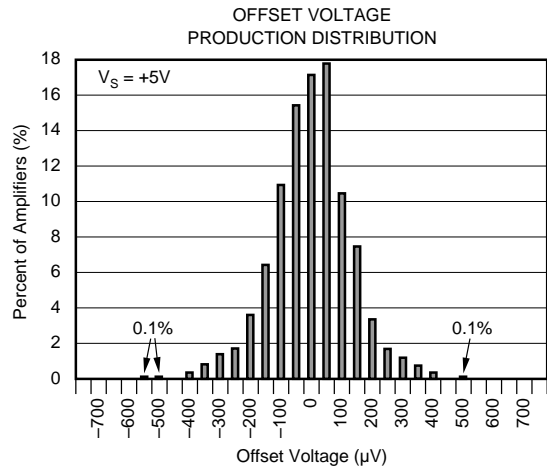
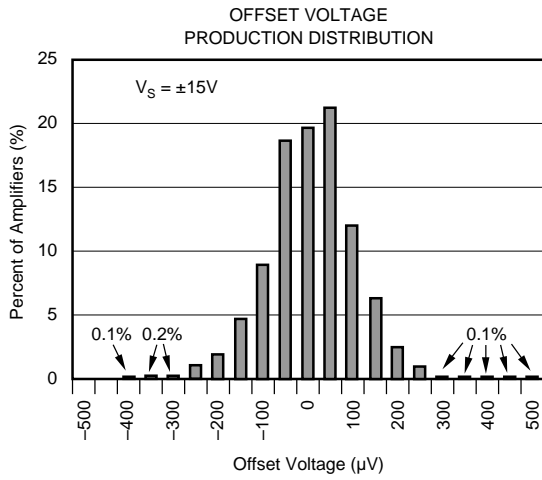


0.1 to 10Hz PEAK-TO-PEAK VOLTAGE NOISE



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



## APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA132. Power supply bypass capacitors should be connected close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. An  $8\Omega$  mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 80dB. Gain accuracy will also be slightly affected. If the source has a known impedance mismatch, an additional resistor in series with one input can be used to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance. As shown in Figure 1, measurements should be sensed at the load.

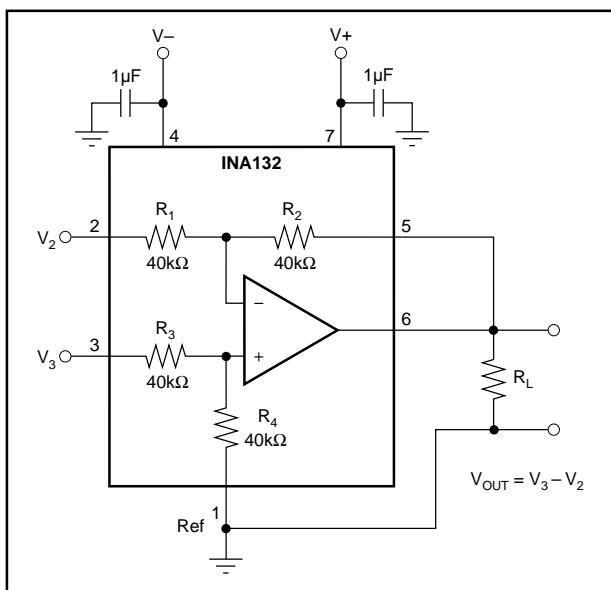


FIGURE 1. Basic Power Supply and Signal Connections.

### OPERATING VOLTAGE

The INA132 operates from single (+2.7V to +36V) or dual ( $\pm 1.35V$  to  $\pm 18V$ ) supplies with excellent performance. Specifications are production tested with +5V and  $\pm 15V$  supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

The internal op amp in the INA132 is a single-supply design. This allows linear operation with the op amp's common-mode voltage equal to, or slightly below  $V^-$  (or single

supply ground). Although input voltages on pins 2 and 3 that are below the negative supply voltage will not damage the device, operation in this region is not recommended. Transient conditions at the inverting input terminal below the negative supply can cause a positive feedback condition that could lock the INA132's output to the negative rail.

The INA132 can accurately measure differential signals that are above the positive power supply. Linear common-mode range extends to nearly twice the positive power supply voltage—see typical performance curve, Common-Mode Range vs Output Voltage.

### OFFSET VOLTAGE TRIM

The INA132 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage. The source impedance of a signal applied to the Ref terminal should be less than  $8\Omega$  to maintain good common-mode rejection. To assure low impedance at the Ref terminal, the trim voltage can be buffered with an op amp, such as the OPA177.

### CAPACITIVE LOAD DRIVE CAPABILITY

The INA132 can drive large capacitive loads, even at low supplies. It is stable with a 10,000pF load. Refer to the "Small-Signal Step Response" and "Settling Time vs Load Capacitance" typical performance curves.

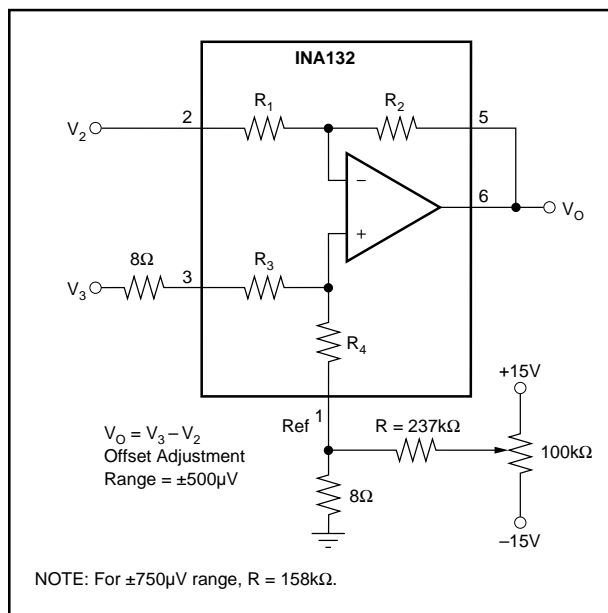


FIGURE 2. Offset Adjustment.

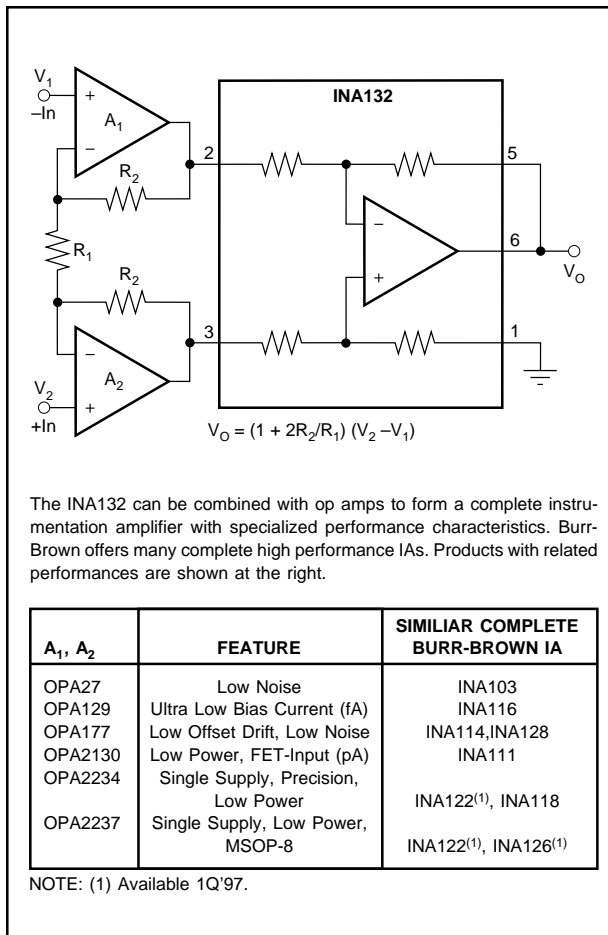


FIGURE 3. Precision Instrumentation Amplifier.

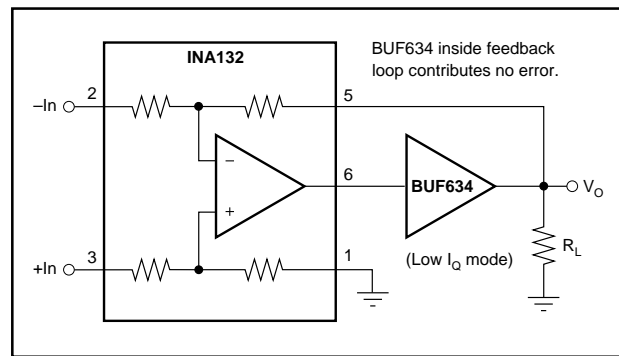


FIGURE 4. Low Power, High Output Current Precision Difference Amplifier.

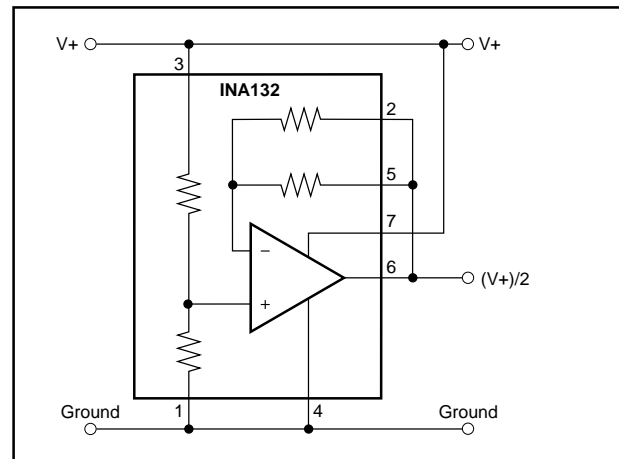


FIGURE 5. Pseudoground Generator.

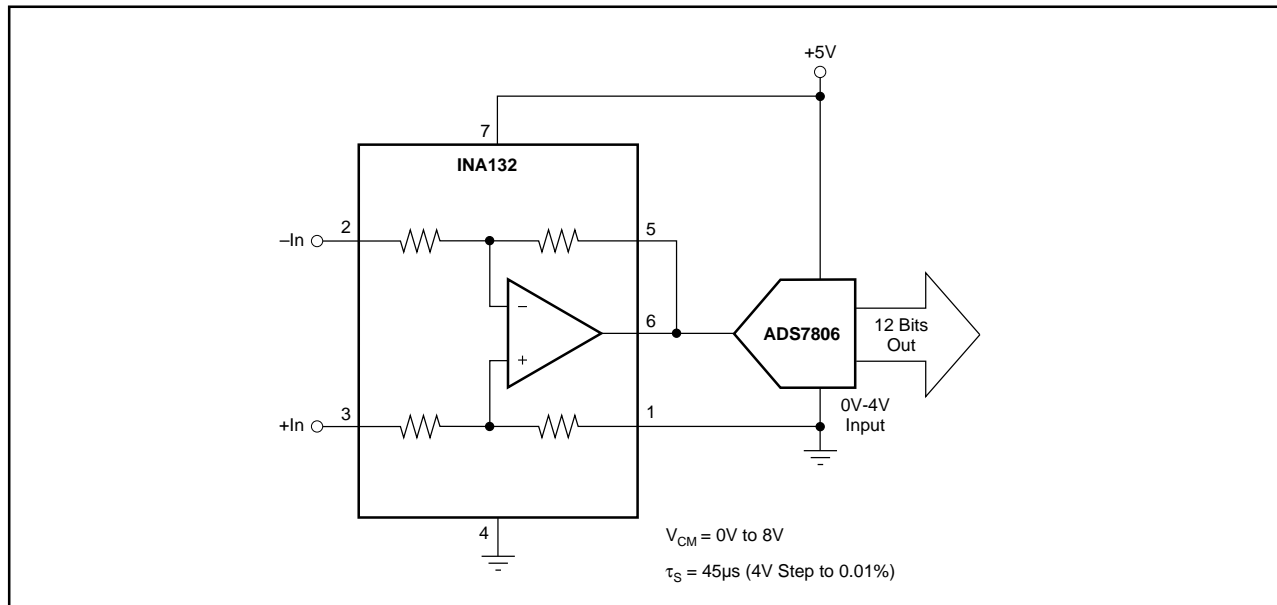


FIGURE 6. Differential Input Data Acquisition.



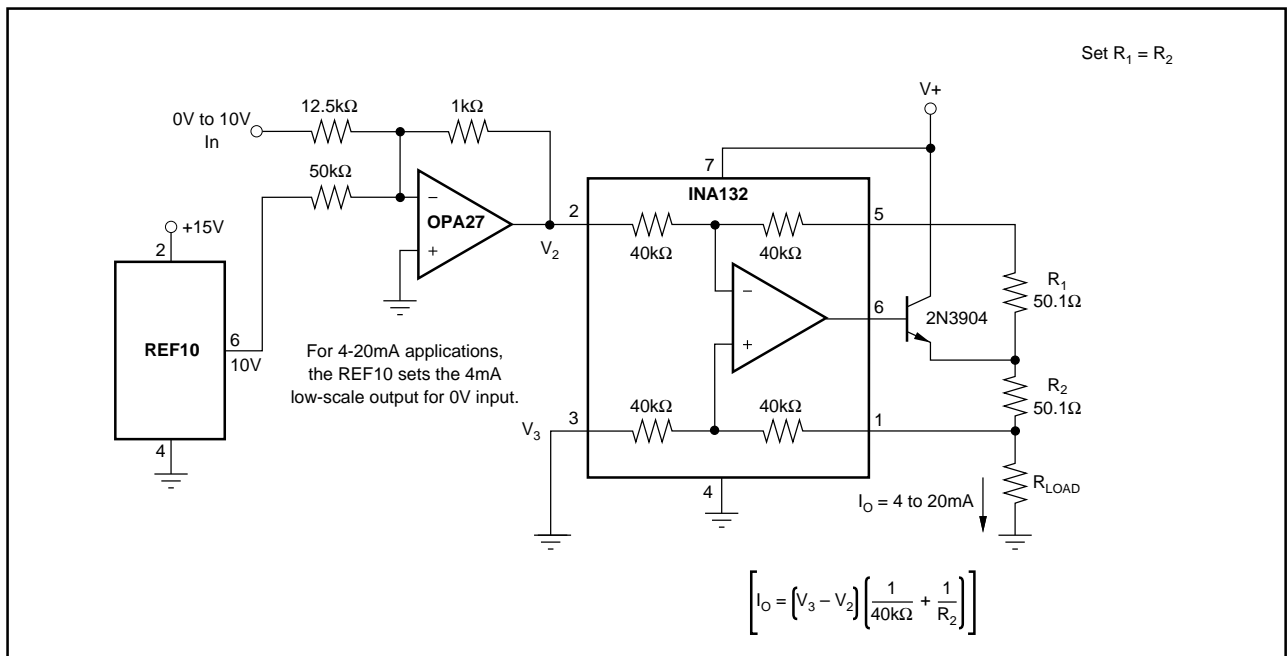


FIGURE 7. Precision Voltage-to-Current Conversion.

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- $\pm 10V$  Precision Voltage Reference
- $\pm 5V$  Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision  $G = 2$  Amplifier
- Precision Summing Amplifier
- Precision  $G = 1/2$  Amplifier
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator
- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low  $I_{OUT}$
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of  $\pm 1$  Amplifier

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
INA132P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
INA132PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
INA132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

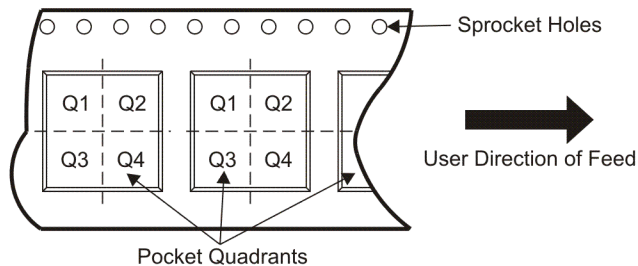
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA132U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
INA132UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA132U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 132U	<a href="#">Samples</a>
INA132U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 132U	<a href="#">Samples</a>
INA132U/2K5E4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI			<a href="#">Samples</a>
INA132UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 132U A	<a href="#">Samples</a>
INA132UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 132U A	<a href="#">Samples</a>
INA132UA/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 132U A	<a href="#">Samples</a>
INA132UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 132U A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA132U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA132UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA132U	D	SOIC	8	75	506.6	8	3940	4.32
INA132UA	D	SOIC	8	75	506.6	8	3940	4.32
INA132UAE4	D	SOIC	8	75	506.6	8	3940	4.32

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