



## microPower, Single-Supply, CMOS INSTRUMENTATION AMPLIFIER

### FEATURES

- LOW COST
- LOW QUIESCENT CURRENT: 40µA/channel  
Shut Down: < 1µA
- HIGH GAIN ACCURACY: G = 5, 0.07%, 2ppm/°C
- GAIN SET WITH EXTERNAL RESISTORS
- LOW BIAS CURRENT: 10pA
- BANDWIDTH: 500kHz, G = 5V/V
- RAIL-TO-RAIL OUTPUT SWING: (V+) – 0.02V
- WIDE TEMPERATURE RANGE:  
–55°C to +125°C
- SINGLE VERSION IN MSOP-8 PACKAGE AND  
DUAL VERSION IN TSSOP-14 PACKAGE

### APPLICATIONS

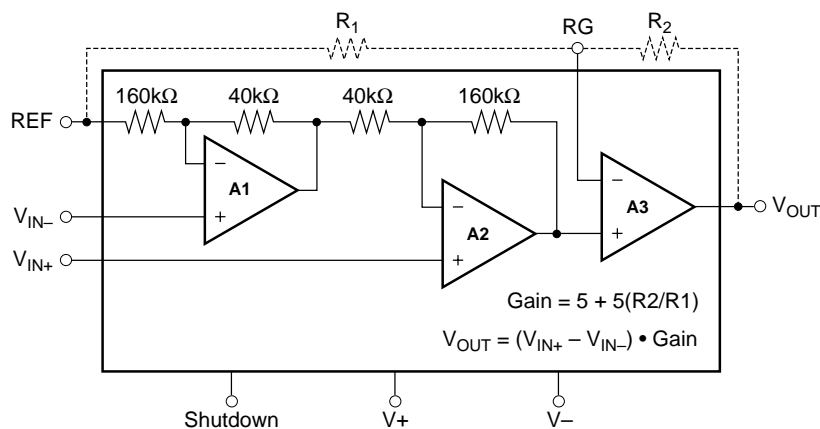
- INDUSTRIAL SENSOR AMPLIFIERS:  
Bridge, RTD, Thermistor, Position
- PHYSIOLOGICAL AMPLIFIERS:  
ECG, EEG, EMG
- A/D CONVERTER SIGNAL CONDITIONING
- DIFFERENTIAL LINE RECEIVERS WITH GAIN
- FIELD UTILITY METERS
- PCMCIA CARDS
- COMMUNICATION SYSTEMS
- TEST EQUIPMENT
- AUTOMOTIVE INSTRUMENTATION

### DESCRIPTION

The INA322 family is a series of low cost, rail-to-rail output, micropower CMOS instrumentation amplifiers that offer wide-range, single-supply, as well as bipolar-supply operation. The INA322 family provides low-cost, low-noise amplification of differential signals with micropower current consumption of 40µA. When shutdown the INA322 has a quiescent current of less than 1µA. Returning to normal operations within microseconds, the shutdown feature makes the INA322 optimal for low-power battery or multiplexing applications.

Configured internally for 5V/V gain, the INA322 offers exceptional flexibility with user-programmable external gain resistors. The INA322 reduces common-mode error over frequency and with CMRR remaining high up to 3kHz, line noise and line harmonics are rejected.

The low-power design does not compromise on bandwidth or slew rate, making the INA322 ideal for driving sampling Analog-to-Digital (A/D) converters as well as general-purpose applications. With high precision, low cost, and small packaging, the INA322 outperforms discrete designs, while offering reliability and performance.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V-.....	7.5V
Signal Input Terminals, Voltage <sup>(2)</sup> ..... (V-) - 0.5V to (V+) + 0.5V	
Current <sup>(2)</sup> .....	10mA
Output Short-Circuit <sup>(3)</sup> .....	Continuous
Operating Temperature.....	-65°C to +150°C
Storage Temperature.....	-65°C to +150°C
Junction Temperature.....	+150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

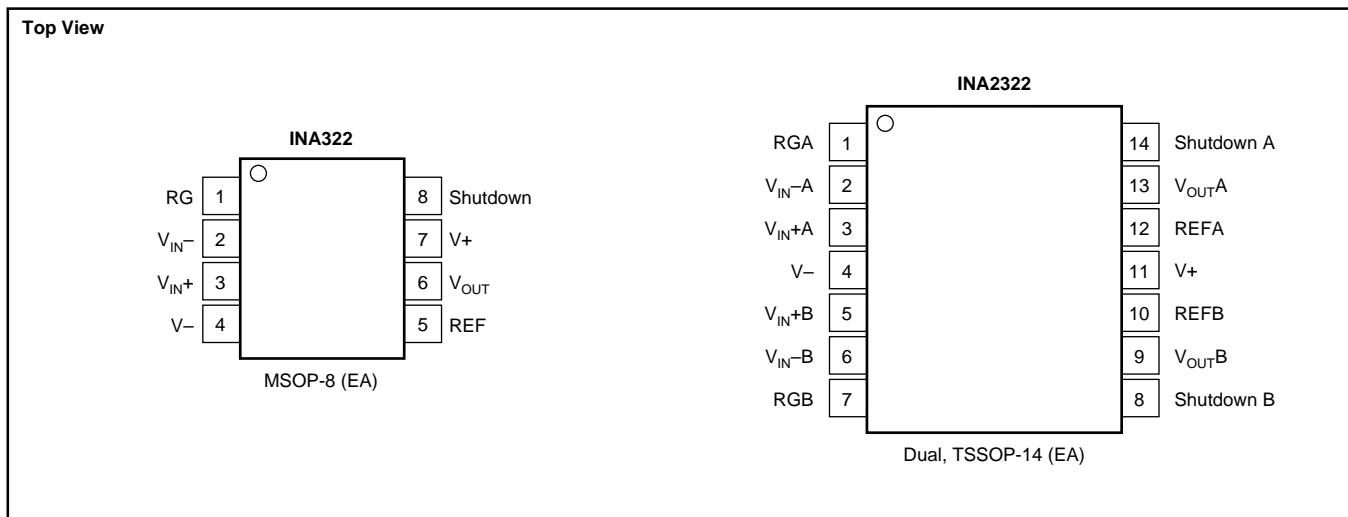
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
<b>SINGLE</b> INA322EA	MSOP-8	DGK	C22
<b>DUAL</b> INA2322EA	TSSOP-14	PW	INA2322EA

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS



# ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$ TO $+5.5V$

**BOLDFACE** limits apply over the specified temperature range,  $T_A = -55^{\circ}C$  TO  $+125^{\circ}C$

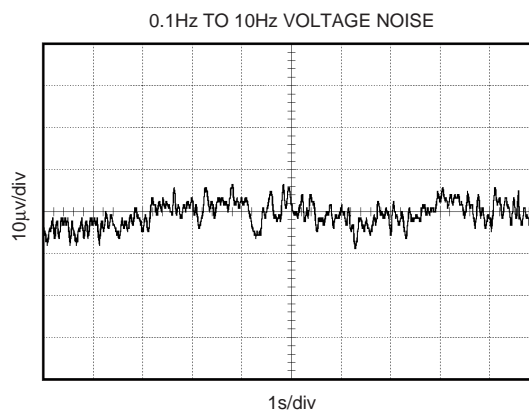
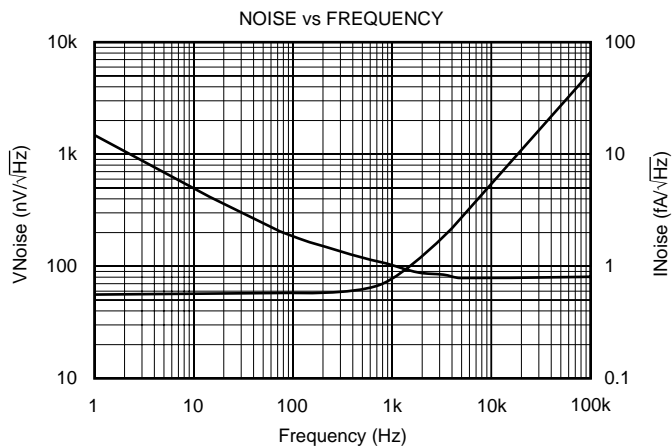
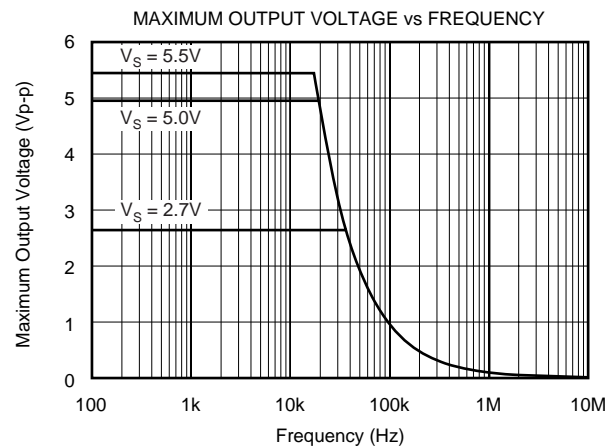
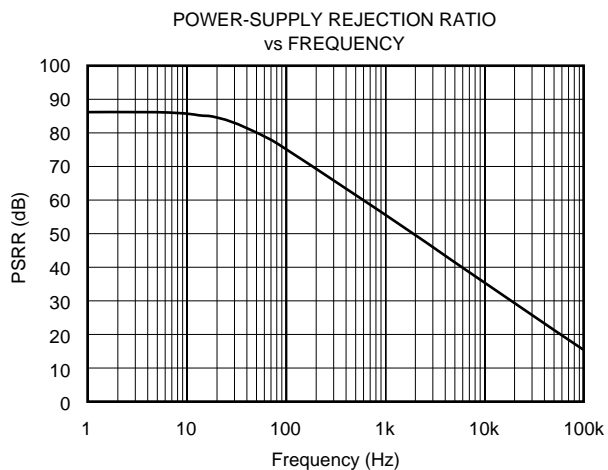
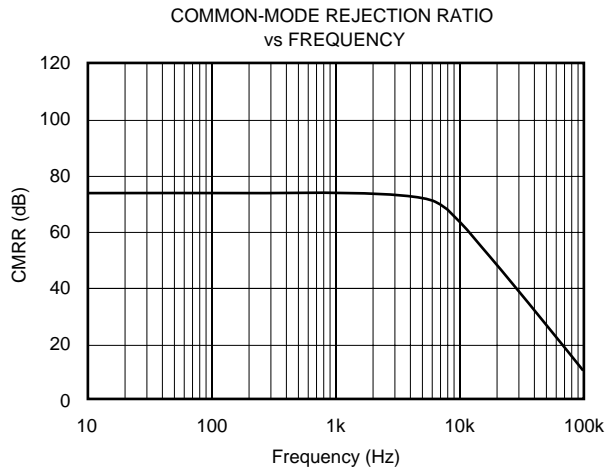
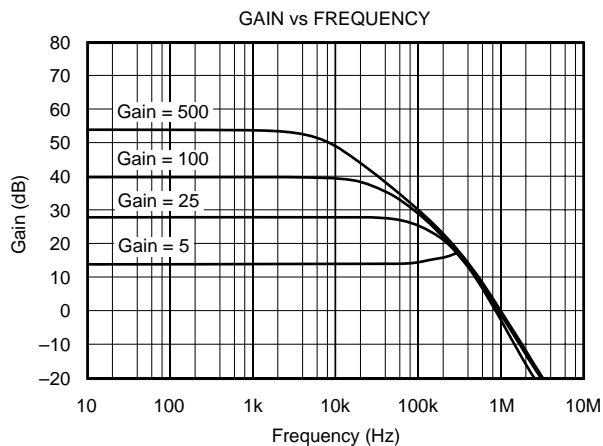
At  $T_A = +25^{\circ}C$ ,  $R_L = 25k\Omega$ ,  $G = 25$ , and  $I_A$  common =  $V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	INA322EA INA2322EA			UNITS
		MIN	TYP	MAX	
<b>INPUT</b> Input Offset Voltage, RTI <b>Over Temperature</b> <b>vs Temperature</b> vs Power Supply <b>Over Temperature</b> Long-Term Stability Input Impedance Input Common-Mode Range	$V_S = +5V$  $V_S = +2.7V$ to $+5.5V$  $V_S = 2.7V$ $V_S = 5V$		$\pm 2$  $\pm 7$ $\pm 50$  $\pm 0.4$ $10^{13} \parallel 3$	$\pm 10$  $\pm 11$  $\pm 250$ <b><math>\pm 260</math></b>	mV mV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$ $\mu V/month$ $\Omega \parallel pF$ V
Common-Mode Rejection <b>Over Temperature</b>  Crosstalk, Dual	CMRR $V_S = 5V, V_{CM} = 0.55V$ to $3.8V$ <b><math>V_S = 5V, V_{CM} = 0.55V</math> to <math>3.8V</math></b> $V_S = 2.7V, V_{CM} = 0.35V$ to $1.5V$	0.35 0.55 <b>60</b> <b>60</b>	73  73 110	1.5 3.8	V dB dB dB
<b>INPUT BIAS CURRENT</b> Bias Current Offset Current			$\pm 0.5$ $\pm 0.5$	$\pm 10$ $\pm 10$	pA pA
<b>NOISE, RTI</b> Voltage Noise: $f = 10Hz$ $f = 100Hz$ $f = 1kHz$ $f = 0.1Hz$ to $10Hz$ Current Noise: $f = 1kHz$	$R_S = 0\Omega$		500 190 100 20 3		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $\mu Vp-p$ $fA/\sqrt{Hz}$
<b>GAIN<sup>(1)</sup></b> Gain Equation, Externally Set Range of Gain Gain Error <b>vs Temperature</b> Nonlinearity <b>Over Temperature</b>	$G > 5$  <b><math>G = 5</math></b> $G = 25, V_S = 5V, V_O = 0.05$ to $4.95$	5	$G = 5 + 5(R2/R1)$  $\pm 0.07$ <b><math>\pm 2</math></b> $\pm 0.001$ <b><math>\pm 0.002</math></b>	1000 $\pm 0.4$ <b><math>\pm 10</math></b> $\pm 0.010$ <b><math>\pm 0.015</math></b>	V/V % ppm/ $^{\circ}C$ % of FS % of FS
<b>OUTPUT</b> Output Voltage Swing from Rail <sup>(2, 5)</sup> <b>Over Temperature</b> Capacitance Load Drive Short-Circuit Current	$G \geq 10$	50 <b>50</b>	25  See Typical Characteristic <sup>(3)</sup> 8 16		mV mV pF mA
<b>FREQUENCY RESPONSE</b> Bandwidth, $-3dB$ Slew Rate Settling Time, 0.1% 0.01% Overload Recovery	BW SR $t_S$  50% Input Overload $G = 25$	$G = 5$  $V_S = 5V, G = 25$ $G = 5, C_L = 50pF, V_O = 2V$ step	500 0.4 8 12 2		kHz V/ $\mu s$ $\mu s$ $\mu s$ $\mu s$
<b>POWER SUPPLY</b> Specified Voltage Range Operating Voltage Range Quiescent Current per Channel <b>Over Temperature</b> Shutdown Quiescent Current/Chan	$I_Q$  $I_{SD}$	$V_{SD} > 2.5^{(4)}$  $V_{SD} < 0.8^{(4)}$	+2.7  +2.5 to +5.5 40 0.01	+5.5  60 <b>70</b> 1	V V $\mu A$ $\mu A$ $\mu A$
<b>TEMPERATURE RANGE</b> Specified Range Operating/Storage Range Thermal Resistance	$\theta_{JA}$ MSOP-8, TSSOP-14 Surface Mount	-55 -65		+125 +150	$^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$

NOTES: (1) Does not include errors from external gain setting resistors (2) Output voltage swings are measured between the output and power-supply rails. Output swings and rail only if  $G \geq 10$ . (3) See typical characteristic *Percent Overshoot vs Load Capacitance*. (4) See typical characteristic *Shutdown Voltage vs Supply Voltage*. (5) Output does not swing to positive rail if gain is less than 10.

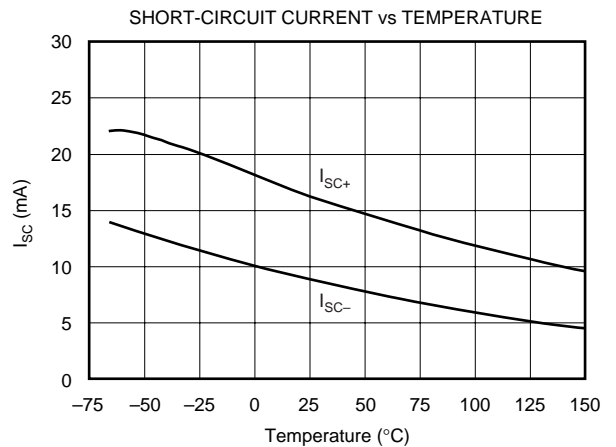
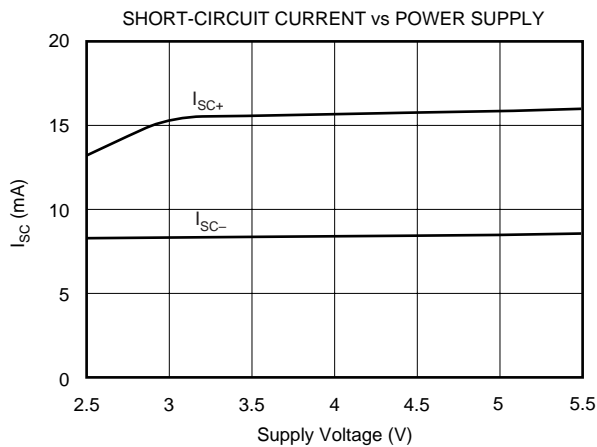
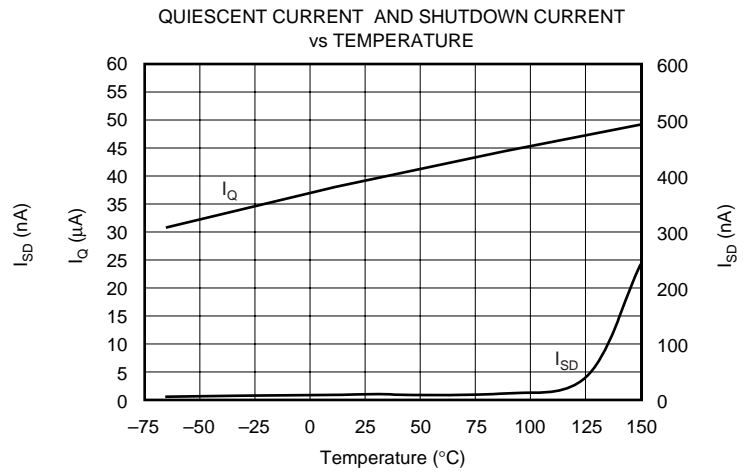
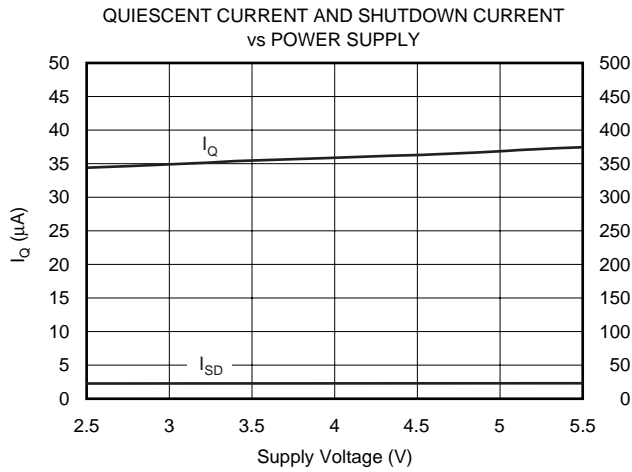
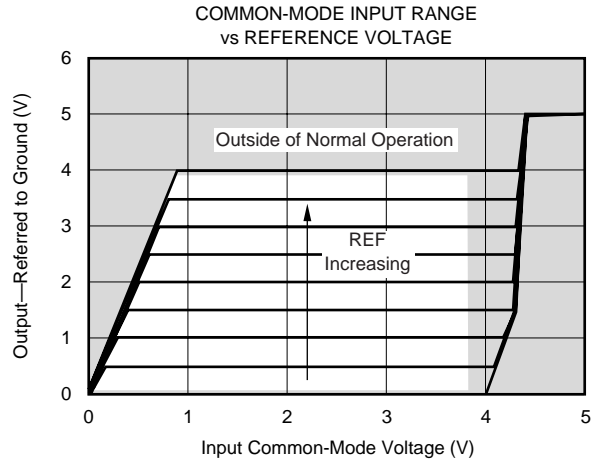
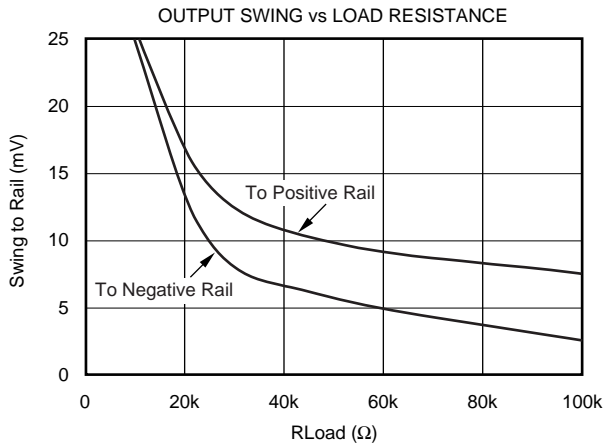
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = 1/2V_S$ ,  $R_L = 25\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

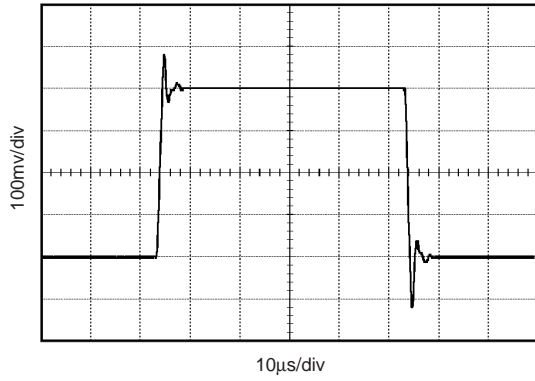
At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{\text{CM}} = 1/2V_S$ ,  $R_L = 25\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , unless otherwise noted.



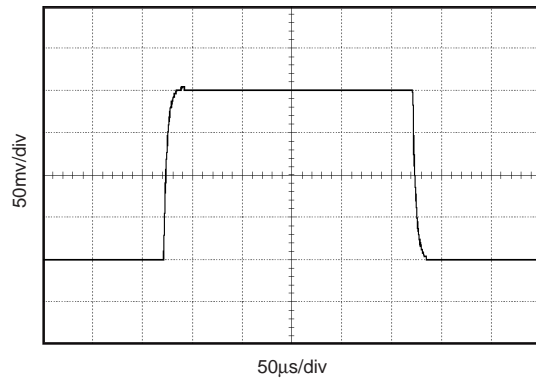
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{\text{CM}} = 1/2V_S$ ,  $R_L = 25\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , unless otherwise noted.

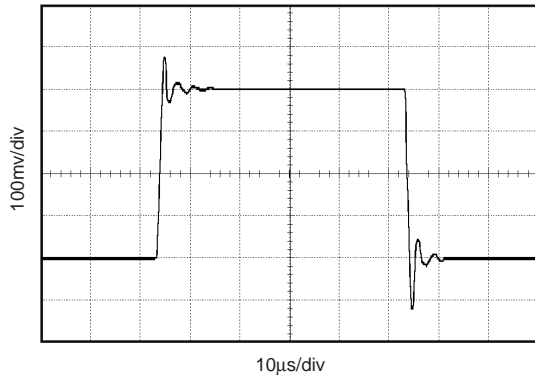
SMALL-SIGNAL STEP RESPONSE ( $G = 5$ )



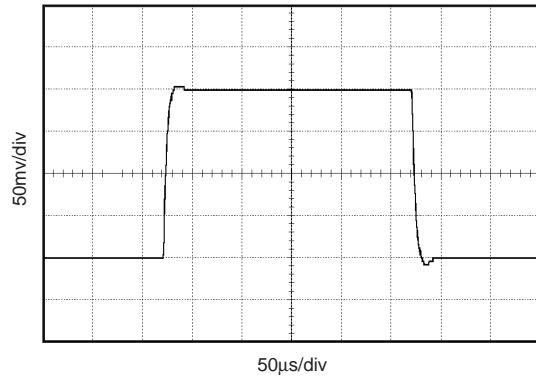
SMALL-SIGNAL STEP RESPONSE ( $G = 100$ )



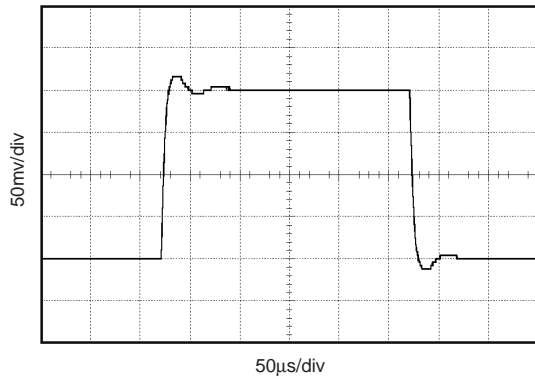
SMALL-SIGNAL STEP RESPONSE  
( $G = 5$ ,  $C_L = 1000\text{pF}$ )



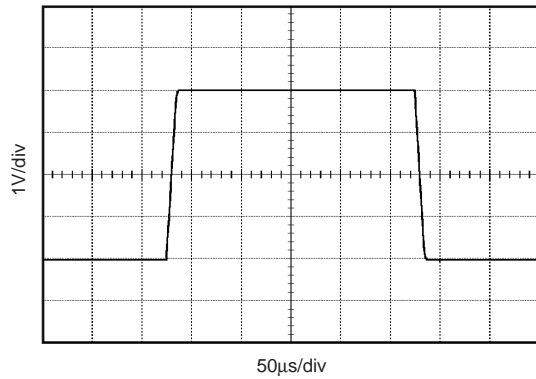
SMALL-SIGNAL STEP RESPONSE  
( $G = 100$ ,  $C_L = 1000\text{pF}$ )



SMALL-SIGNAL STEP RESPONSE  
( $G = 100$ ,  $C_L = 5000\text{pF}$ )

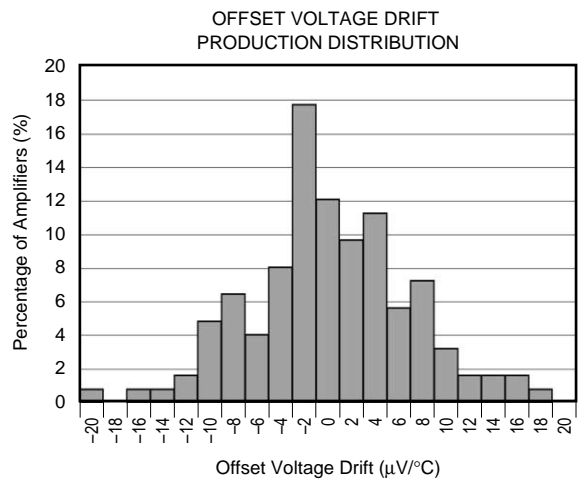
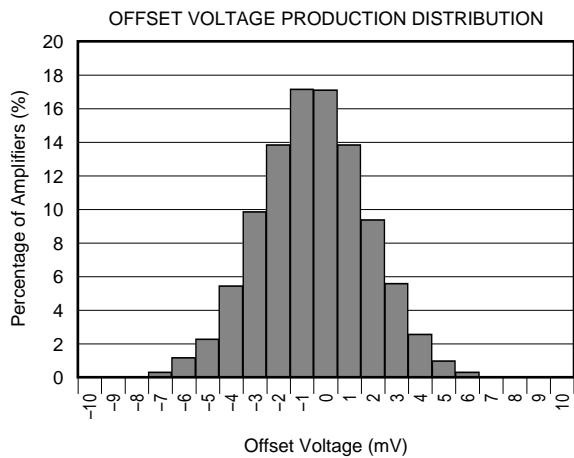
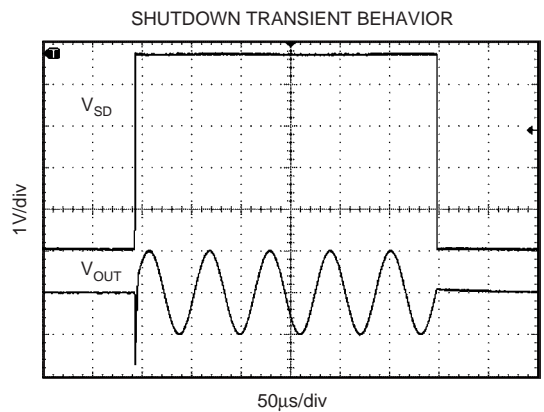
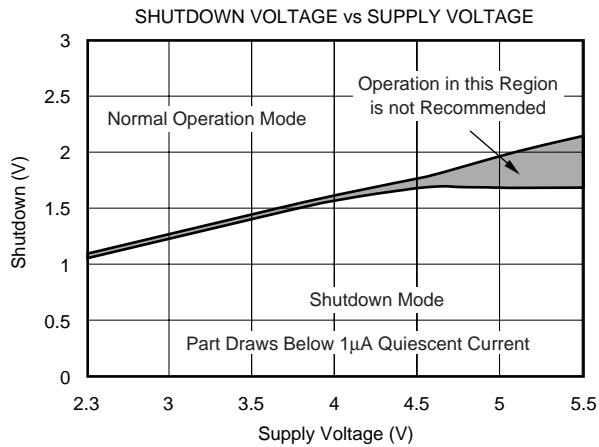
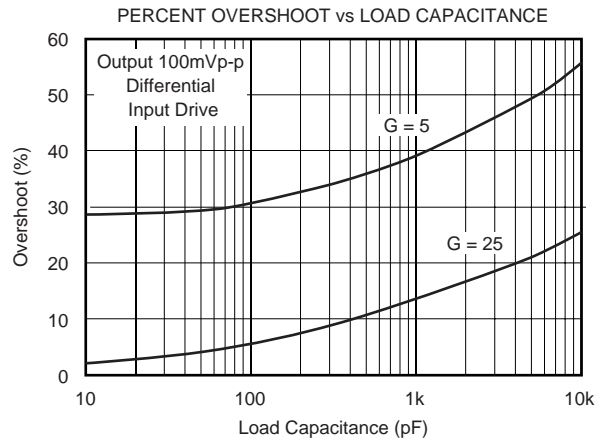
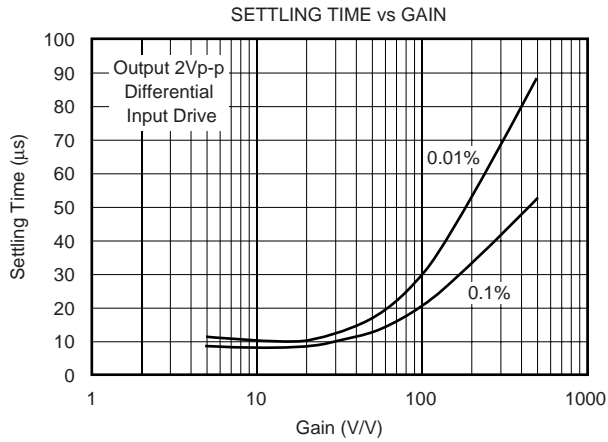


LARGE-SIGNAL STEP RESPONSE  
( $G = 25$ ,  $C_L = 50\text{pF}$ )



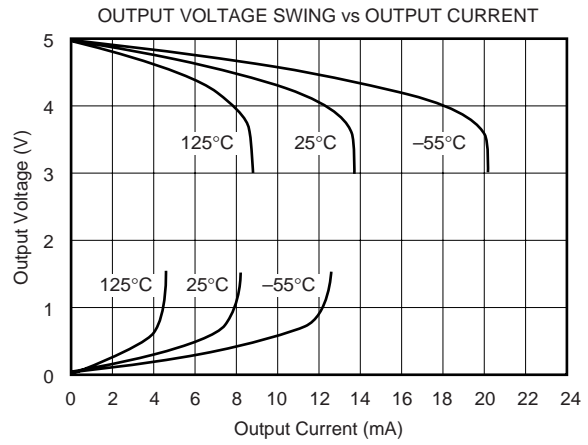
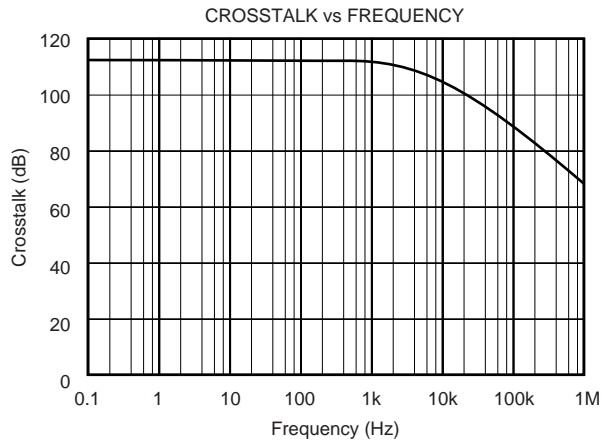
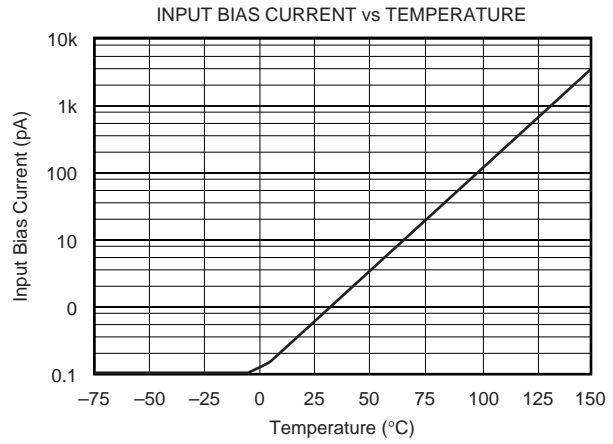
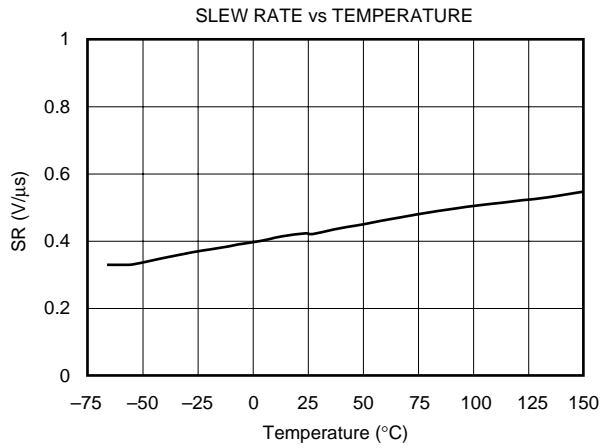
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = 1/2V_S$ ,  $R_L = 25\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = 1/2V_S$ ,  $R_L = 25\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , unless otherwise noted.





# APPLICATIONS INFORMATION

The INA322 is a modified version of the classic “two op amp” instrumentation amplifier, with an additional gain amplifier.

Figure 1 shows the basic connections for the operation of the INA322 and INA2322. The power supply should be capacitively decoupled with 0.1µF capacitors as close to the INA322 as possible for noisy or high-impedance applications.

The output is referred to the reference terminal, which must be at least 1.2V below the positive supply rail.

# OPERATING VOLTAGE

The INA322 family is fully specified over a supply range of +2.7V to +5.5V, with key parameters specified over the temperature range of -55°C to +125°C. Parameters that vary significantly with operating conditions, such as load conditions or temperature, are shown in the Typical Characteristic Curves.

The INA322 may be operated on a single supply. Figure 2 shows a bridge amplifier circuit operated from a single +5V supply. The bridge provides a small differential voltage riding on an input common-mode voltage.

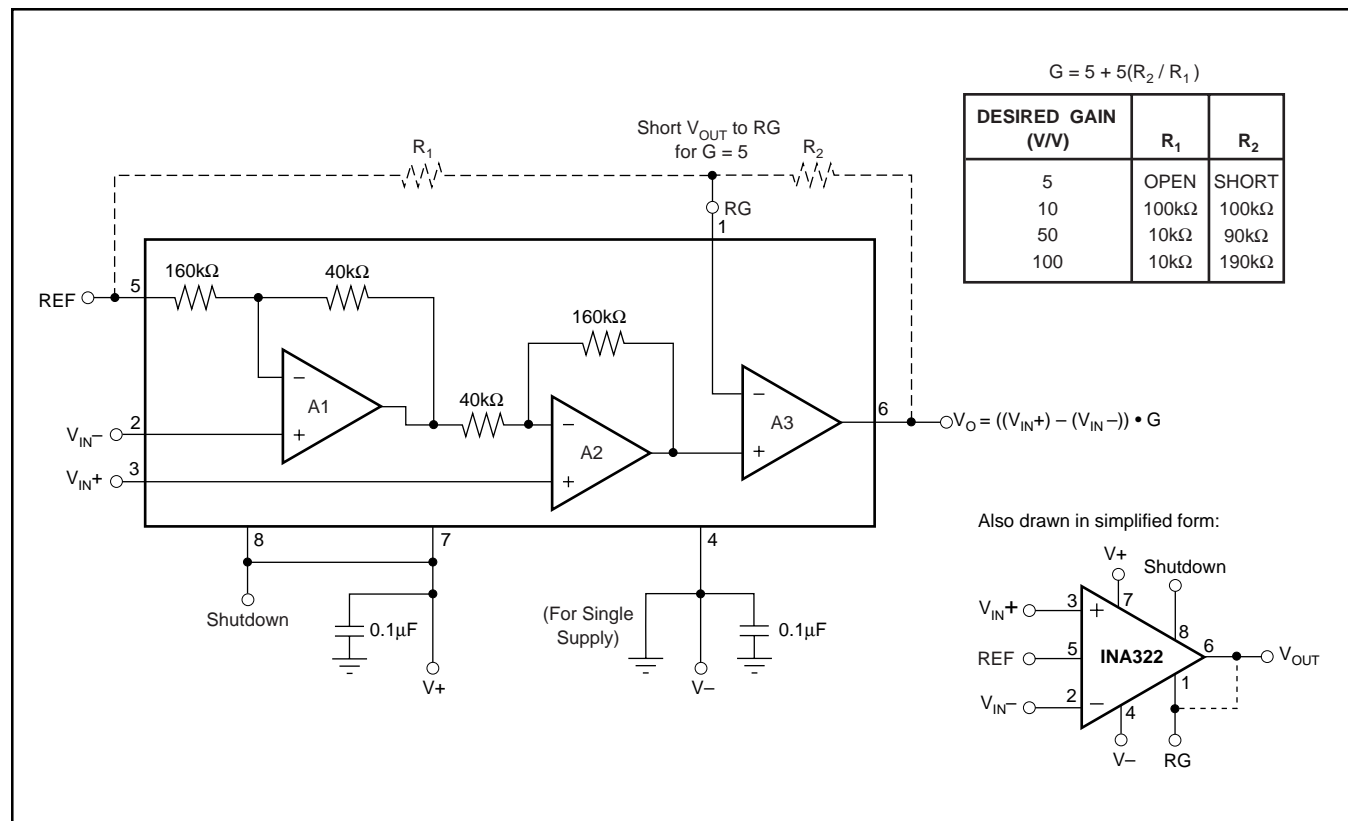


FIGURE 1. Basic Connections.

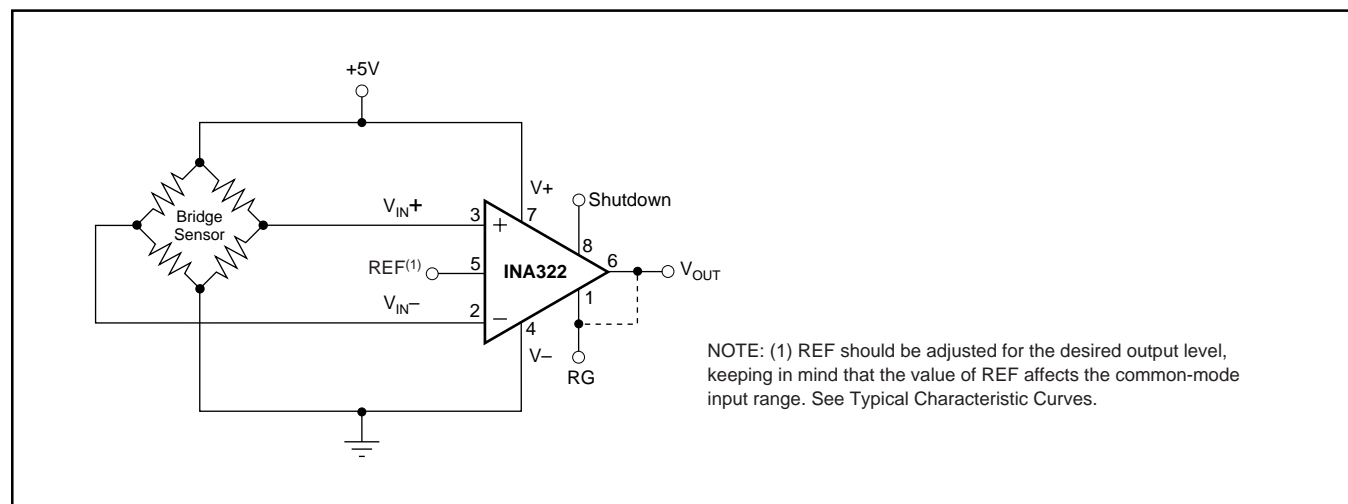


FIGURE 2. Bridge Amplifier of the INA322.

## SETTING THE GAIN

The ratio of  $R_2$  to  $R_1$ , or the impedance between pins 1, 5, and 6, determines the gain of the INA322. With an internally set gain of 5, the INA322 can be programmed for gains greater than 5 according to the following equation:

$$G = 5 + 5(R_2/R_1)$$

The INA322 is designed to provide accurate gain, with gain error specified to be less than 0.4%. Setting gain with matching TC resistors will minimize gain drift. Errors from external resistors will add directly to the error, and may become dominant error sources.

## INPUT COMMON-MODE RANGE

The upper limit of the common mode input range is set by the common-mode input range of the second amplifier, A2, to 1.2V below positive supply. Under most conditions, the amplifier operates beyond this point with reduced performance. The lower limit of the input range is bounded by the output swing of amplifier A1, and is a function of the reference voltage according to the following equation:

$$V_{OA1} = 5/4 V_{CM} - 1/4 V_{REF}$$

(See Typical Characteristic Curves for Input Common-Mode Range vs Reference Voltage).

## REFERENCE

The reference terminal defines the zero output voltage level. In setting the reference voltage, the common mode input of A3 should be considered according to the following equation:

$$V_{OA2} = V_{REF} + 5(V_{IN+} - V_{IN-})$$

$V_{OA2}$  should be less than  $V_{DD} - 1.2V$ .

The reference pin requires a low-impedance connection. Any resistance in series with the reference pin will degrade the CMRR. The reference pin may be used to compensate for the offset voltage (see Offset Trimming section). The reference voltage level also influences the common-mode input range (see Common-Mode Input Range section).

## INPUT BIAS CURRENT RETURN

With a high input impedance of  $10^{13}\Omega$ , the INA322 is ideal for use with high-impedance sources. The input bias current of less than 10pA makes the INA322 nearly independent of input impedance and ideal for low-power applications.

For proper operation, a path must be provided for input bias currents for both inputs. Without input bias current paths, the inputs will “float” to a potential that exceeds common-

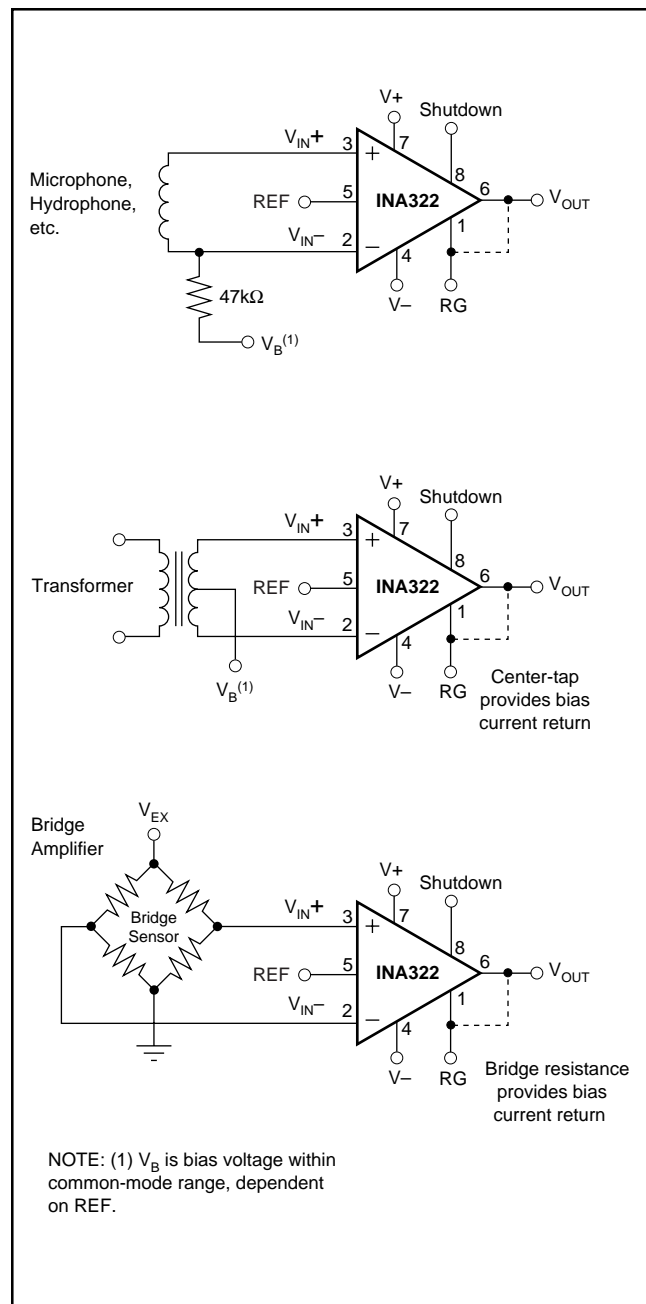


FIGURE 3. Providing an Input Common-Mode Path.

mode range and the input amplifier will saturate. Figure 3 shows how bias current path can be provided in the cases of microphone applications, thermistor applications, ground returns, and dc-coupled resistive bridge applications.

When differential source impedance is low, the bias current return path can be connected to one input. With higher source impedance, two equal resistors will provide a balanced input. The advantages are lower input offset voltage due to bias current flowing through the source impedance and better high-frequency gain.

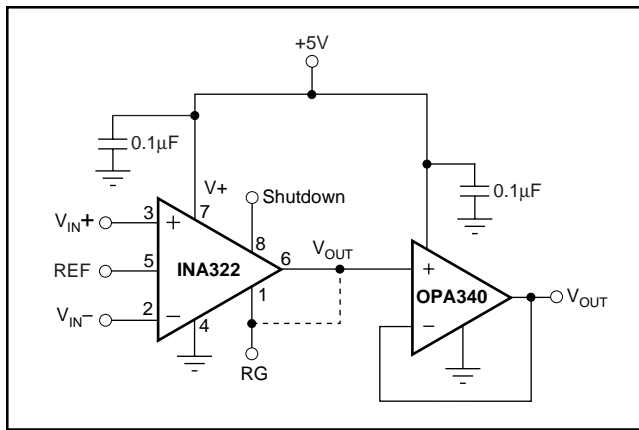


FIGURE 4. Output Buffering Circuit. Able to drive loads as low as 600Ω.

### SHUTDOWN MODE

The shutdown pin of the INA322 is nominally connected to V+. When the pin is pulled below 0.8V on a 5V supply, the INA322 goes into sleep mode within nanoseconds. For actual shutdown threshold, see typical characteristic curve “Shutdown Voltage vs Supply Voltage”. Drawing less than 1µA of current, and returning from sleep mode in microseconds, the shutdown feature is useful for portable applications. Once in ‘sleep-mode’ the amplifier has high output impedance, making the INA322 suitable for multiplexing.

### RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output for gains of 10 or greater. When the amplifier is in  $G = 5$  the output will not swing to positive rail. For resistive loads greater than 25kΩ, the output voltage can swing to within a few millivolts of the supply rail while maintaining low gain error. For heavier loads and over temperature, see the typical characteristic curve “Output Voltage Swing vs Output Current.” The INA322’s low output impedance at high frequencies makes it suitable for directly driving Capacitive Digital-to-Analog (CDAC) input A/D converters, as shown in Figure 5.

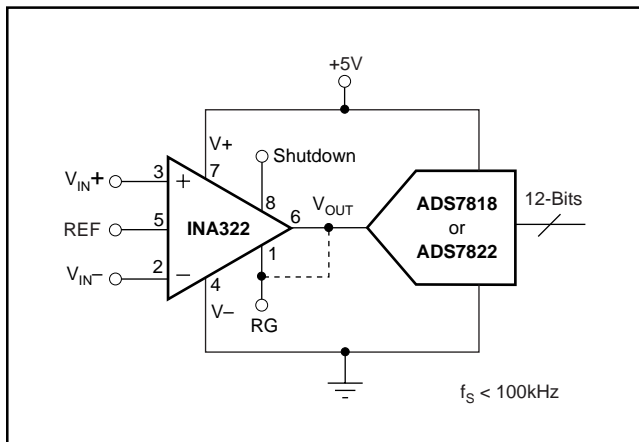


FIGURE 5. INA322 Directly Drives a Capacitive-Input, A/D Converter.

### OUTPUT BUFFERING

The INA322 is optimized for a load impedance of 10kΩ or greater. For higher output current the INA322 can be buffered using the OPA340, as shown in Figure 4. The OPA340 can swing within 50mV of the supply rail, driving a 600Ω load. The OPA340 is available in the tiny MSOP-8 package.

### OFFSET TRIMMING

In the event that external offset adjustment is required, the offset can be adjusted by applying a correction voltage to the reference terminal. Figure 6 shows an optional circuit for trimming offset voltage. The voltage applied to the REF terminal is added to the output signal. The gain from REF to V\_OUT is +1. An op-amp buffer is used to provide low impedance at the REF terminal to preserve good common-mode rejection.

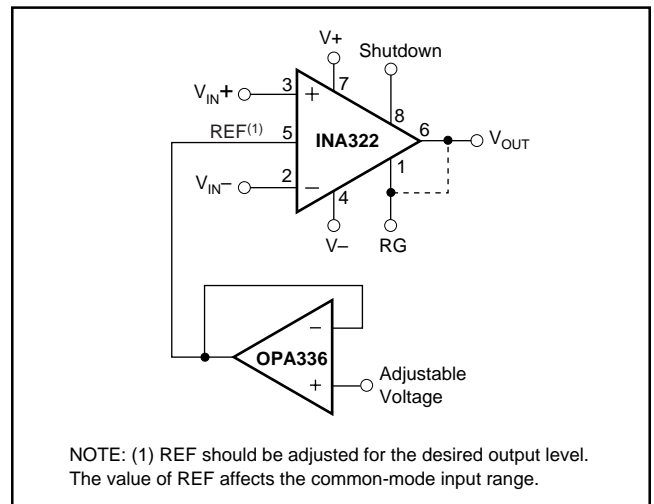


FIGURE 6. Optional Offset Trimming Voltage.

### INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current through the input pins is limited to 10mA. This is easily accomplished with input resistor  $R_{LIM}$ , as shown in Figure 7. Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.

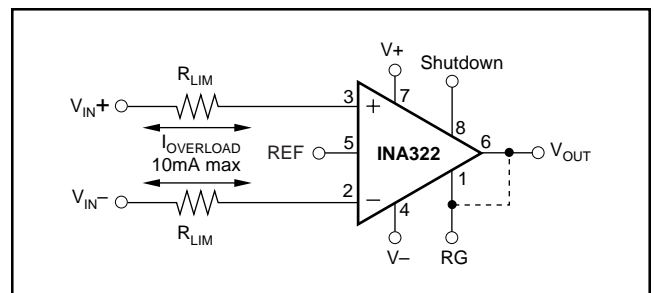


FIGURE 7. Input Protection.

## OFFSET VOLTAGE ERROR CALCULATION

The offset voltage ( $V_{OS}$ ) of the INA322EA has a specified maximum of 10mV with a +5V power supply and the common-mode voltage at  $V_S/2$ . Additional specifications for power-supply rejection and common-mode rejection are provided to allow the user to easily calculate worst-case expected offset under the conditions of a given application. Power Supply Rejection Ratio (PSRR) is specified in  $\mu\text{V}/\text{V}$ . For the INA322, worst case PSRR is  $250\mu\text{V}/\text{V}$ , which means for each volt of change in power supply, the offset may shift up to  $250\mu\text{V}$ . Common-Mode Rejection Ratio (CMRR) is specified in dB, which can be converted to  $\mu\text{V}/\text{V}$  using the following equation:

$$\text{CMRR (in } \mu\text{V}/\text{V)} = 10^{[(\text{CMRR in dB})/-20]} \cdot 10^6$$

For the INA322, the worst case CMRR over the specified common-mode range is 60dB (at  $G = 25$ ) or about  $1\text{mV}/\text{V}$ . This means that for every volt of change in common-mode, the offset will shift less than  $1\text{mV}$ .

These numbers can be used to calculate excursions from the specified offset voltage under different application conditions. For example, an application might configure the amplifier with a 3.3V supply with 1V common-mode. This configuration varies from the specified configuration, representing a 1.7V variation in power supply (5V in the offset specification versus 3.3V in the application) and a 0.65V variation in common-mode voltage from the specified  $V_S/2$ .

Calculation of the worst-case expected offset would be as follows:

$$\text{Adjusted } V_{OS} = \text{Maximum specified } V_{OS} + (\text{power-supply variation}) \cdot \text{PSRR} + (\text{common-mode variation}) \cdot \text{CMRR}$$

$$V_{OS} = 10\text{mV} + (1.7\text{V} \cdot 0.250\text{mV}/\text{V}) + (0.65\text{V} \cdot 1\text{mV}/\text{V}) \\ = \pm 11.075\text{mV}$$

However, the typical value will be closer to 2.2mV (calculated using the typical values).

## FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor,  $R_F$ , as shown in Figure 8. This capacitor compensates for the zero created by the feedback network impedance and the INA322's RG-pin input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks. Also,  $R_X$  and  $C_L$  can be added to reduce high-frequency noise.

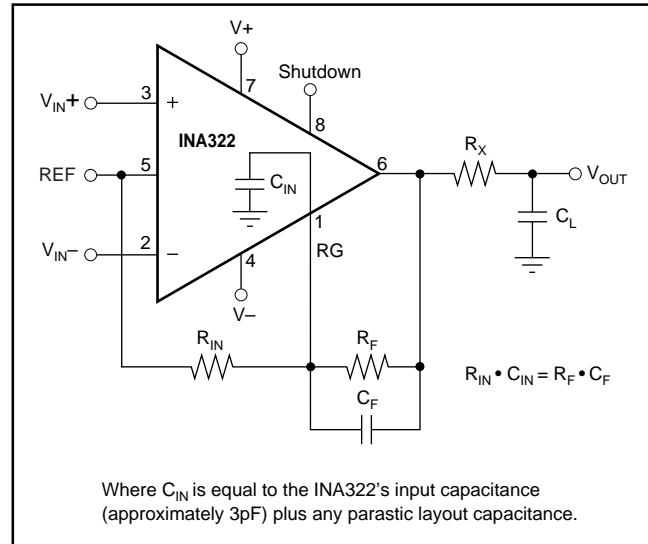


FIGURE 8. Feedback Capacitor Improves Dynamic Performance.

It is suggested that a variable capacitor be used for the feedback capacitor since input capacitance may vary between instrumentation amplifiers, and layout capacitance is difficult to determine. For the circuit shown in Figure 8, the value of the variable feedback capacitor should be chosen by the following equation:

$$R_{IN} \cdot C_{IN} = R_F \cdot C_F$$

Where  $C_{IN}$  is equal to the INA322's RG-pin input capacitance (typically 3pF) plus the layout capacitance. The capacitor can be varied until optimum performance is obtained.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA322EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI   NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	C22	<a href="#">Samples</a>
INA322EA/250G4	ACTIVE	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-55 to 125		<a href="#">Samples</a>
INA322EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI   NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	C22	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.





- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated