



12-BIT 250-KSPS SERIAL CMOS SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 250-kHz Sampling Rate
- 4-V, 5-V, 10-V, ± 3.33 -V, ± 5 -V, and ± 10 -V Input Ranges
- 73-dB SINAD With 45-kHz Input
- ± 0.45 LSB Max INL
- ± 0.45 LSB Max DNL, 12-Bits No Missing Codes
- ± 1 LSB Bipolar Zero Errors
- ± 0.4 PPM/ $^{\circ}$ C Bipolar Zero Error Drift
- Six Specified Input Ranges
- SPI Compatible Serial Output with Daisy-Chain (TAG) Feature
- 5-V Supply
- Pin-Compatible With ADS7808 (Low Speed) and 16-Bit ADS8509/7809
- Uses Internal or External Reference
- 70-mW Typ Power Dissipation at 250 KSPS
- 20-Pin SO Package
- Simple DSP Interface

APPLICATIONS

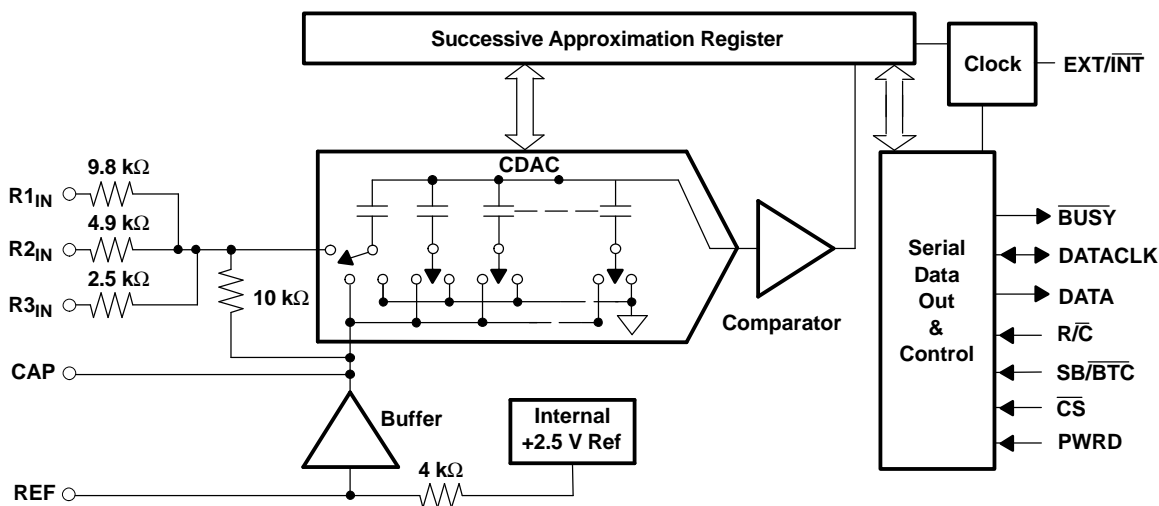
- Industrial Process Control
- Data Acquisition Systems
- Digital Signal Processing
- Medical Equipment
- Instrumentation

DESCRIPTION

The ADS8508 is a complete 12-bit sampling analog-to-digital (A/D) converter using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, successive approximation register (SAR) A/D converter with sample-and-hold, reference, clock, and a serial data interface. Data can be output using the internal clock or can be synchronized to an external data clock. The ADS8508 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS8508 is specified at a 250-kHz sampling rate over the full temperature range. Precision resistors provide various input ranges including ± 10 V and 0 V to 5 V, while the innovative design allows operation from a single +5-V supply with power dissipation under 100 mW.

The ADS8508 is available in a 20-pin SO package, fully specified for operation over the industrial -40° C to 85° C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	NO MISSING CODE	MINIMUM SINAD (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8508IB	±0.45	12	72	-40°C to 85°C	SO-20	DW	ADS8508IBDW	Tube, 25
							ADS8508IBDWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		ADS8508
Analog inputs	R1 _{IN}	±25 V
	R2 _{IN}	±25 V
	R3 _{IN}	±25 V
	CAP	+V _{ANA} + 0.3 V to AGND2 - 0.3 V
	REF	Indefinite short to AGND2, momentary short to V _{ANA}
Ground voltage differences	DGND, AGND2	±0.3 V
	V _{ANA}	6 V
	V _{DIG} to V _{ANA}	0.3 V
	V _{DIG}	6 V
Digital inputs		-0.3 V to +V _{DIG} + 0.3 V
Maximum junction temperature		165°C
Storage temperature range		-65°C to 150°C
Internal power dissipation		700 mW
Lead temperature (soldering, 10s)		260°C

(1) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At T_A = -40°C to 85°C, f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference and fixed resistors (See [Figure 28](#) and [Figure 29](#)) (unless otherwise specified)

PARAMETER	TEST CONDITIONS	ADS8508IB			UNIT
		MIN	TYP	MAX	
Resolution				12	Bits
ANALOG INPUT					
Voltage ranges ⁽¹⁾					
Impedance ⁽¹⁾					
Capacitance			50		pF
THROUGHPUT SPEED					
Conversion cycle	Acquire and convert			4	µs
Throughput rate		250			kHz
DC ACCURACY					
INL	Integral linearity error	-0.45		0.45	LSB ⁽²⁾
DNL	Differential linearity error	-0.45		0.45	LSB
	No missing codes	12			Bits
	Transition noise ⁽³⁾		0.1		LSB

(1) ±10 V, 0 V to 5 V, etc. (see [Table 3](#))

(2) LSB means least significant bit. For the ±10-V input range, one LSB is 4.88 mV.

(3) Typical rms noise at worst case transitions and temperatures.

ELECTRICAL CHARACTERISTICS (continued)

At $T_A = -40^{\circ}\text{C}$ to 85°C , $f_s = 250\text{ kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = 5\text{ V}$, using internal reference and fixed resistors (See [Figure 28](#) and [Figure 29](#)) (unless otherwise specified)

PARAMETER		TEST CONDITIONS	ADS8508IB			UNIT	
			MIN	TYP	MAX		
Full-scale error ⁽⁴⁾⁽⁵⁾	±10 V range	Int. Ref. with 0.1% external fixed resistors	-0.5		0.5	%FS	
	All other ranges		-0.5		0.5		
Full-scale error drift		Int. Ref.	±7			ppm/°C	
Full-scale error ⁽⁴⁾⁽⁵⁾	±10 V range	Ext. Ref. with 0.1% external fixed resistors	-0.5		0.5	%FS	
	All other ranges		-0.5		0.5		
Full-scale error drift		Ext. Ref.	±2			ppm/°C	
Bipolar zero error ⁽⁴⁾			-1		1	mV	
Bipolar zero error drift			±0.4			ppm/°C	
Unipolar zero error ⁽⁴⁾	10 V range		-5		5	mV	
	4 V and 5 V range		-3		3		
Unipolar zero error drift			±2			ppm/°C	
Recovery to rated accuracy after power down		1-µF Capacitor to CAP	1			ms	
Power supply sensitivity ($V_{\text{DIG}} = V_{\text{ANA}} = V_{\text{D}}$)		+4.75 V < V_{D} < +5.25 V	-0.5		0.5	LSB	
AC ACCURACY							
SFDR	Spurious-free dynamic range	$f_i = 45\text{ kHz}$	86	95		dB ⁽⁶⁾	
THD	Total harmonic distortion	$f_i = 45\text{ kHz}$		-95	-86	dB	
SINAD	Signal-to-(noise+distortion)	$f_i = 45\text{ kHz}$	72	73		dB	
		-60-dB Input		32		dB	
SNR	Signal-to-noise ratio	$f_i = 45\text{ kHz}$	72	73		dB	
Full-power bandwidth ⁽⁷⁾			500			kHz	
SAMPLING DYNAMICS							
Aperture delay			5			ns	
Transient response		FS Step				2	µs
Overvoltage recovery ⁽⁸⁾			150			ns	
REFERENCE							
Internal reference voltage		No load	2.48	2.5	2.52	V	
Internal reference source current (must use external buffer)			1			µA	
Internal reference drift			8			ppm/°C	
External reference voltage range for specified linearity			2.3	2.5	2.7	V	
External reference current drain		Ext. 2.5-V Ref.				100	µA
DIGITAL INPUTS							
Logic levels							
V_{IL}	Low-level input voltage		-0.3		0.8	V	
V_{IH}	High-level input voltage		2.0	$V_{\text{DIG}} + 0.3\text{ V}$		V	

- (4) As measured with circuit shown in [Figure 28](#) and [Figure 29](#). Adjustable to zero with external potentiometer. Factory calibrated with 0.1%, 0.25-W resistors.
- (5) For bipolar input ranges, full-scale error is the worst case of -full-scale or +full-scale uncalibrated deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.
- (6) All specifications in dB are referred to a full-scale ±10-V input.
- (7) Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB.
- (8) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

At $T_A = -40^{\circ}\text{C}$ to 85°C , $f_s = 250\text{ kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = 5\text{ V}$, using internal reference and fixed resistors (See Figure 28 and Figure 29) (unless otherwise specified)

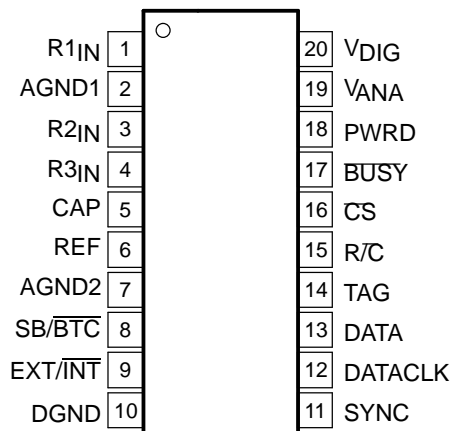
PARAMETER	TEST CONDITIONS	ADS8508IB			UNIT		
		MIN	TYP	MAX			
I_{IL}	Low-level input current	$V_{\text{IL}} = 0\text{ V}$			± 10	μA	
I_{IH}	High-level input current	$V_{\text{IH}} = 5\text{ V}$			± 10	μA	
DIGITAL OUTPUTS							
	Data format (Serial 16-bits)						
	Data coding (Binary 2's complement or straight binary)						
	Pipeline delay (Conversion results only available after completed conversion.)						
	Data clock (Selectable for internal or external data clock)						
	Internal clock (output only when transmitting data)	EXT/ $\overline{\text{INT}}$ Low			9	MHz	
	External clock (can run continually but not recommended for optimum performance)	EXT/ $\overline{\text{INT}}$ High			0.1	26	MHz
V_{OL}	Low-level output voltage	$I_{\text{SINK}} = 1.6\text{ mA}$			0.4	V	
V_{OH}	High-level output voltage	$I_{\text{SOURCE}} = 500\ \mu\text{A}$			4	V	
	Leakage current	Hi-Z state, $V_{\text{OUT}} = 0\text{ V}$ to V_{DIG}			± 5	μA	
	Output capacitance	Hi-Z state			15	pF	
POWER SUPPLIES							
V_{DIG}	Digital input voltage	Must be $\leq V_{\text{ANA}}$	4.75	5	5.25	V	
V_{ANA}	Analog input voltage		4.75	5	5.25	V	
I_{DIG}	Digital input current		4			mA	
I_{ANA}	Analog input current		10			mA	
POWER DISSIPATION							
	PWRD Low	$f_s = 250\text{ kHz}$			70	100	mW
	PWRD High				50		μW
TEMPERATURE RANGE							
	Specified performance				-40	85	$^{\circ}\text{C}$
	Derated performance ⁽⁹⁾				-55	125	$^{\circ}\text{C}$
	Storage				-65	150	$^{\circ}\text{C}$
THERMAL RESISTANCE (Θ_{JA})							
	SO				75		$^{\circ}\text{C}/\text{W}$

(9) The internal reference may not be started correctly beyond the industrial temperature range (-40°C to 85°C), therefore use of an external reference is recommended.

TIMING REQUIREMENTS, $T_A = -40^{\circ}\text{C}$ to 85°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{w1}	Pulse duration, convert	40			ns
t_{d1}	Delay time, $\overline{\text{BUSY}}$ from $\text{R}/\overline{\text{C}}$ low		6	20	ns
t_{w2}	Pulse duration, $\overline{\text{BUSY}}$ low			2.2	μs
t_{d2}	Delay time, $\overline{\text{BUSY}}$, after end of conversion		5		ns
t_{d3}	Delay time, aperture		5		ns
t_{conv}	Conversion time			2.2	μs
t_{acq}	Acquisition time	1.8			μs
$t_{\text{conv}} + t_{\text{acq}}$	Cycle time			4	μs
t_{d4}	Delay time, $\text{R}/\overline{\text{C}}$ Low to internal DATACLK output		270		ns
t_{c1}	Cycle time, internal DATACLK		110		ns
t_{d5}	Delay time, data valid to internal DATACLK high	15	35		ns
t_{d6}	Delay time, data valid after internal DATACLK low	20	35		ns
t_{c2}	Cycle time, external DATACLK	35			ns
t_{w3}	Pulse duration, external DATACLK high	15			ns
t_{w4}	Pulse duration, external DATACLK low	15			ns
$t_{\text{su}1}$	Setup time, $\text{R}/\overline{\text{C}}$ rise/fall to external DATACLK high	15	$t_{c2} + 5$		ns
$t_{\text{su}2}$	Setup time, $\text{R}/\overline{\text{C}}$ transition to $\overline{\text{CS}}$ transition	10			ns
t_{d7}	Delay time, SYNC, after external DATACLK high	3		35	ns
t_{d8}	Delay time, data valid	2		20	ns
t_{d9}	Delay time, $\overline{\text{CS}}$ to rising edge	10			ns
t_{d10}	Delay time, previous data available after $\overline{\text{CS}}$, $\text{R}/\overline{\text{C}}$ low	2			μs
$t_{\text{su}3}$	Setup time, $\overline{\text{BUSY}}$ transition to first external DATACLK	5			ns
t_{d11}	Delay time, final external DATACLK to $\overline{\text{BUSY}}$ falling edge			1	μs
$t_{\text{su}3}$	Setup time, TAG valid	0			ns
t_{h1}	Hold time, TAG valid	2			ns

**DW PACKAGE
(TOP VIEW)**



Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
AGND1	2	–	Analog ground. Used internally as ground reference point. Minimal current flow.
AGND2	7	–	Analog ground
BUSY	17	O	Busy output. Falls when a conversion is started, and remains low until the conversion is completed and the data is latched into the output shift register.
CAP	5	–	Reference buffer capacitor. 2.2- μ F Tantalum to ground.
\overline{CS}	16	–	Chip select. Internally ORed with R/\overline{C}
DATA	13	O	Serial data output. Data is synchronized to DATACLK, with the format determined by the level of SB/ \overline{BTC} . In the external clock mode, after 16 bits of data, the ADS8508 outputs the level input on TAG as long as \overline{CS} is low and R/\overline{C} is high (see Figure 8 and Figure 9). If EXT/ \overline{INT} is low, data is valid on both the rising and falling edges of DATACLK, and between conversions DATA stays at the level of the TAG input when the conversion was started.
DATACLK	12	I/O	Either an input or an output depending on the EXT/ \overline{INT} level. Output data is synchronized to this clock. If EXT/ \overline{INT} is low, DATACLK transmits 16 pulses after each conversion, and then remains low between conversions.
DGND	10	–	Digital ground
EXT/ \overline{INT}	9	–	Selects external or internal clock for transmitting data. If high, data is output synchronized to the clock input on DATACLK. If low, a convert command initiates the transmission of the data from the previous conversion, along with 16-clock pulses output on DATACLK.
NC	–	–	No connect
PWRD	18	I	Power down input. If high, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
R/\overline{C}	15	I	Read/convert input. With \overline{CS} low, a falling edge on R/\overline{C} puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/ \overline{INT} is low, this also initiates the transmission of the data results from the previous conversion. If EXT/ \overline{INT} is high, a rising edge on R/\overline{C} with \overline{CS} low, or a falling edge on \overline{CS} with R/\overline{C} high, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
REF	6	I/O	Reference input/output. Outputs internal 2.5-V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2- μ F tantalum capacitor.
R1 _{IN}	1	I	Analog input. See Table 3 for input range connections.
R2 _{IN}	3	I	Analog input. See Table 3 for input range connections.
R3 _{IN}	4	I	Analog input. See Table 3 for input range connections.
SB/ \overline{BTC}	8	O	Select straight binary or binary 2's complement data output format. If high, data is output in a straight binary format. If low, data is output in a binary 2's complement format.
SYNC	11	O	Sync output. This pin is used to supply a data synchronization pulse when the EXT level is high and at least one external clock pulse has occurred when not in the read mode. See the external clock modes descriptions.
TAG	14	I	Tag input for use in the external clock mode. If EXT is high, digital data input from TAG is output on DATA with a delay that is dependent on the external clock mode. See Figure 8 and Figure 9 .
V _{ANA}	19	I	Analog supply input. Nominally +5 V. Connect directly to pin 20, and decouple to ground with 0.1- μ F ceramic and 10- μ F tantalum capacitors.
V _{DIG}	20	I	Digital supply input. Nominally +5 V. Connect directly to pin 19. Must be $\leq V_{ANA}$.

PARAMETER MEASUREMENT INFORMATION

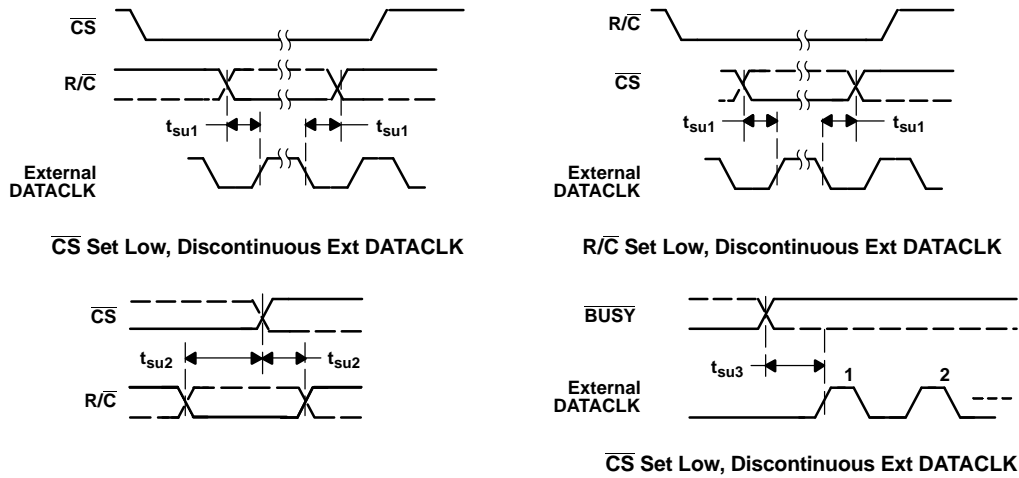


Figure 1. Critical Timing

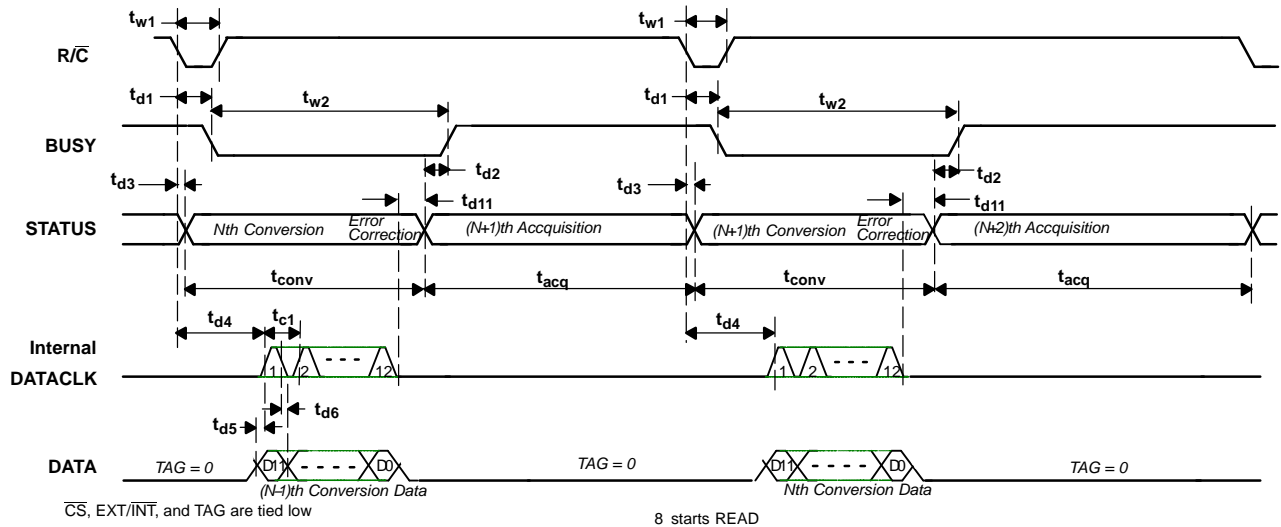


Figure 2. Basic Conversion Timing - Internal DATACLK (Read Previous Data During Conversion)

PARAMETER MEASUREMENT INFORMATION (continued)

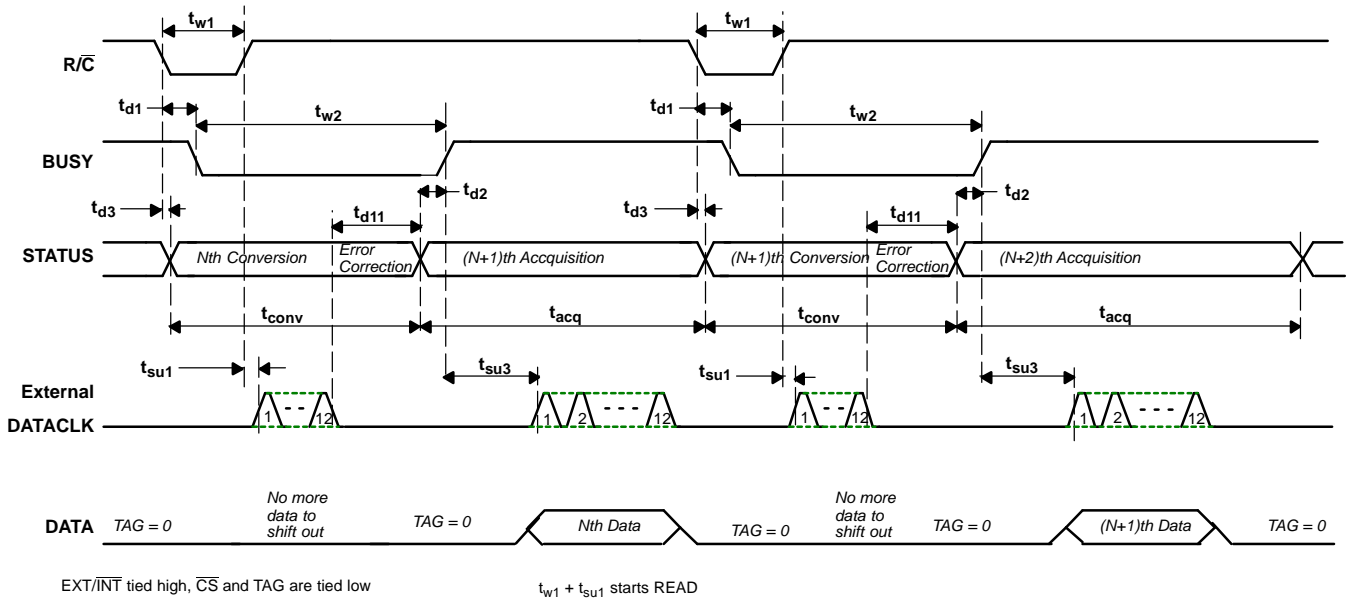


Figure 3. Basic Conversion Timing - External DATACLK

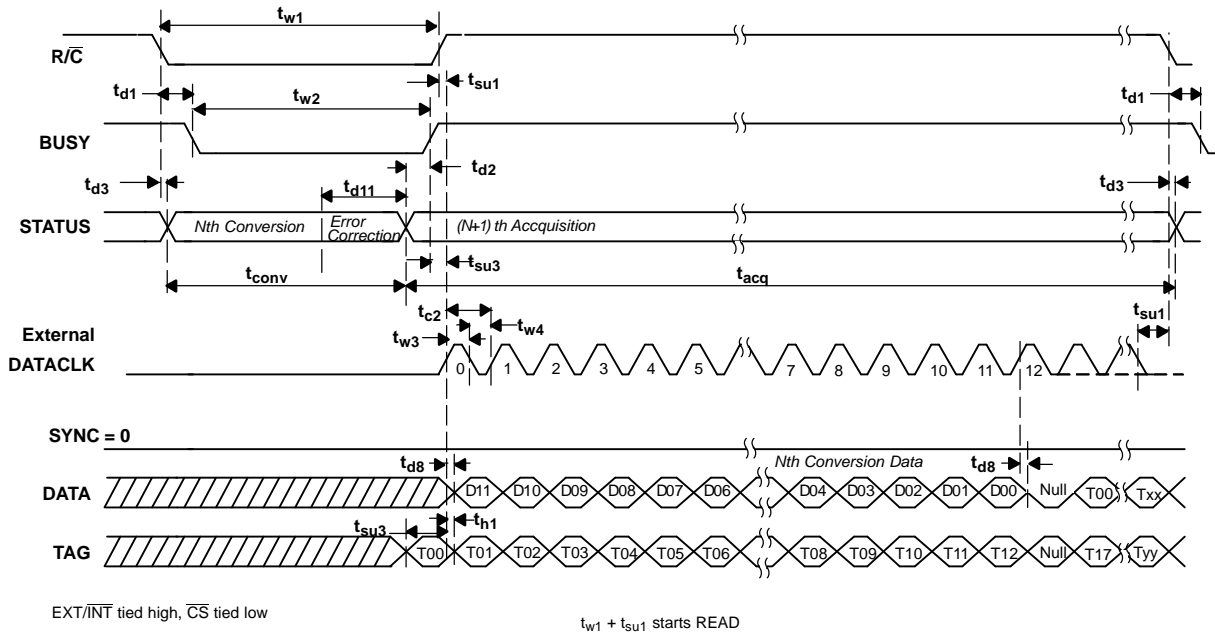


Figure 4. Read After Conversion (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

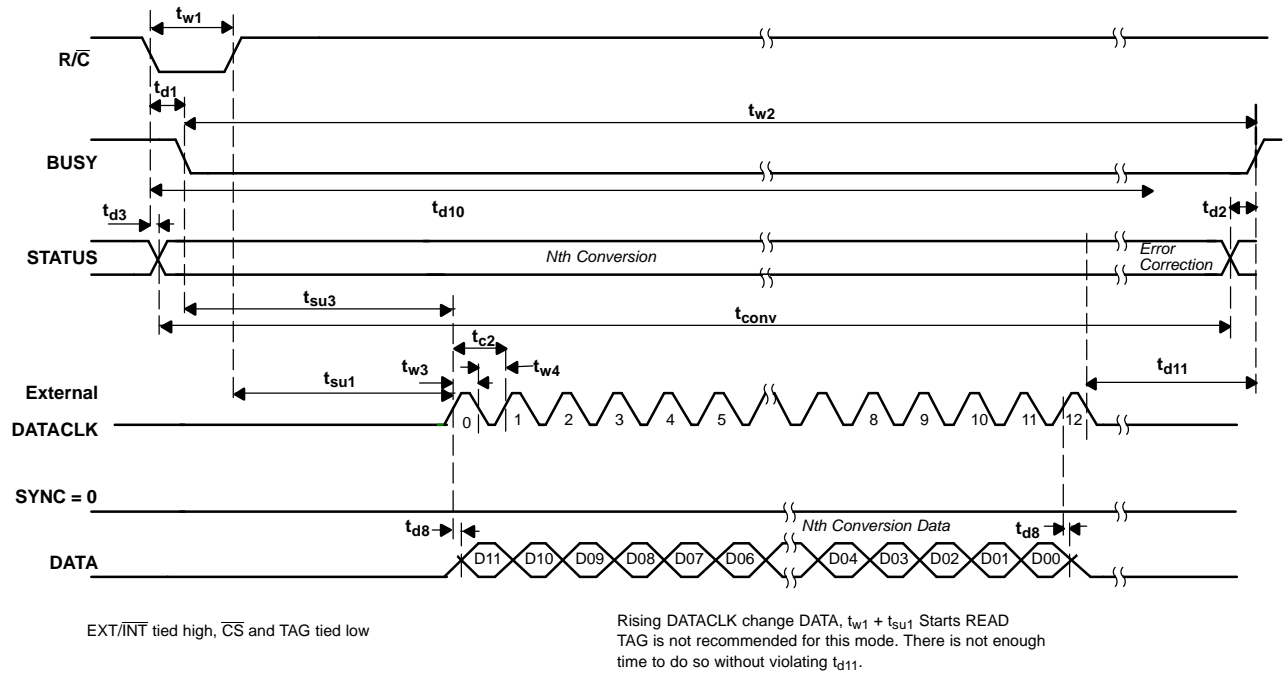


Figure 5. Read During Conversion (Discontinuous External DATACLK)

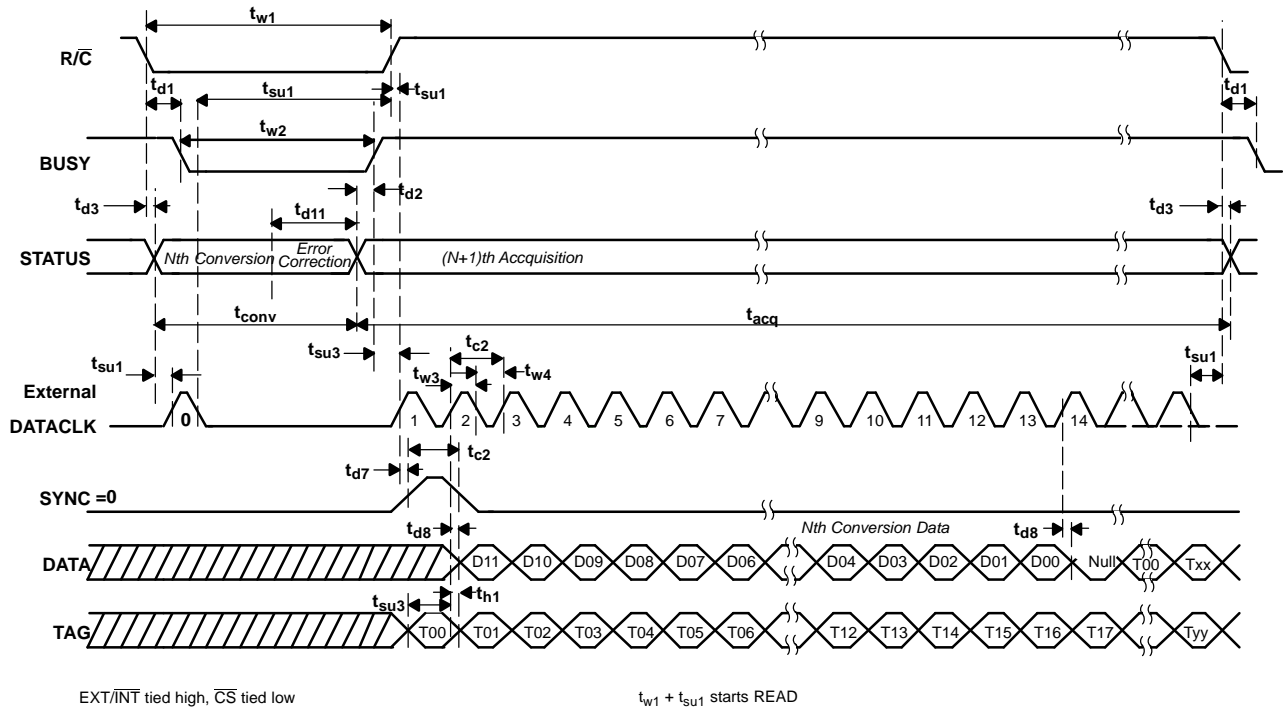


Figure 6. Read After Conversion With SYNC (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

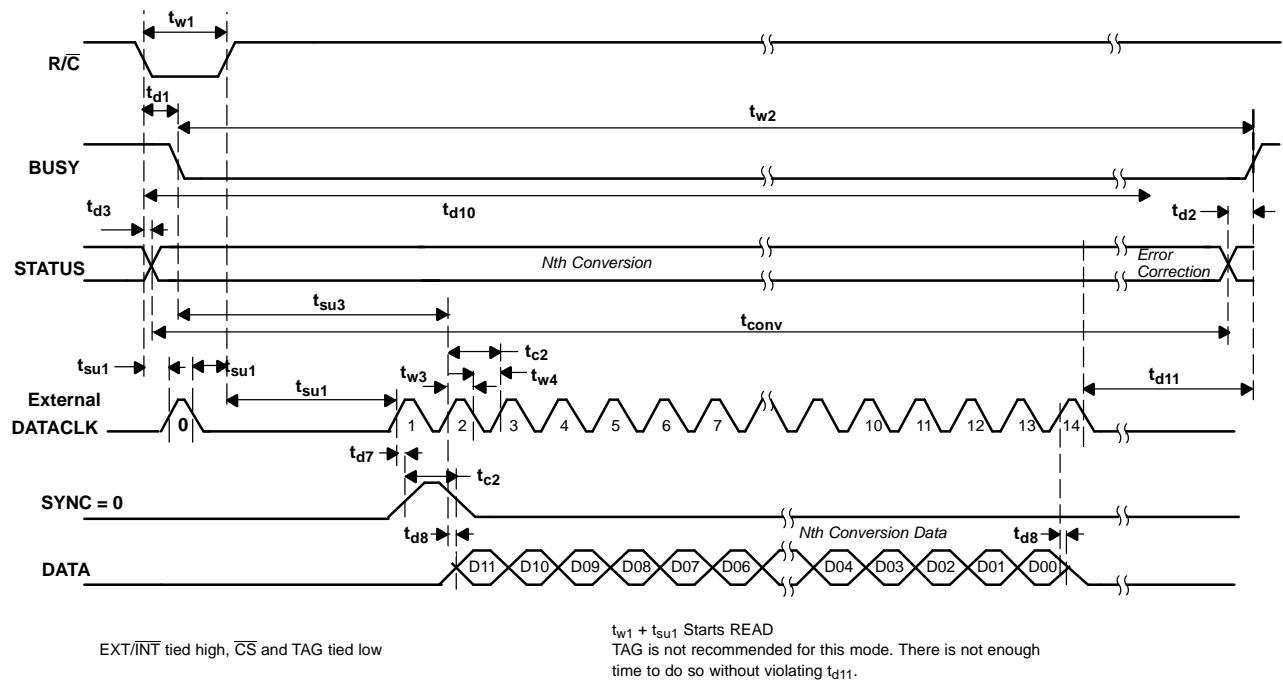


Figure 7. Read During Conversion With SYNC (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

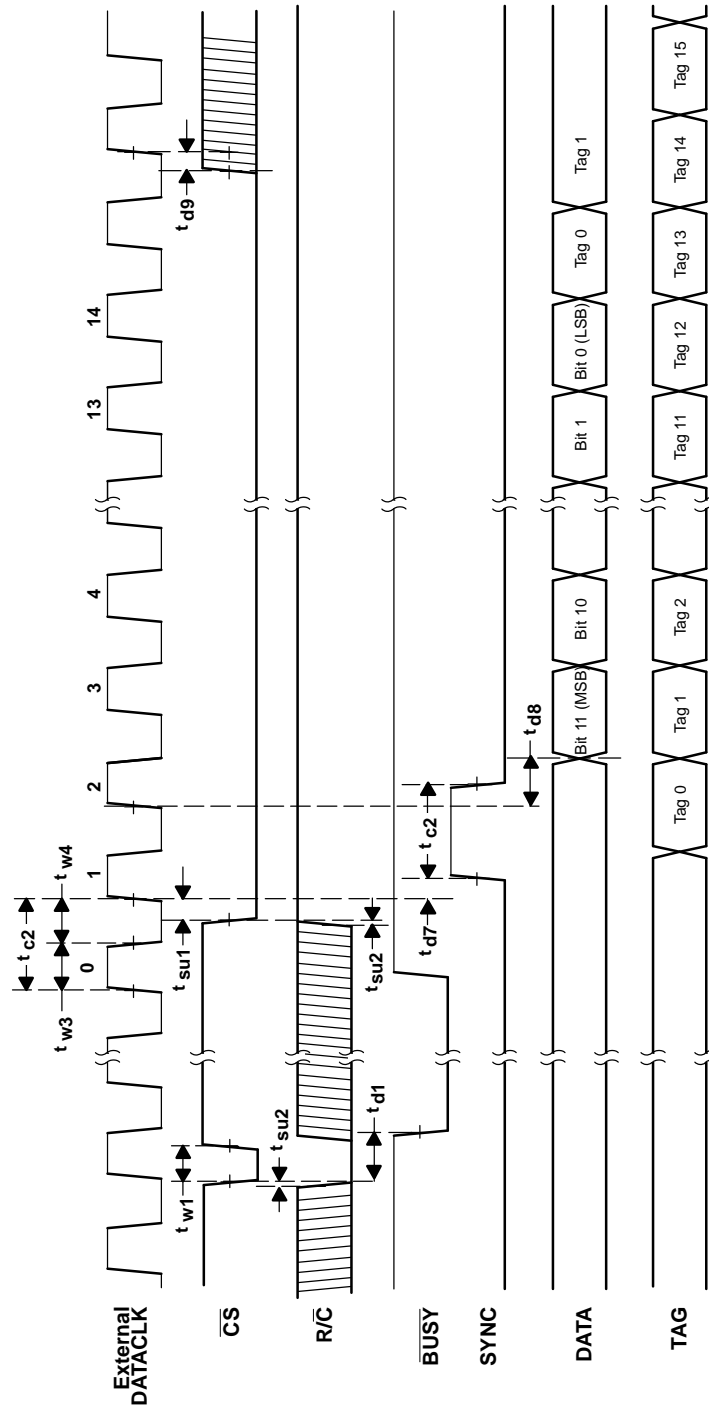


Figure 8. Conversion and Read Timing with Continuous External DATACLK (EXT/INT Tied High) Read After Conversions (Not Recommended)

PARAMETER MEASUREMENT INFORMATION (continued)

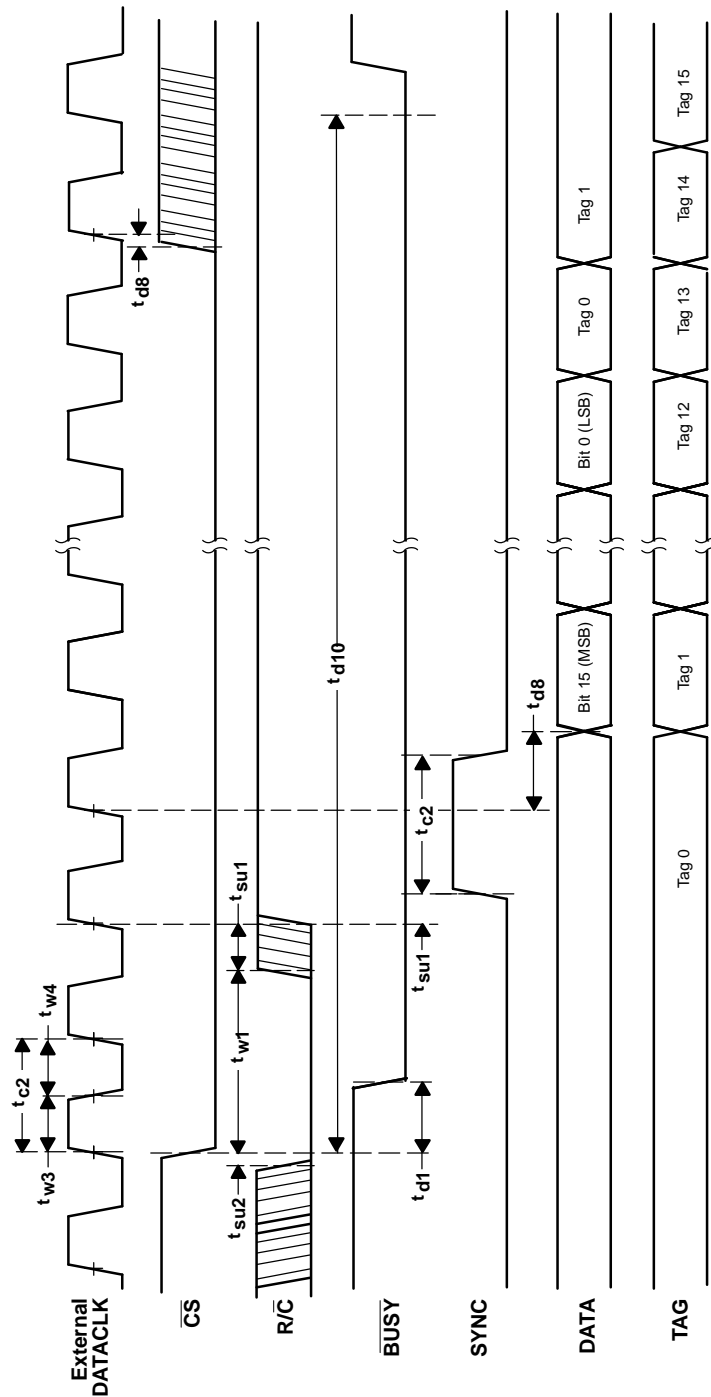


Figure 9. Conversion and Read Timing with Continuous External DATACLK (EXT/INT Tied High) Read Previous Conversion Result During Conversion (Not Recommended)

TYPICAL CHARACTERISTICS

**SPURIOUS FREE DYNAMIC RANGE
VS
FREE-AIR TEMPERATURE**

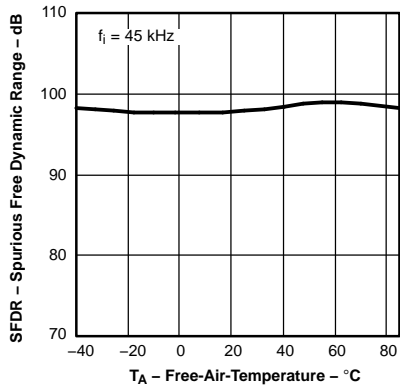


Figure 10.

**TOTAL HARMONIC DISTORTION
VS
FREE-AIR TEMPERATURE**

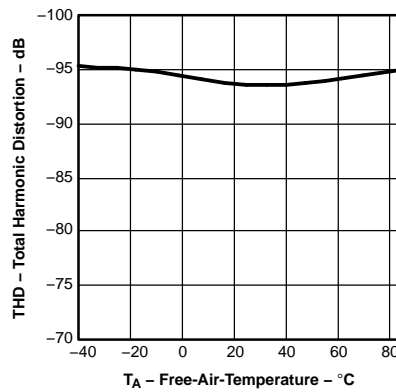


Figure 11.

**SIGNAL-TO-NOISE RATIO
VS
FREE-AIR TEMPERATURE**

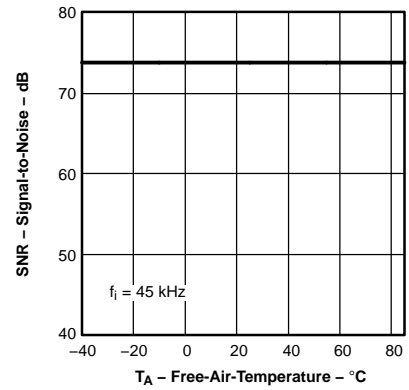


Figure 12.

**SIGNAL-TO-NOISE AND DISTOR-
TION
VS
FREE-AIR TEMPERATURE**

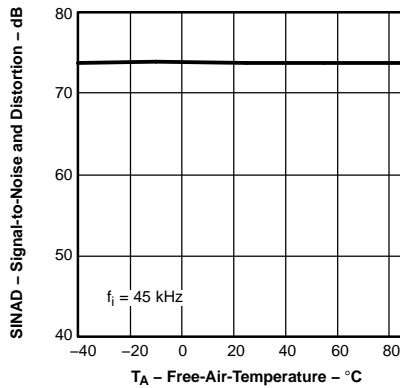


Figure 13.

**SIGNAL-TO-NOISE RATIO
VS
INPUT FREQUENCY**

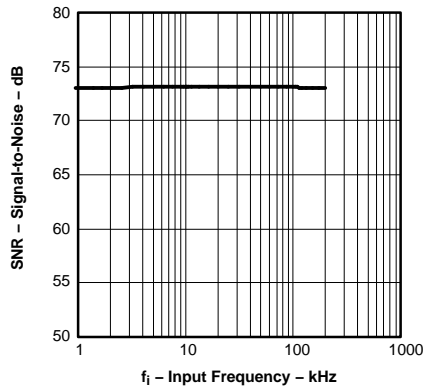


Figure 14.

**SIGNAL-TO-NOISE AND DISTOR-
TION
VS
INPUT FREQUENCY**

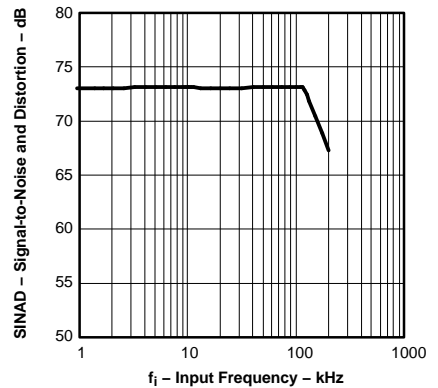


Figure 15.

**SPURIOUS FREE DYNAMIC RANGE
VS
INPUT FREQUENCY**

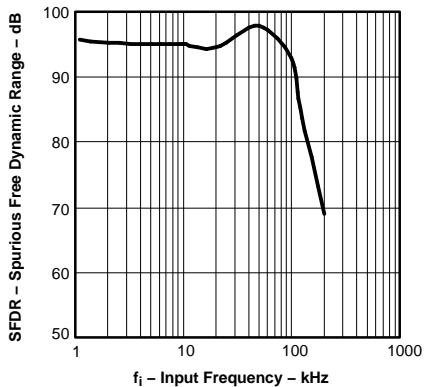


Figure 16.

**TOTAL HARMONIC DISTORTION
VS
INPUT FREQUENCY**

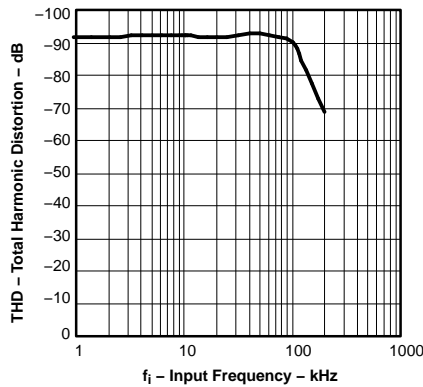


Figure 17.

**BIPOLAR ZERO SCALE ERROR
VS
FREE-AIR TEMPERATURE**

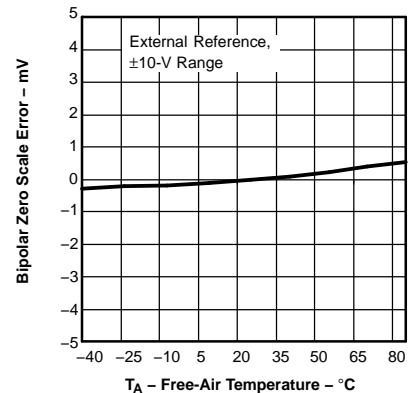


Figure 18.

TYPICAL CHARACTERISTICS (continued)

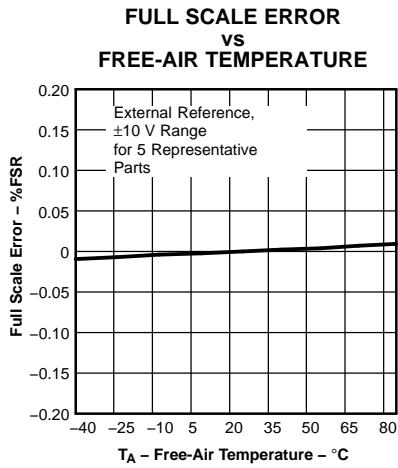


Figure 19.

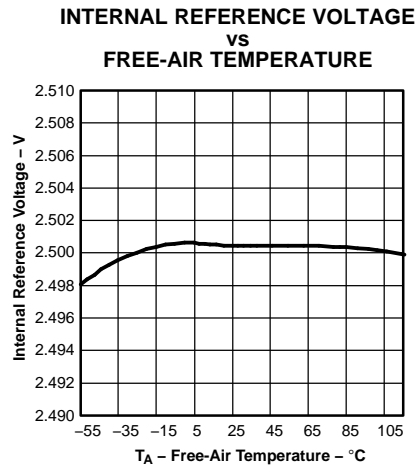


Figure 20.

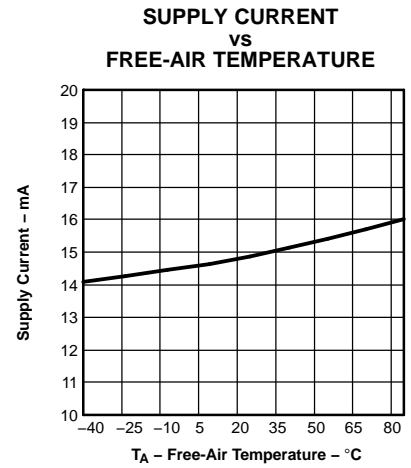


Figure 21.

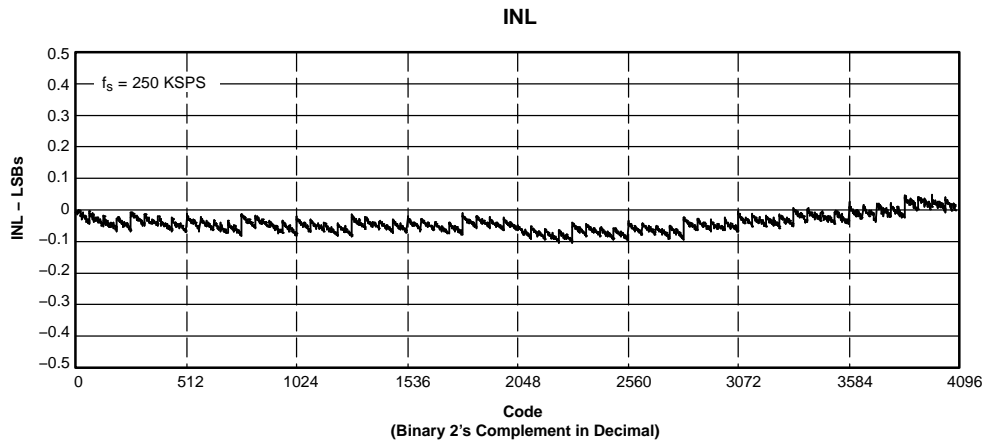


Figure 22.

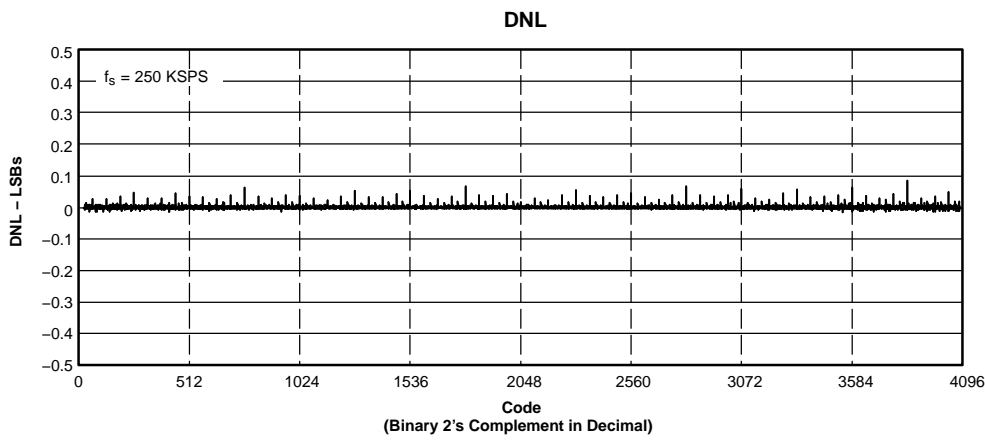


Figure 23.

TYPICAL CHARACTERISTICS (continued)

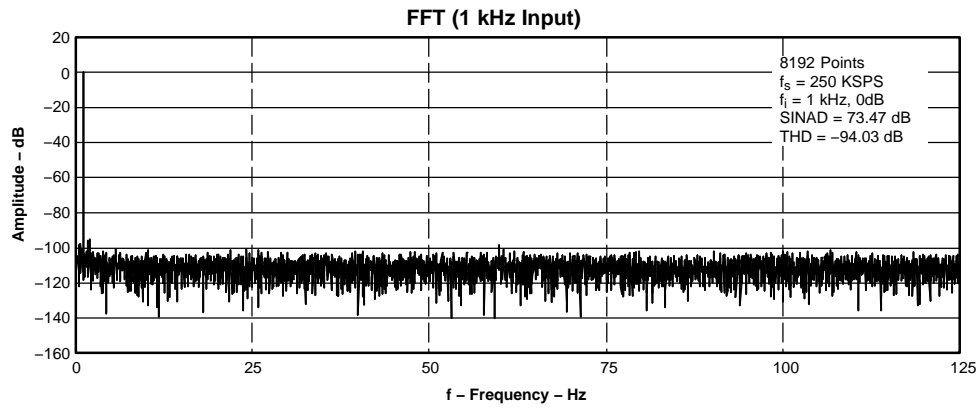


Figure 24.

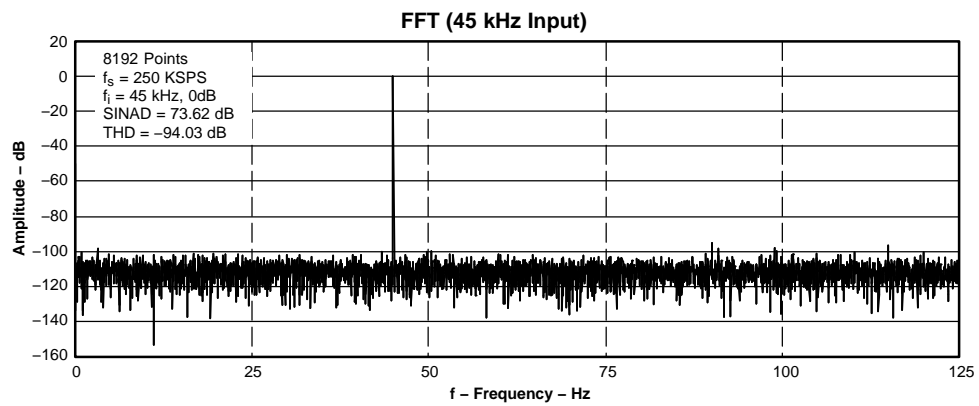


Figure 25.

BASIC OPERATION

Two signals control conversion in the ADS8508: \overline{CS} and R/\overline{C} . These two signals are internally ORed together. To start a conversion the chip must be selected, \overline{CS} low, and the conversion signal must be active, R/\overline{C} low. Either signal can be brought low first. Conversion starts on the falling edge of the second signal. \overline{BUSY} goes low when conversion starts and returns high after the data from that conversion is shifted into the internal storage register. Sampling begins when \overline{BUSY} goes high.

To reduce the number of control pins \overline{CS} can be tied low permanently. The R/\overline{C} pin now controls conversion and data reading exclusively. In the external clock mode this means that the ADS8508 will clock out data whenever R/\overline{C} is brought high and the external clock is active. In the internal clock mode data is clocked out every convert cycle regardless of the states of \overline{CS} and R/\overline{C} . The ADS8508 provides a TAG input for cascading multiple converters together.

READING DATA

The conversion result is available as soon as \overline{BUSY} returns to high therefore, data always represents the conversion previously completed even when it is read during a conversion. The ADS8508 outputs serial data in either straight binary or binary two's complement format. The SB/\overline{BTC} pin controls the format. Data is shifted out MSB first. The first conversion immediately following a power-up will not produce a valid conversion result.

Data can be clocked out with either the internally generated clock or with an external clock. The EXT/\overline{INT} pin controls this function. If external clock is used the TAG input can be used to daisy-chain multiple ADS8508 data pins together.

INTERNAL DATACLK

In the internal clock mode data for the previous conversion is clocked out during each conversion period. The internal data clock is synchronized to the internal conversion clock so that it does not interfere with the conversion process.

The DATACLK pin becomes an output when EXT/\overline{INT} is low. 12 clock pulses are generated at the beginning of each conversion after timing t_b is satisfied, i.e. you can only read previous conversion result during conversion. DATACLK returns to low when it is inactive. The 12 bits of serial data are shifted out the DATA pin synchronous to this clock with each bit available on a rising and then a falling edge. DATA pin returns to the state of TAG pin input sensed at the start of transmission.

EXTERNAL DATACLK

The external clock mode offers several ways to retrieve conversion results. However, since the external clock cannot be synchronized to the internal conversion clock care must be taken to avoid corrupting the data.

When EXT/\overline{INT} is set high, the R/\overline{C} and \overline{CS} signals control the read state. When the read state is initiated the result from the previously completed conversion is shifted out the DATA pin synchronous to the external clock that is connected to the DATACLK pin. Each bit is available on a falling and then a rising edge. The maximum external clock speed of 28.5 MHz allows data shifted out quickly either at the beginning of conversion or the beginning of sampling.

There are several modes of operation available when using an external clock. It is recommended that the external clock run only while reading data. This is the discontinuous clock mode. Since the external clock is not synchronized to the internal clock that controls conversion slight changes in the external clock can cause conflicts that can corrupt the conversion process. Specifications with a continuously running external clock cannot be guaranteed. It is especially important that the external clock does not run during the second half of the conversion cycle (approximately the time period specified by t_{d11} , see timing table).

In the discontinuous clock mode data can be read during conversion or during sampling, with or without a SYNC pulse. Data read during a conversion must meet the t_{d11} timing specification. Data read during sampling must be complete before starting a conversion.

Whether reading during sampling or during conversion a SYNC pulse is generated whenever at least one rising edge of the external clock occurs while the part is not in the read state. In the *discontinuous external clock with SYNC* mode a SYNC pulse follows the first rising edge after the read command. The data is shifted out after the SYNC pulse. The first rising clock edge after the read command generates a SYNC pulse. The SYNC pulse can be detected on the next falling edge and then the next rising edge. Successively, each bit can be read first on the falling edge and then on the next rising edge. Thus 13 clock pulses after the read command are required to read on the falling edge, and 14 clock pulses are necessary to read on the rising edge.

Table 2. DATACLK Pulses

DESCRIPTION	DATACLK PULSES REQUIRED	
	WITH SYNC	WITHOUT SYNC
Read on falling edge of DATACLK	13	12
Read on rising edge of DATACLK	14	13

If the clock is entirely inactive when not in the read state no SYNC pulse is generated. In this case the first rising clock edge shifts out the MSB. The MSB can be read on the first falling edge or on the next rising edge. In this *discontinuous external clock mode with no SYNC*, 12 clocks are necessary to read the data on the falling edge and 13 clocks for reading on the rising edge. Data always represents the conversion already completed.

TAG FEATURE

The TAG feature allows the data from multiple ADS8508 converters to be read on a single serial line. The converters are cascaded together using the DATA pins as outputs and the TAG pins as inputs as illustrated in [Figure 26](#). The DATA pin of the last converter drives the processor's serial data input. Data is then shifted through each converter, synchronous to the externally supplied data clock, onto the serial data line. The internal clock cannot be used for this configuration.

The preferred timing uses the discontinuous, external, data clock during the sampling period. Data must be read during the sampling period because there is not sufficient time to read data from multiple converters during a conversion period without violating the t_{d11} constraint (see the EXTERNAL DATACLOCK section). The sampling period must be sufficiently long to allow all data words to be read before starting a new conversion.

Note, in [Figure 26](#), that a NULL bit separates the data word from each converter. The state of the DATA pin at the end of a READ cycle reflects the state of the TAG pin at the start of the cycle. This is true in all READ modes, including the internal clock mode. For example, when a single converter is used in the internal clock mode the state of the TAG pin determines the state of the DATA pin after all 12 bits have shifted out. When multiple converters are cascaded together this state forms the NULL bit that separates the words. Thus, with the TAG pin of the first converter grounded as shown in [Figure 26](#) the NULL bit becomes a zero between each data word.

The external reference voltage can vary from 2.3 V to 2.7 V. The reference voltage determines the size of the least significant bit (LSB). The larger reference voltages produce a larger LSB, which can improve SNR. Smaller reference voltages can degrade SNR.

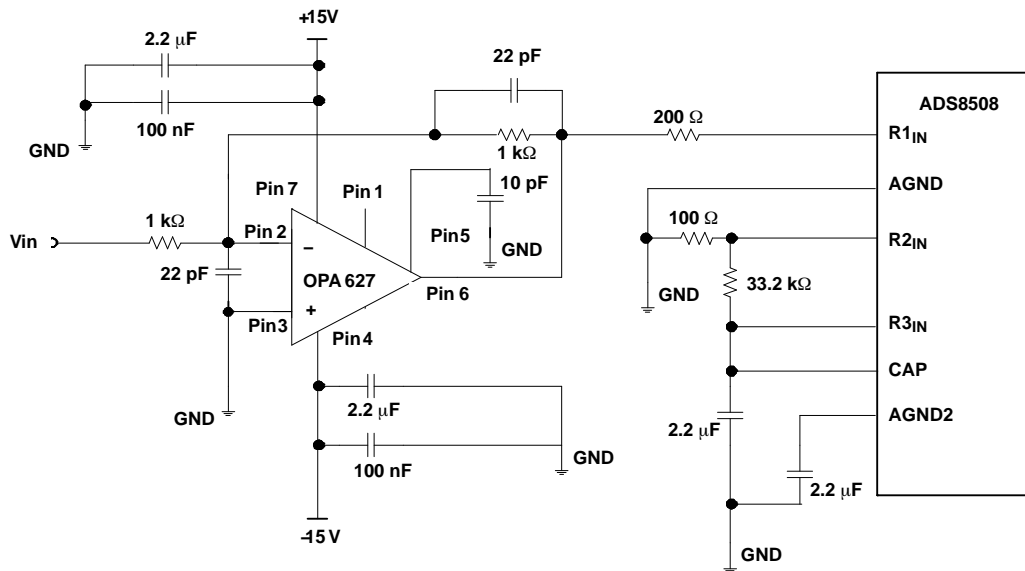


Figure 27. Typical Driving Circuitry (± 10 V, No Trim)

Table 3. Input Range Connections (see Figure 28 and Figure 29 for complete information)

ANALOG INPUT RANGE	CONNECT R1 _{IN} VIA 200 Ω TO	CONNECT R2 _{IN} VIA 100 Ω TO	CONNECT R3 TO	IMPEDANCE
± 10 V	V _{IN}	AGND	CAP	11.5 kΩ
± 5 V	AGND	V _{IN}	CAP	6.7 kΩ
± 3.33 V	V _{IN}	V _{IN}	CAP	5.4 kΩ
0 V to 10 V	AGND	V _{IN}	AGND	6.7 kΩ
0 V to 5 V	AGND	AGND	V _{IN}	5.0 kΩ
0 V to 4 V	V _{IN}	AGND	V _{IN}	5.4 kΩ

Table 4. Control Truth Table

SPECIFIC FUNCTION	\overline{CS}	R/ \overline{C}	BUSY	EXT/ \overline{INT}	DATACLK	PWRD	SB/ \overline{BTC}	OPERATION
Initiate conversion and output data using internal clock	1 > 0	0	1	0	Output	0	x	Initiates conversion <i>n</i> . Data from conversion <i>n</i> - 1 clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
	0	1 > 0	1	0	Output	0	x	
Initiate conversion and output data using external clock	1 > 0	0	1	1	Input	0	x	Initiates conversion <i>n</i> .
	0	1 > 0	1	1	Input	0	x	Initiates conversion <i>n</i> .
	1 > 0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion <i>n</i> clocked out synchronized to external DATACLK.
	1 > 0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion <i>n</i> - 1 clocked out synchronized to external DATACLK. ⁽¹⁾ Conversion <i>n</i> in process.
0	0 > 1	0	1	Input	0	x		
Incorrect conversions	0	0	0 > 1	x	x	0	x	\overline{CS} or R/ \overline{C} must be HIGH or a new conversion will be initiated without time for acquisition.
Power down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed..
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.

(1) See Figure XXX for the constraints on previous data valid during a conversion.

Table 4. Control Truth Table (continued)

Selecting output format	x	x	x	x	x	x	0	Serial data is output in binary 2s complement format.
	x	x	x	x	x	x	1	Serial data is output in straight binary format.

Table 5. Output Codes and Ideal Input Voltages

DESCRIP- TION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY 2's COMPLEMENTS (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-scale range	±10	±5	±3.33 V	0 V to 5 V	0 V to 10 V	0 V to 4 V				
Least signifi- cant bit (LSB)	4.88 mV	2.44 mV	1.63 mV	1.22 mV	2.44 mV	0.98 mV				
Full scale (FS - 1LSB)	9.99512 V	4.997567 V	3.33171 V	4.99878 V	9.99756 V	3.99902 V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0 V	0 V	0 V	2.5 V	5 V	2 V	0000 0000 0000	000	1000 0000 0000	800
One LSB below midscale	-4.88 mV	-2.44 mV	-1.63 mV	2.49878 V	4.99756 V	1.99902 V	1111 1111 1111	FFF	0111 1111 1111	7FF
-Full scale	-10 V	-5 V	-3.333333 V	0 V	0 V	0 V	1000 0000 0000	800	0000 0000 0000	000

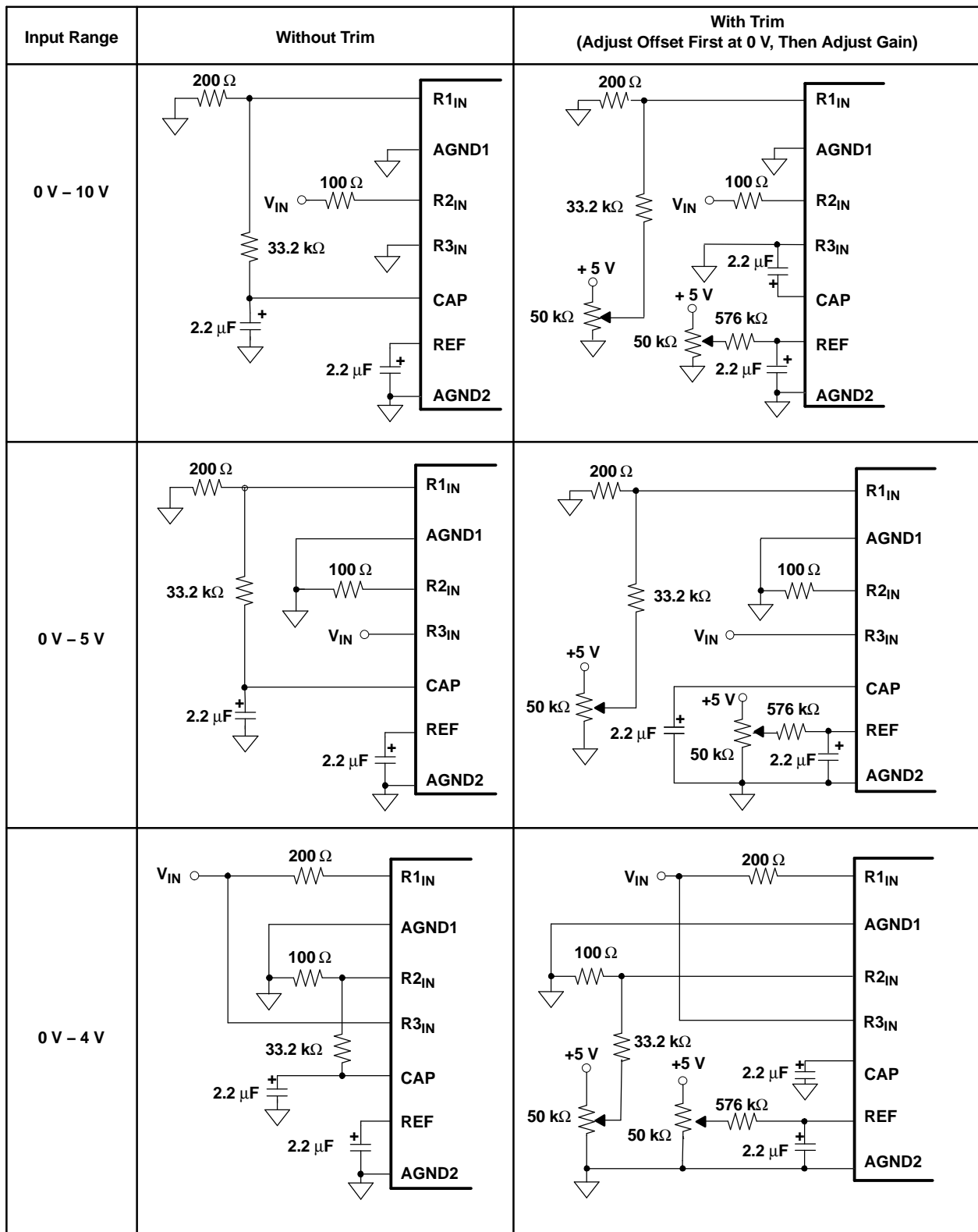


Figure 28. Offset/Gain Circuits for Unipolar Input Ranges

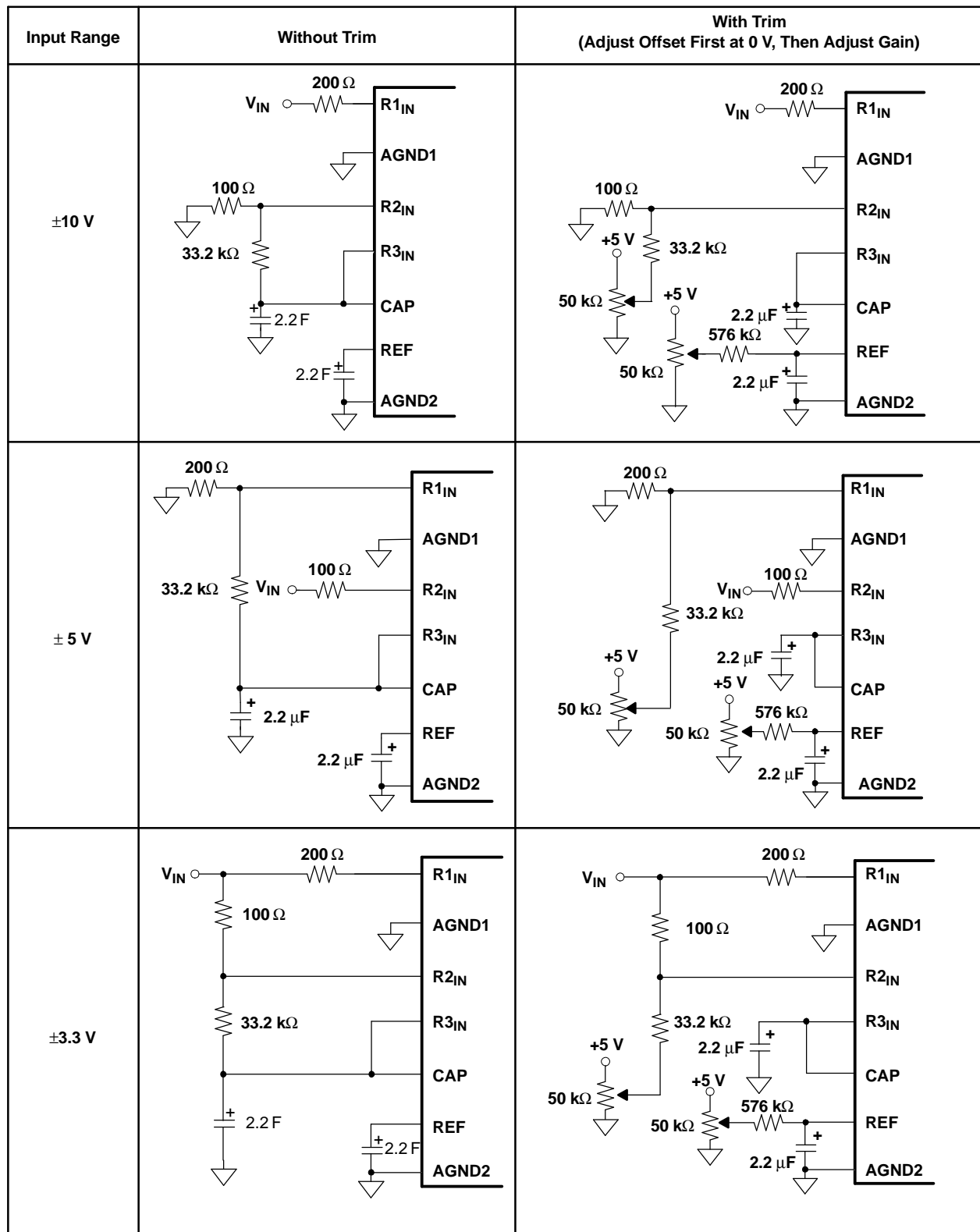


Figure 29. Offset/Gain Circuits for Bipolar Input Ranges

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8508IBDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8508IB	Samples
ADS8508IBDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8508IB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8508IBDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8508IBDWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ADS8508IBDW	DW	SOIC	20	25	506.98	12.7	4826	6.6

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

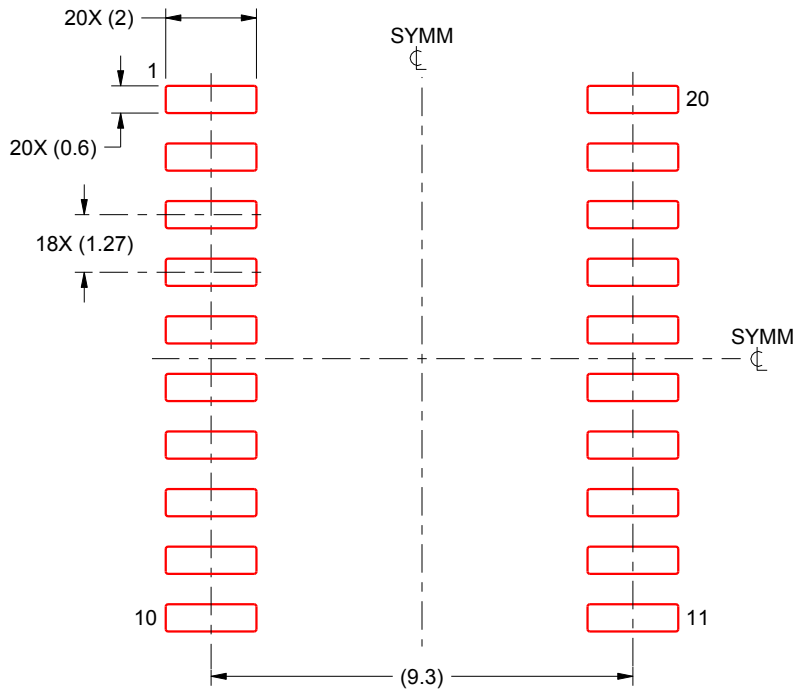
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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