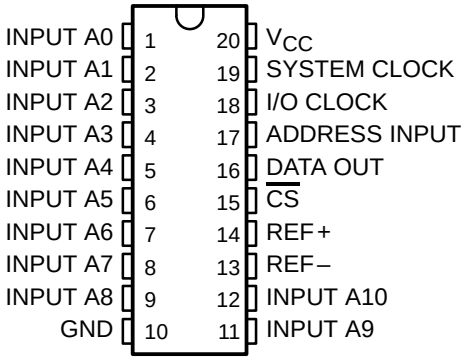
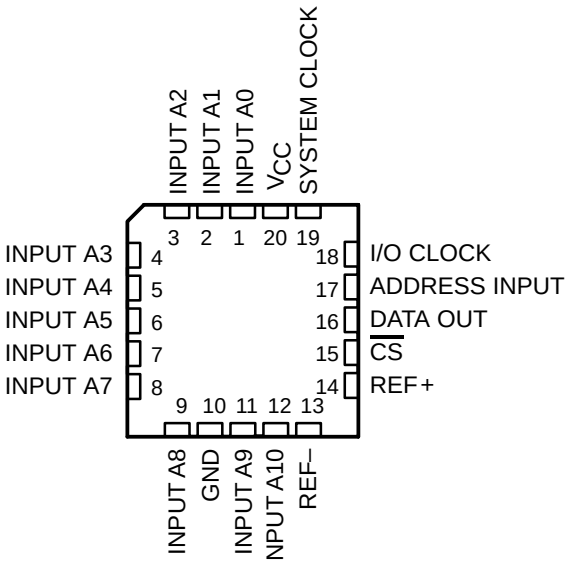
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **TLC541 Is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 Is Capable of Higher Speed**
- **Pinout and Control Signals Compatible With TLC1540 Family of 10-Bit A/D Converters**
- **CMOS Technology**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PARAMETER	TLC540	TLC541
Channel Acquisition Sample Time	2 µs	3.6 µs
Conversion Time (Max)	9 µs	17 µs
Samples per Second (Max)	75×10^3	40×10^3
Power Dissipation (Max)	12.5 mW	12.5 mW

description

The TLC540 and TLC541 are CMOS A/D converters built around an 8-bit switched-capacitor successive-approximation A/D converters. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs, including independent SYSTEM CLOCK, I/O CLOCK, chip select ($\overline{CS}$), and ADDRESS INPUT. A 4-MHz system clock for the TLC540 and a 2.1-MHz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SO PLASTIC DIP (DW)	PLASTIC DIP (N)	CHIP CARRIER (FN)
–40°C to 85°C	— TLC541IDW	TLC540IN TLC541IN	TLC540IFN TLC541IFN
–55°C to 125°C	—	TLC541MN	—

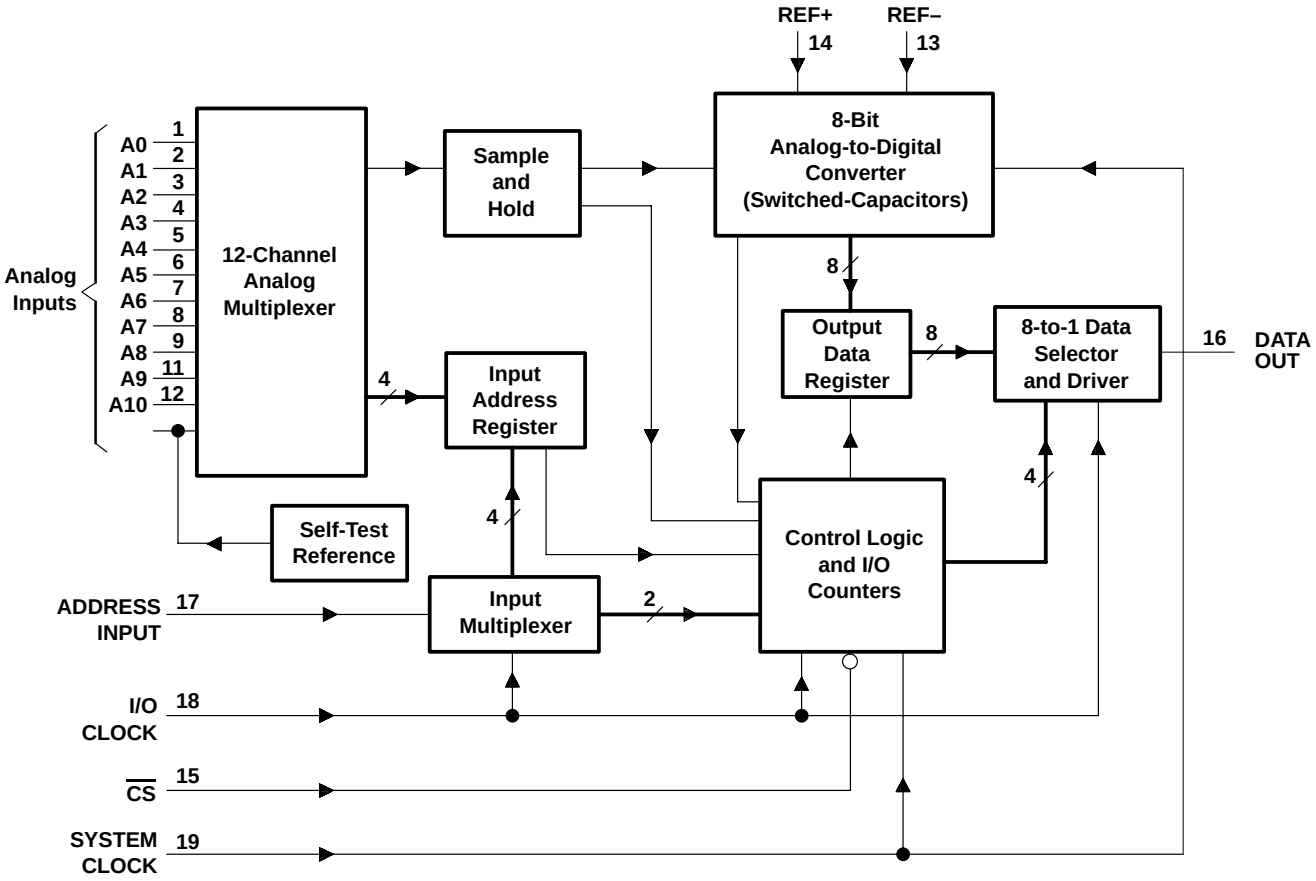
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

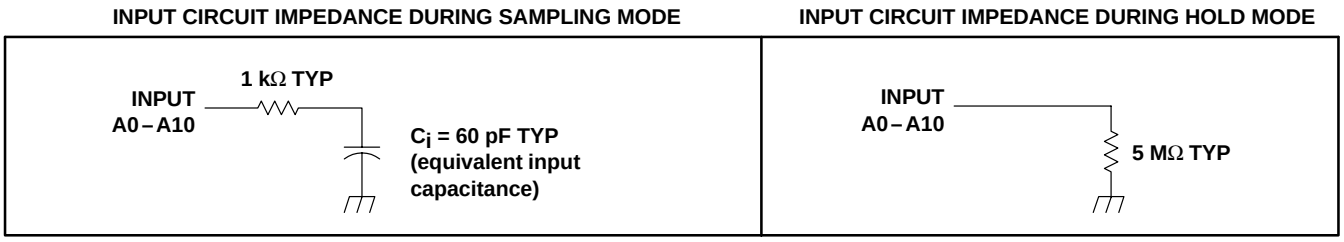
The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 9 μs for the TLC540 and 17 μs for the TLC541 over the full operating temperature range.

The TLC540I and TLC541I are characterized for operation from –40°C to 85°C.The TLC541M is characterized for operation from –55°C to 125°C.

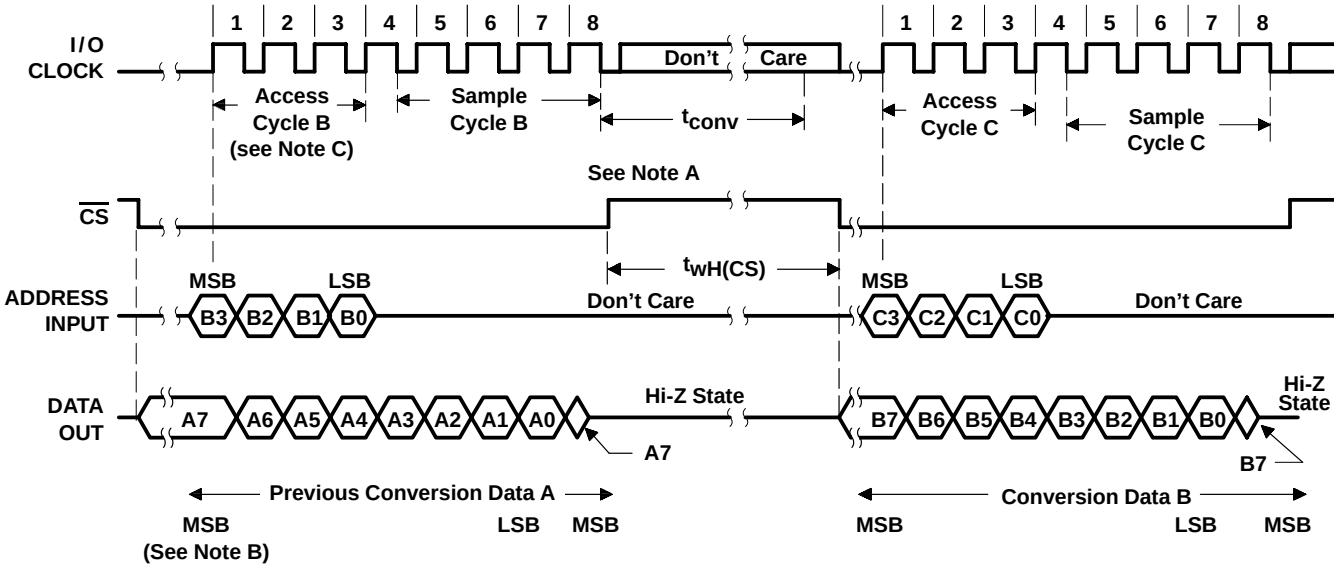
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated on the 8th falling edge of I/O CLOCK after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, I/O CLOCK must remain low for at least 36 system clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.

C. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	–0.3 V to V_{CC} +0.3 V
Output voltage range, V_O	–0.3 V to V_{CC} +0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, T_A: TLC540I, TLC541I	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)			–0.1	0	2.5	– 0.1	0	2.5	V
Differential reference voltage, $V_{ref+} – V_{ref-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$			200			400			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
I/O CLOCK frequency, $f_{clock(I/O)}$			0		2.048	0		1.1	MHz
Pulse duration, SYSTEM CLOCK frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		4	$f_{clock(I/O)}$		2.1	MHz
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$			110			210			MHz
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$			100			190			MHz
Pulse duration, I/O clock high, $t_{wH(I/O)}$			200			404			ns
Pulse duration, I/O clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \le 1048$ kHz			30			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{clock(I/O)} \le 525$ kHz			100			100	
		$f_{clock(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540I, TLC541I	–40		85	–40		85	°C

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all 1s (11111111), while input voltages less than that applied to REF– convert as all 0s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF– voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three SYSTEM CLOCK cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{ref+} = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC540 or $f_{clock(I/O)}$ = 1.1 MHz for TLC541 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, DATA OUT		V_{CC} = 4.75 V, I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 1.6 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}, $\overline{CS}$ at V_{CC}			10	μA
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}		0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0		−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}		−0.4	−1	
I_{CC} + I_{ref}	Supply and reference current		V_{ref+} = V_{CC}, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

† All typical values are at T_A = 25°C.

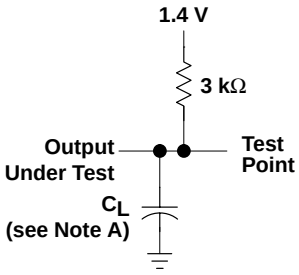
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} - 4.75$ V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC540 or 1.1 MHz for TLC541, $f_{clock(SYS)}$ = 4 MHz for TLC540 or 2.1 MHz for TLC541

PARAMETER		TEST CONDITIONS	TLC540		TLC541		UNIT
			MIN	MAX	MIN	MAX	
E_L	Linearity error	See Note 5		±0.5		±0.5	LSB
E_{ZS}	Zero–scale error	See Notes 2 and 6		±0.5		±0.5	LSB
E_{FS}	Full-scale error	See Notes 2 and 6		±0.5		±0.5	LSB
	Total unadjusted error	See Note 7		±0.5		±0.5	LSB
	Self-test output code	Input A11 address = 1011, (see Note 8)	01111101 (125)	10000011 (131)	01111101 (125)	10000011 (131)	
t_{conv}	Conversion time	See operating sequence		9		17	µs
	Total access and conversion time	See operating sequence		13.3		25	µs
t_a	Channel acquisition time (sample cycle)	See operating sequence		4		4	I/O clock cylces
t_v	Time output data remains valid after I/O CLOCK↓		10		10		ns
t_d	Delay time, I/O CLOCK↓ to data output valid	See Parameter Measurement Information		300		400	ns
t_{en}	Output enable time			150		150	ns
t_{dis}	Output disable time			150		150	ns
$t_{r(bus)}$	Data bus rise time			300		300	ns
$t_{f(bus)}$	Data bus fall time			300		300	ns

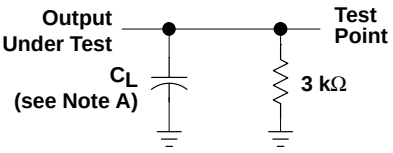
NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all 1s (11111111) while input voltages less than that applied to REF– convert to all 0s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF– voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.

PARAMETER MEASUREMENT INFORMATION

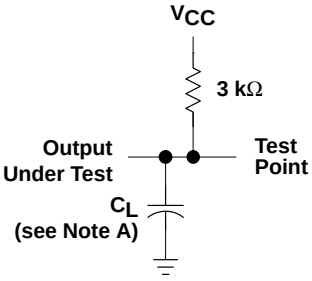


LOAD CIRCUIT FOR t_d, t_r, AND t_f



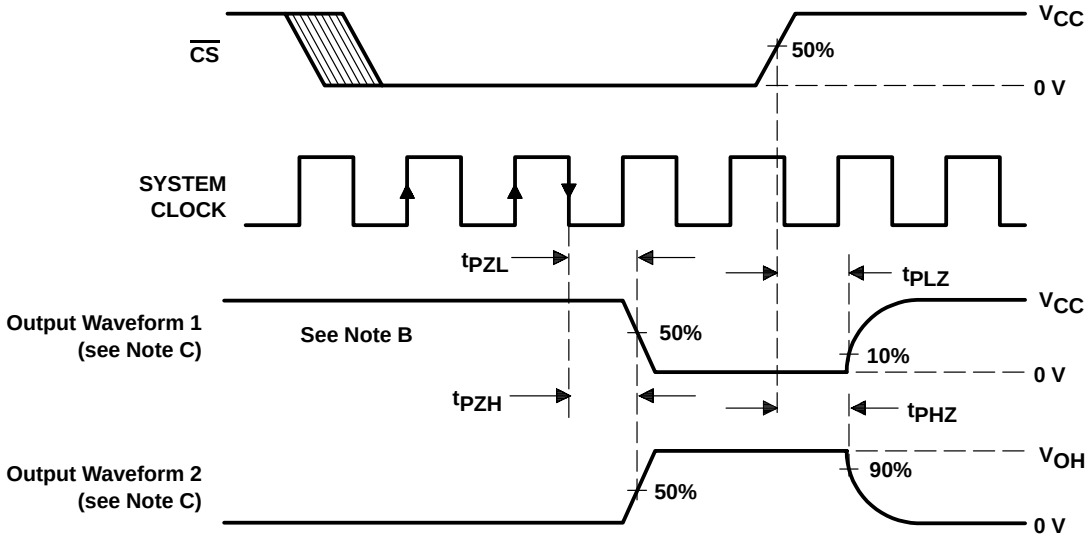
See Note B

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

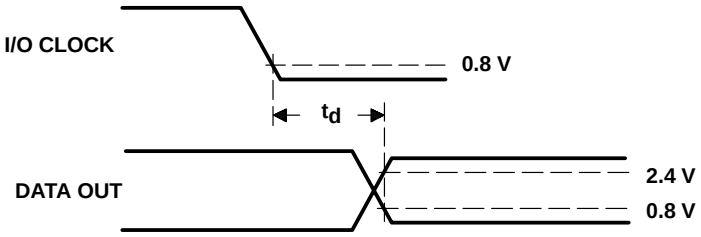


See Note B

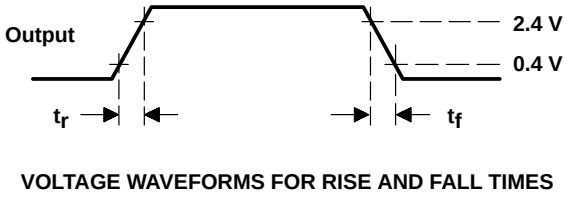
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541.
B. $t_{en} = t_{PZH}$ or t_{PZL}, $t_{dis} = t_{PHZ}$ or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1-e^{-t_c/R_tC_i}\right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ LSB) = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/512\right) = V_S\left(1-e^{-t_c/R_tC_i}\right) \quad (3)$$

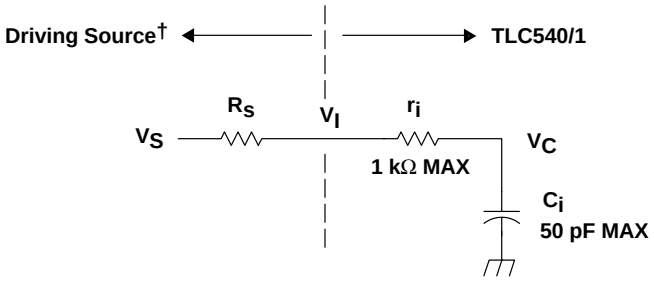
and

$$t_c\ (1/2\ LSB) = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ LSB) = (R_S + 1\ k\Omega) \times 60\ pF \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0 – A10
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance
C_i = Equivalent Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 μs, while complete input-conversion-output cycles can be repeated every 13 μs. With TLC541 a conversion can be completed in 17 μs, while complete input-conversion-output cycles are repeated every 25 μs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in self-test and in any order desired by the controlling processor.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to SYSTEM CLOCK, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK will drive the conversion crunching circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of $\overline{CS}$, to share a control logic point with their counterpart terminals on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to I/O CLOCK and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion in progress.

A new conversion can be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O clock together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. The first two clocks are required for this device to recognize $\overline{CS}$ is at a valid low level when the common clock signal is used as an I/O CLOCK. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low $\overline{CS}$ must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a $\overline{CS}$ transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the eighth valid (10 total) I/O CLOCK. Otherwise, additional common clock cycles are recognized as I/O CLOCKS and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth valid I/O clock cycle, the hold function is not initiated until the negative edge of the eighth valid I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the eighth valid I/O clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 continues sampling the analog input until the eighth falling edge of the I/O clock. The control circuitry or software then immediately lowers the I/O clock signal and holds the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC540IDW	LIFEBUY	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	TLC540I	
TLC540IDWR	LIFEBUY	SOIC	DW	20		TBD	Call TI	Call TI		TLC540I	
TLC540IFN	LIFEBUY	PLCC	FN	20		TBD	Call TI	Call TI		TLC540I	
TLC540IFNG3	LIFEBUY	PLCC	FN	20		TBD	Call TI	Call TI		TLC540I	
TLC540IFNR	LIFEBUY	PLCC	FN	20		TBD	Call TI	Call TI		TLC540I	
TLC540IN	LIFEBUY	PDIP	N	20		TBD	Call TI	Call TI		TLC540IN	
TLC541IDW	LIFEBUY	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	TLC541I	
TLC541IDWR	LIFEBUY	SOIC	DW	20		TBD	Call TI	Call TI		TLC541I	
TLC541IFN	LIFEBUY	PLCC	FN	20		TBD	Call TI	Call TI		TLC541I	
TLC541IFNR	LIFEBUY	PLCC	FN	20		TBD	Call TI	Call TI		TLC541I	
TLC541IN	LIFEBUY	PDIP	N	20		TBD	Call TI	Call TI		TLC541IN	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

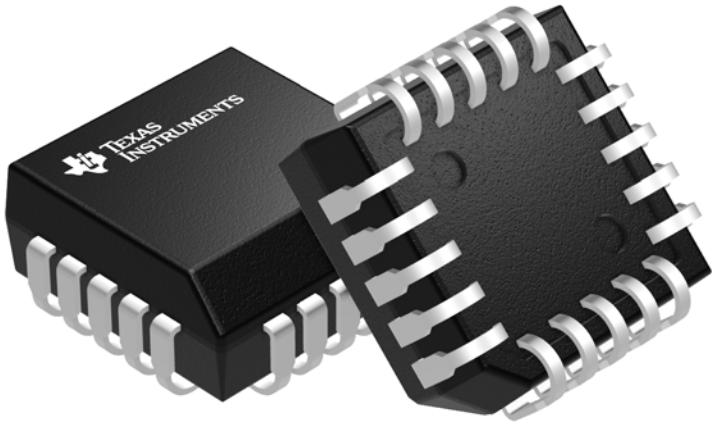
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

FN 20 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

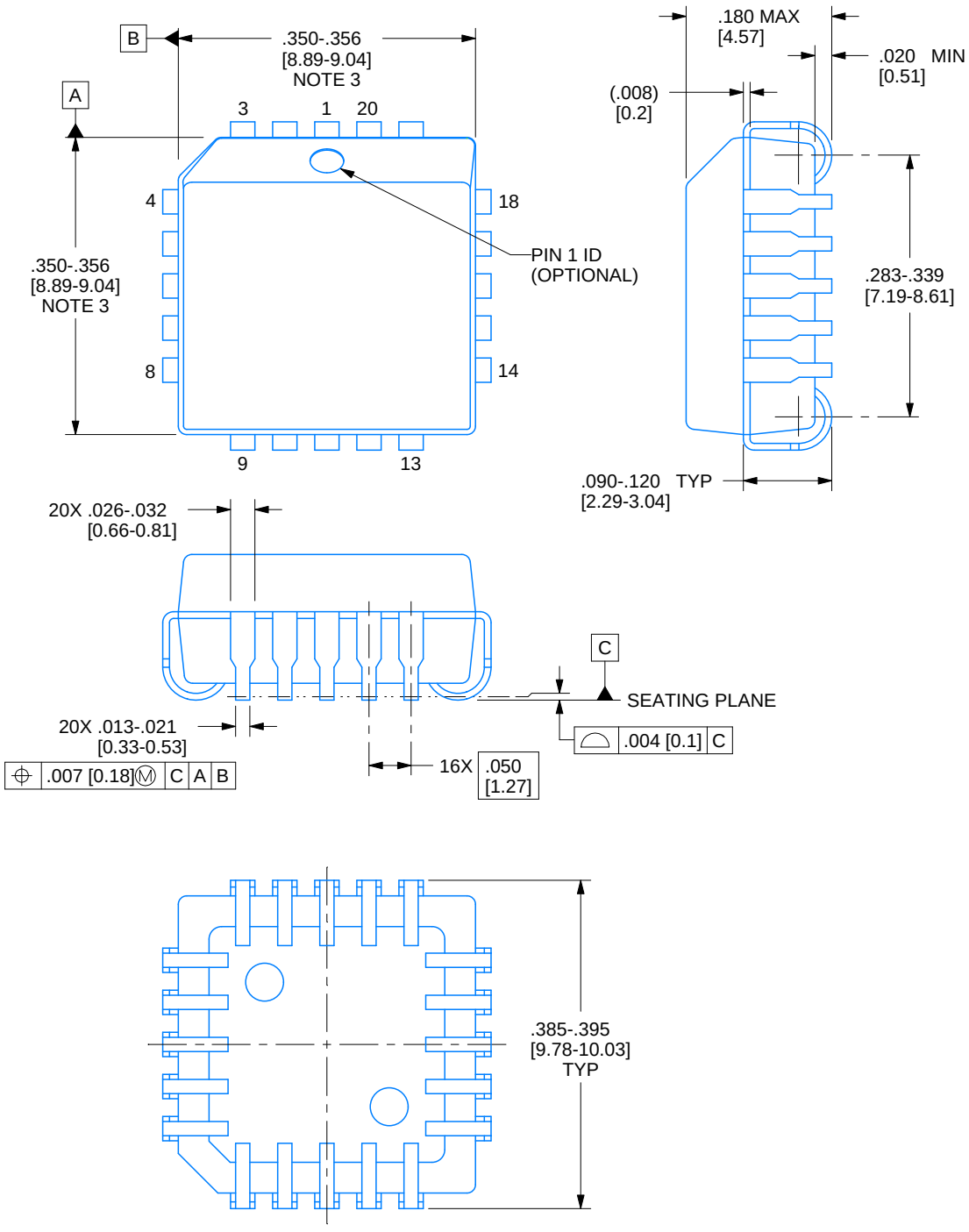
4040005-2/C

PACKAGE OUTLINE

FN0020A

PLCC - 4.57 mm max height

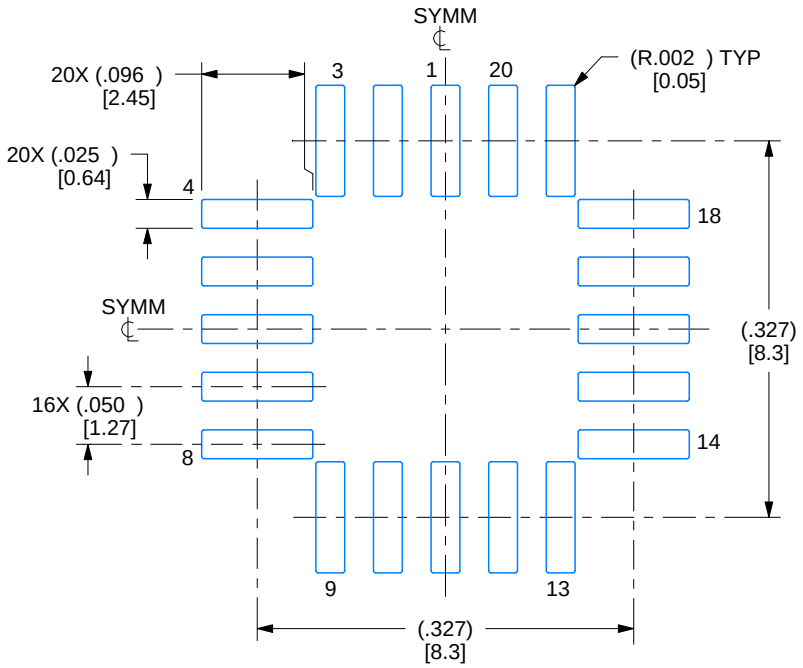
PLASTIC CHIP CARRIER



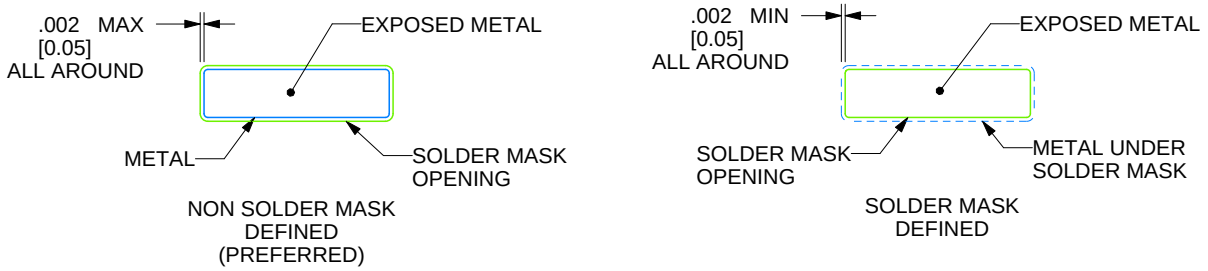
4215152/B 04/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

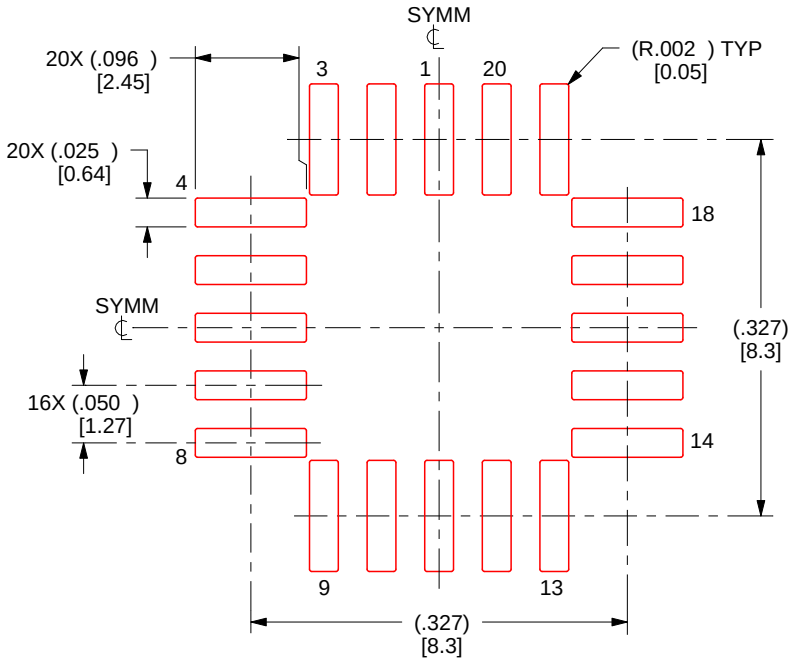


SOLDER MASK DETAILS

4215152/B 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215152/B 04/2017

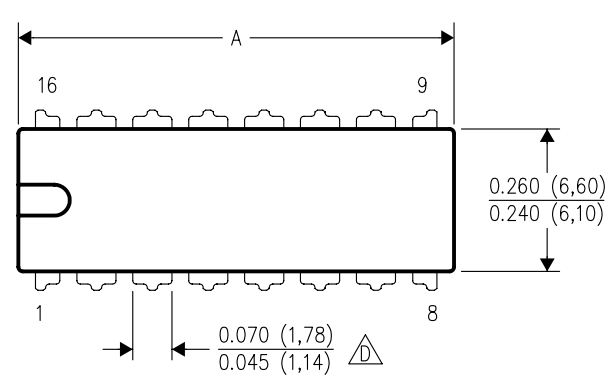
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

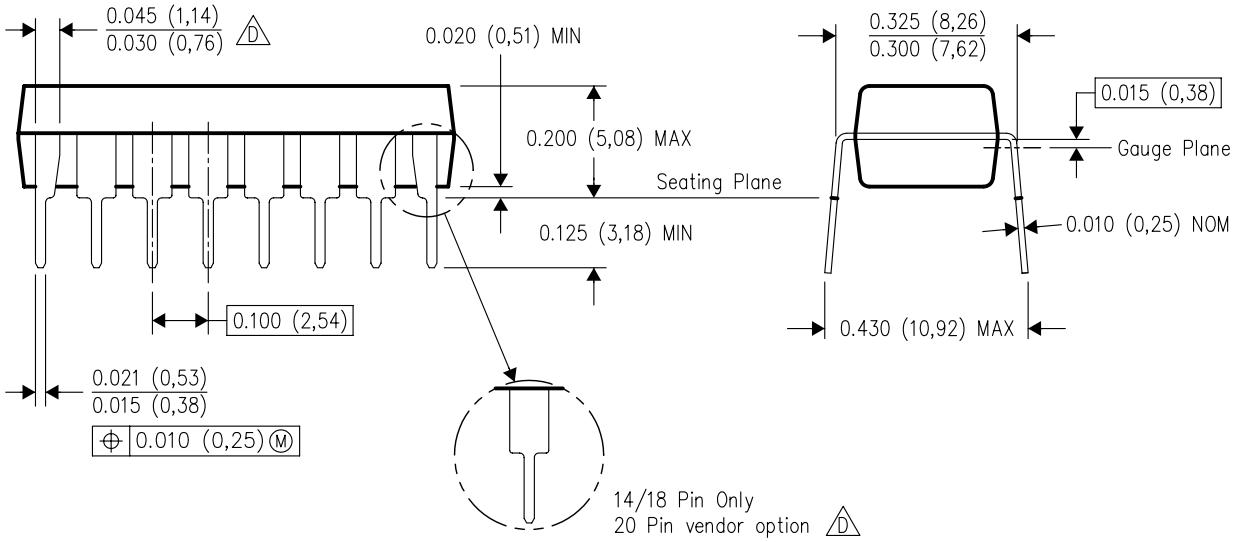
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

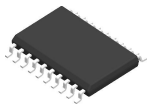


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

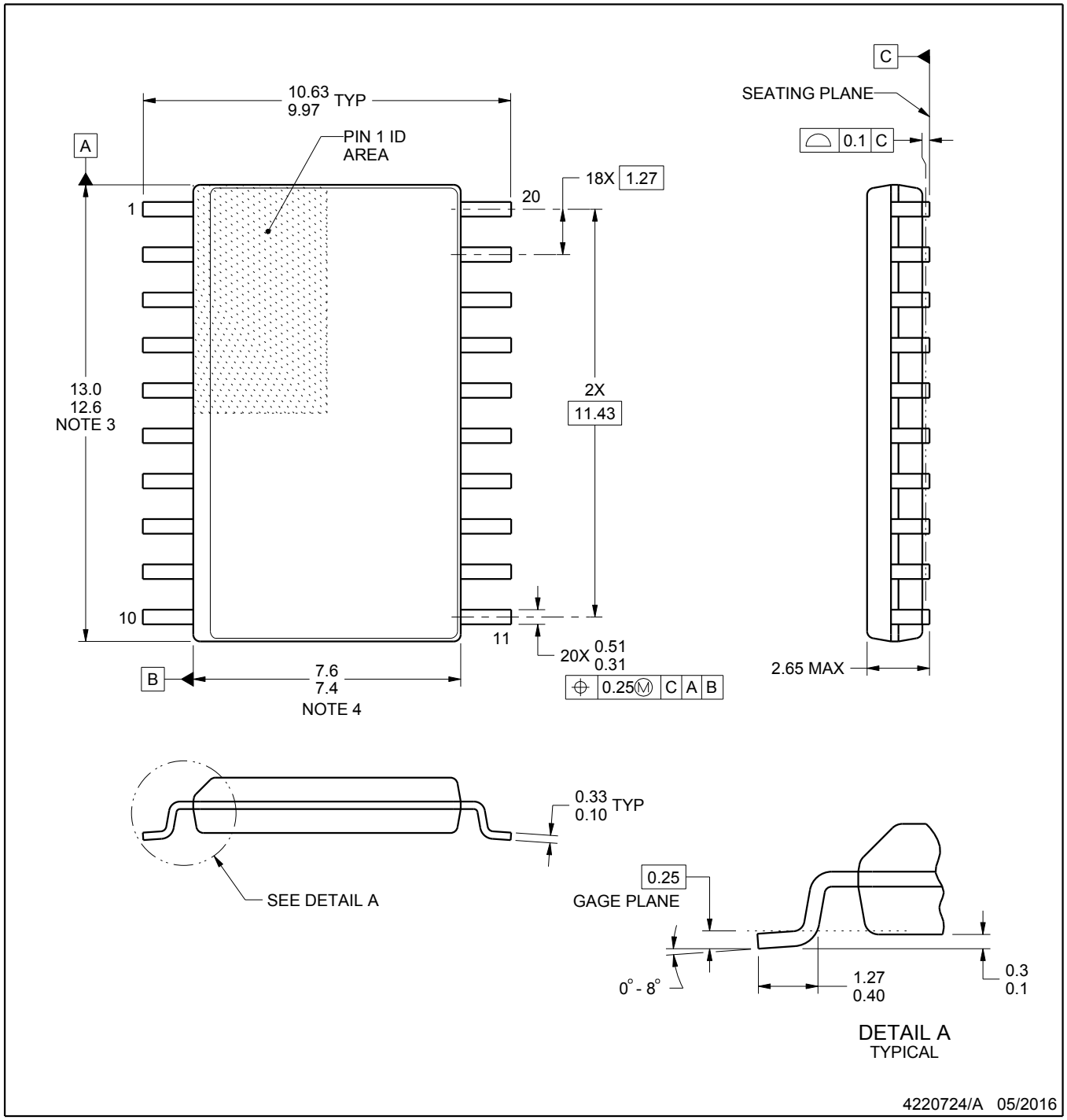


PACKAGE OUTLINE

DW0020A

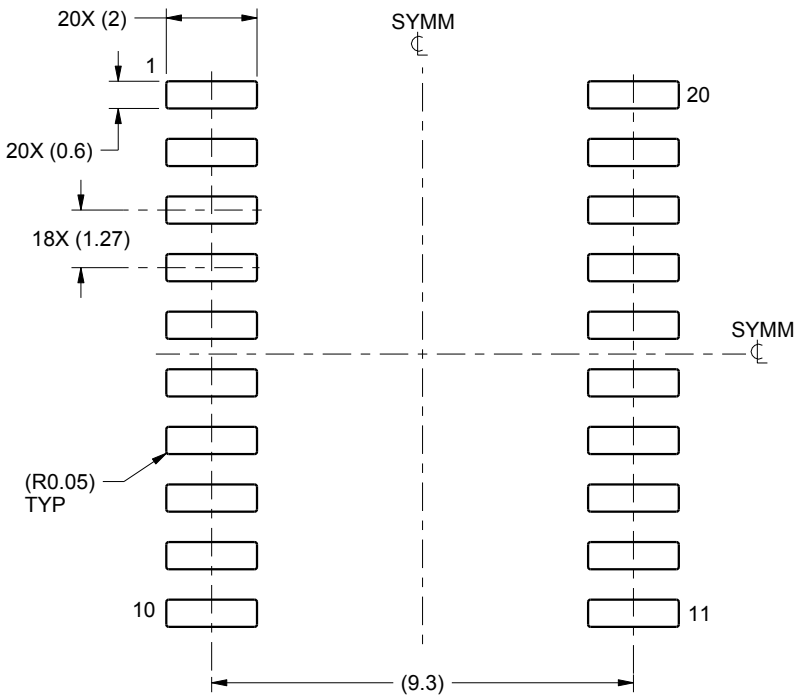
SOIC - 2.65 mm max height

SOIC

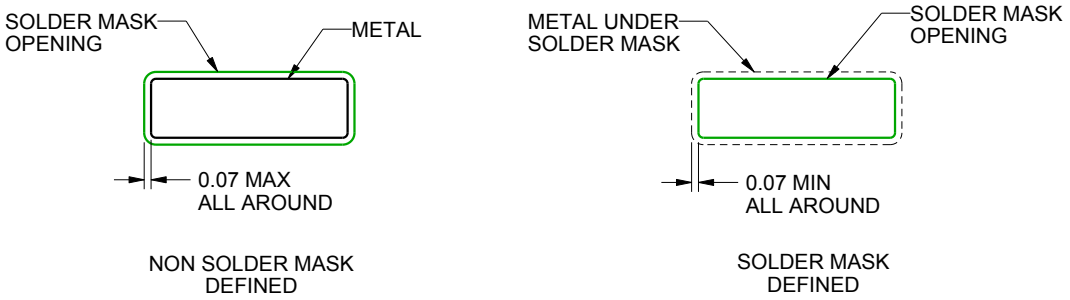


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

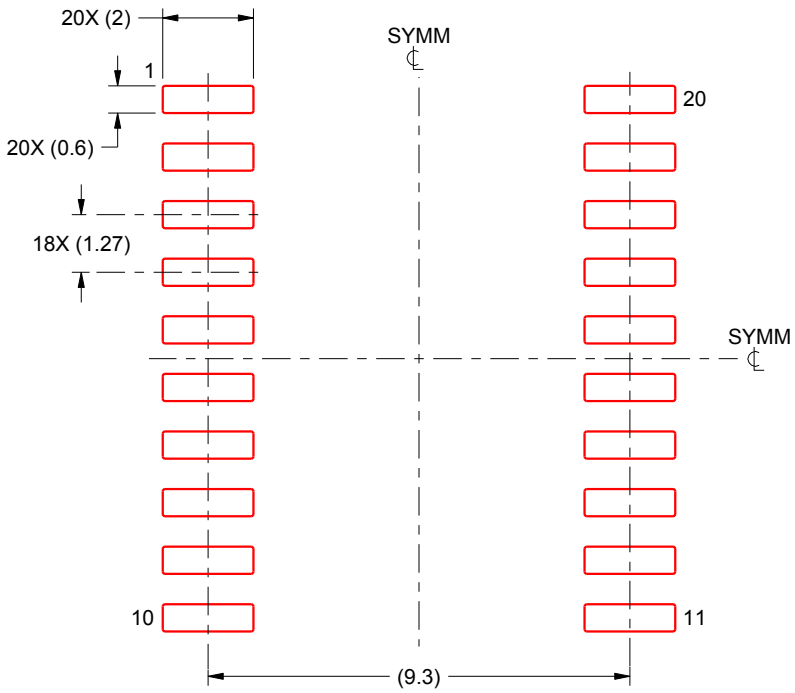


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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