National Semiconductor

PRELIMINARY

HPC16083/HPC26083/HPC36083/HPC46083/ HPC16003/HPC26003/HPC36003/HPC46003 High-Performance microControllers

General Description

The HPC16083 and HPC16003 are members of the HPC™ family of High Performance microControllers. Each member of the family has the same core CPU with a unique memory and I/O configuration to suit specific applications. The HPC16083 has 8k bytes of on-chip ROM. The HPC16003 has no on-chip ROM and is intended for use with external direct memory. Each part is fabricated in National's advanced microCMOS technology. This process combined with an advanced architecture provides fast, flexible I/O control, efficient data manipulation, and high speed computation.

The HPC devices are complete microcomputers on a single chip. All system timing, internal logic, ROM, RAM, and I/O are provided on the chip to produce a cost effective solution for high performance applications. On-chip functions such as UART, up to eight 16-bit timers with 4 input capture registers, vectored interrupts, WATCHDOG™ logic and MICROWIRE/PLUS™ provide a high level of system integration. The ability to address up to 64k bytes of external memory enables the HPC to be used in powerful applications typically performed by microprocessors and expensive peripheral chips. The term "HPC16083" is used throughout this datasheet to refer to the HPC16083 and HPC16003 devices unless otherwise specified.

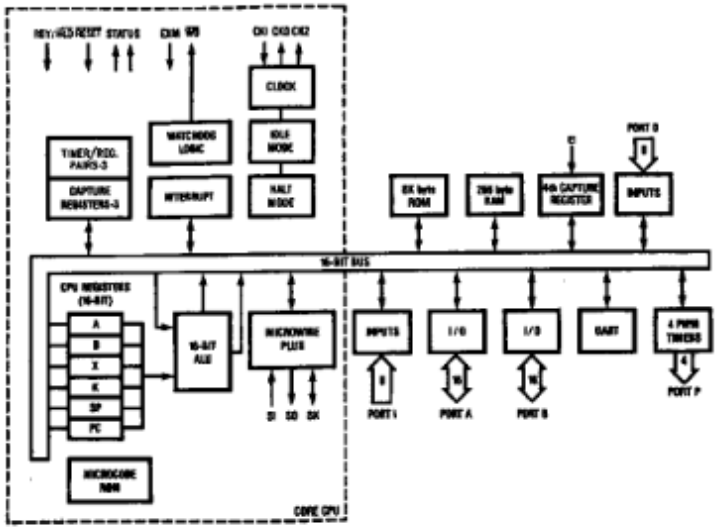
The microCMOS process results in very low current drain and enables the user to select the optimum speed/power product for his system. The IDLE and HALT modes provide further current savings. The HPC is available in 68-pin PLCC, LDCC, PGA and 80-Pin PQFP packages.

Features

- HPC family—core features:
  - 16-bit architecture, both byte and word
  - 16-bit data bus, ALU, and registers
  - 64k bytes of external direct memory addressing
  - FAST—200 ns for fastest instruction when using 20.0 MHz clock, 134 ns at 30 MHz
  - High code efficiency—most instructions are single byte
  - 16 x 16 multiply and 32 x 16 divide
  - Eight vectored interrupt sources
  - Four 16-bit timer/counters with 4 synchronous outputs and WATCHDOG logic
  - MICROWIRE/PLUS serial I/O interface
  - CMOS—very low power with two power save modes: IDLE and HALT
- UART—full duplex, programmable baud rate
- Four additional 16-bit timer/counters with pulse width modulated outputs
- Four input capture registers
- 52 general purpose I/O lines (memory mapped)
- 8k bytes of ROM, 256 bytes of RAM on chip
- ROMless version available (HPC16003)
- Commercial (0°C to +70°C), industrial (−40°C to +85°C), automotive (−40°C to +105°C) and military (−55°C to +125°C) temperature ranges

For applications requiring more RAM and ROM see HPC16064 data sheet.

Block Diagram (HPC16083 with 8k ROM shown)



TL/DD/8801-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Allowable Source or Sink Current	100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
V_{CC} with Respect to GND	−0.5V to 7.0V
All Other Pins	(V_{CC} + 0.5)V to (GND − 0.5)V

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C for HPC46083/HPC46003, −40°C to +85°C for HPC36083/HPC36003, −40°C to +105°C for HPC26083/HPC26003, −55°C to +125°C for HPC16083/HPC16003

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC_1}	Supply Current	V_{CC} = 5.5V, f_{in} = 30 MHz (Note 1)		65	mA
		V_{CC} = 5.5V, f_{in} = 20 MHz (Note 1)		47	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz (Note 1)		10	mA
I_{CC_2}	IDLE Mode Current	V_{CC} = 5.5V, f_{in} = 30 MHz (Note 1)		5.0	mA
		V_{CC} = 5.5V, f_{in} = 20 MHz, (Note 1)		3.0	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz, (Note 1)		1	mA
I_{CC_3}	HALT Mode Current	V_{CC} = 5.5V, f_{in} = 0 kHz, (Note 1)		200	µA
		V_{CC} = 2.5V, f_{in} = 0 kHz, (Note 1)		50	µA
INPUT VOLTAGE LEVELS FOR SCHMITT TRIGGERED INPUTS $\overline{RESET}$, NMI AND $\overline{WO}$; AND ALSO CKI					
V_{IH_1}	Logic High		0.9 V_{CC}		V
V_{IL_1}	Logic Low			0.1 V_{CC}	V
ALL OTHER INPUTS					
V_{IH_2}	Logic High		0.7 V_{CC}		V
V_{IL_2}	Logic Low			0.2 V_{CC}	V
I_{LI1}	Input Leakage Current	V_{IN} = 0 and V_{IN} = V_{CC}		±2	µA
I_{LI2}	Input Leakage Current RDY/$\overline{HLD}$, $\overline{EXUI}$	V_{IN} = 0	−3	−50	µA
I_{LI3}	Input Leakage Current B12	$\overline{RESET}$ = 0, V_{IN} = V_{CC}	0.5	7	mA
C_I	Input Capacitance	(Note 2)		10	pF
C_{IO}	I/O Capacitance	(Note 2)		20	pF
OUTPUT VOLTAGE LEVELS					
V_{OH_1}	Logic High (CMOS)	I_{OH} = −10 µA (Note 2)	V_{CC} − 0.1		V
V_{OL_1}	Logic Low (CMOS)	I_{OH} = 10 µA (Note 2)		0.1	V
V_{OH_2}	Port A/B Drive, CK2 (A_0–A_{15}, B_{10}, B_{11}, B_{12}, B_{15})	I_{OH} = −7 mA	2.4		V
V_{OL_2}		I_{OL} = 3 mA		0.4	V
V_{OH_3}	Other Port Pin Drive, $\overline{WO}$ (open drain) (B_0–B_9, B_{13}, B_{14}, P_0–P_3)	I_{OH} = −1.6 mA (except $\overline{WO}$)	2.4		V
V_{OL_3}		I_{OL} = 0.5 mA		0.4	V
V_{OH4}	ST1 and ST2 Drive	I_{OH} = −6 mA	2.4		V
V_{OL_4}		I_{OL} = 1.6 mA		0.4	V
V_{OH5}	Port A/B Drive (A_0–A_{15}, B_{10}, B_{11}, B_{12}, B_{15}) when used as External Address/Data Bus	I_{OH} = −1 mA	2.4		V
V_{OL5}		I_{OL} = 3 mA		0.4	V
V_{RAM}	RAM Keep-Alive Voltage	(Note 3)	2.5	V_{CC}	V
I_{OZ}	TRI-STATE® Leakage Current	V_{IN} = 0 and V_{IN} = V_{CC}		±5	µA

Note 1: I_{CC_1}, I_{CC_2}, I_{CC_3} measured with no external drive (I_{OH} and I_{OL} = 0, I_{IH} and I_{IL} = 0). I_{CC_1} is measured with $\overline{RESET}$ = V_{SS}, I_{CC_3} is measured with NMI = V_{CC}. CKI driven to V_{IH1} and V_{IL1}, with rise and fall times less than 10 ns.

Note 2: This is guaranteed by design and not tested.

Note 3: Test duration is 100 ms.

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20 MHz

AC Electrical Characteristics

(See Notes 1 and 4 and *Figure 1* thru *Figure 5*) V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C for HPC46083/HPC46003, −40°C to +85°C for HPC36083/HPC36003, −40°C to +105°C for HPC26083/HPC26003, −55°C to +125°C for HPC16083/HPC16003

	Symbol and Formula	Parameter	Min	Max	Units	Note
Clocks	f_C	CKI Operating Frequency	2	20	MHz	
	$t_{C1} = 1/f_C$	CKI Clock Period	50	500	ns	
	t_{CKIH}	CKI High Time	22.5		ns	
	t_{CKIL}	CKI Low Time	22.5		ns	
	$t_C = 2/f_C$	CPU Timing Cycle	100		ns	
	$t_{WAIT} = t_C$	CPU Wait State Period	100		ns	
	t_{DC1C2R}	Delay of CK2 Rising Edge after CKI Falling Edge	0	55	ns	(Note 1)
	t_{DC1C2F}	Delay of CK2 Falling Edge after CK1 Falling Edge	0	55	ns	(Note 1)
	$f_U = f_C/8$	External UART Clock Input Frequency		2.5**	MHz	
	f_{MW}	External MICROWIRE/PLUS Clock Input Frequency		1.25	MHz	
Timers	$f_{XIN} = f_C/22$	External Timer Input Frequency		0.91	MHz	
	$t_{XIN} = t_C$	Pulse Width for Timer Inputs	100		ns	
MICROWIRE/PLUS	t_{UWS}	MICROWIRE Setup Time—Master —Slave	100 20		ns	
	t_{UWH}	MICROWIRE Hold Time—Master —Slave	20 50		ns	
	t_{UWV}	MICROWIRE Output Valid Time—Master —Slave		50 150	ns	
External Hold	$t_{SALE} = 3/4\ t_C + 40$	$\overline{HLD}$ Falling Edge before ALE Rising Edge	115		ns	
	$t_{HWP} = t_C + 10$	$\overline{HLD}$ Pulse Width	110		ns	
	$t_{HAE} = t_C + 100$	$\overline{HLDA}$ Falling Edge after $\overline{HLD}$ Falling Edge		200	ns	(Note 3)
	$t_{HAD} = 3/4\ t_C + 85$	$\overline{HLDA}$ Rising Edge after $\overline{HLD}$ Rising Edge		160	ns	
	$t_{BF} = 1/2\ t_C + 66$	Bus Float after $\overline{HLDA}$ Falling Edge		116	ns	(Note 5)
	$t_{BE} = 1/2\ t_C + 66$	Bus Enable after $\overline{HLDA}$ Rising Edge	116		ns	(Note 5)
UPI Timing	t_{UAS}	Address Setup Time to Falling Edge of $\overline{URD}$	10		ns	
	t_{UAH}	Address Hold Time from Rising Edge of $\overline{URD}$	10		ns	
	t_{RPW}	$\overline{URD}$ Pulse Width	100		ns	
	t_{OE}	$\overline{URD}$ Falling Edge to Output Data Valid	0	60	ns	
	t_{OD}	Rising Edge of $\overline{URD}$ to Output Data Invalid	5	35	ns	(Note 6)
	t_{DRDY}	$\overline{RDRDY}$ Delay from Rising Edge of $\overline{URD}$		70	ns	
	t_{WDW}	$\overline{UWR}$ Pulse Width	40		ns	
	t_{UDS}	Input Data Valid before Rising Edge of $\overline{UWR}$	10		ns	
	t_{UDH}	Input Data Hold after Rising Edge of $\overline{UWR}$	20		ns	
	t_A	$\overline{WRRDY}$ Delay from Rising Edge of $\overline{UWR}$		70	ns	

**This maximum frequency is attainable provided that this external baud clock has a duty cycle such that the high period includes two (2) falling edges of the CK2 clock.