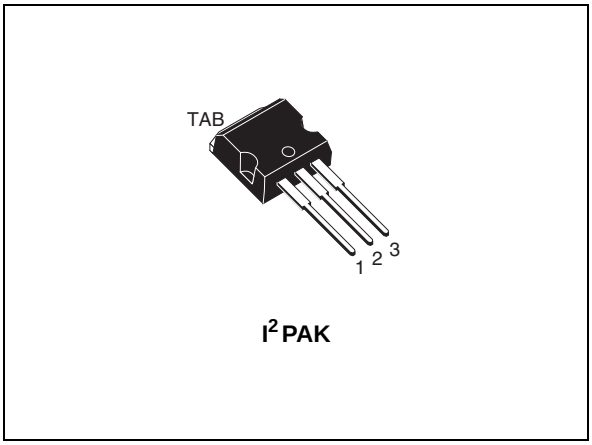
STI5N52U

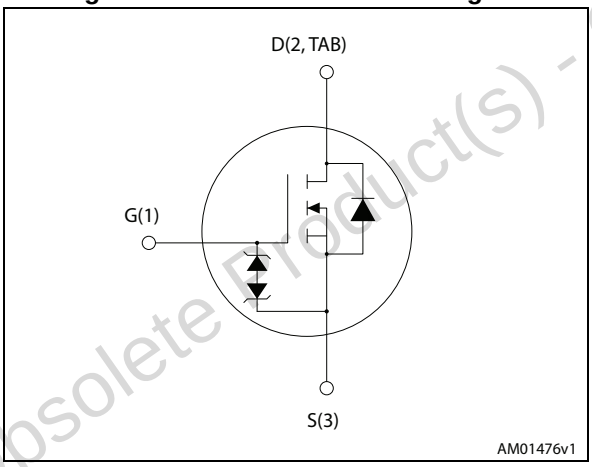
N-channel 525 V, 1.25 Ω typ., 4.4 A UltraFASTmesh™ Power MOSFET in a I^2PAK package

Datasheet - not recommended for new design



I^2PAK

Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STI5N52U	525 V	1.5 Ω	4.4 A	70 W

- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low $R_{DS(on)}$
- Extremely low t_{rr}

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using UltraFASTmesh™ technology, which combines the advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with an enhanced fast body-drain recovery diode.

Table 1. Device summary

Order code	Marking	Package	Packaging
STI5N52U	5N52U	I^2PAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.4	A
I_D	Drain current (continuous) at T_C = 100 °C	2.8	A
I_{DM} (1)	Drain current (pulsed)	17.6	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4.4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	170	mJ
dv/dt(2)	Peak diode recovery voltage slope	20	V/ns
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2800	kV
T_J	Operating junction temperature	-55 to 150 °C	°C
T_{stg}	Storage temperature		°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 4.4 A, di/dt ≤ 400 A/µs, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.78	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	100	°C/W

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	525			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 525 V			10	µA
		V_{DS} = 525 V, T_C=125 °C			500	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.2 A		1.25	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	529	-	pF
C_{oss}	Output capacitance		-	71	-	pF
C_{rss}	Reverse transfer capacitance		-	13.4	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 420 V, V_{GS} = 0	-	11	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 416 V, I_D = 4.4 A, V_{GS} = 10 V *(see Figure 15)*	-	16.9	-	nC
Q_{gs}	Gate-source charge		-	4.2	-	nC
Q_{gd}	Gate-drain charge		-	8.4	-	nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 2.2 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 14)*	-	11.4	-	ns
t_r	Rise time		-	13.6	-	ns
$t_{d(off)}$	Turn-off-delay time		-	23.1	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.4	A
I_{SDM} (1)	Source-drain current (pulsed)		-		17.6	A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.4 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 16)*	-	55		ns
Q_{rr}	Reverse recovery charge		-	95		nC
I_{RRM}	Reverse recovery current		-	3.5		A
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 16)*	-	120		ns
Q_{rr}	Reverse recovery charge		-	266		nC
I_{RRM}	Reverse recovery current		-	4.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

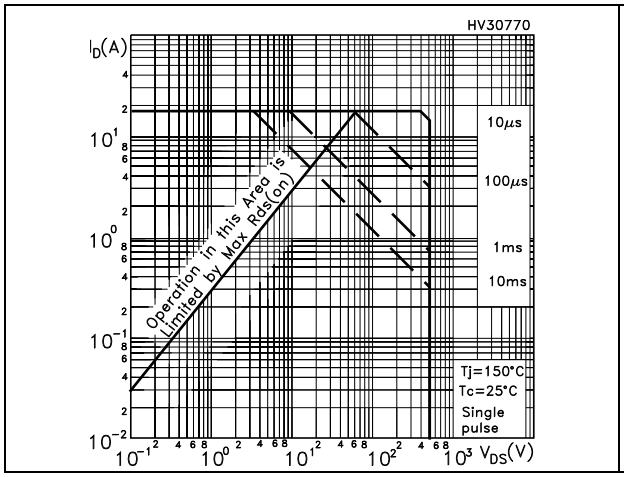


Figure 3. Thermal impedance

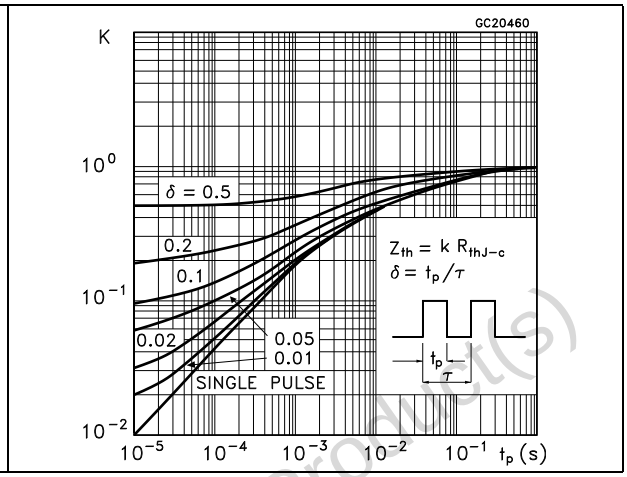


Figure 4. Output characteristics

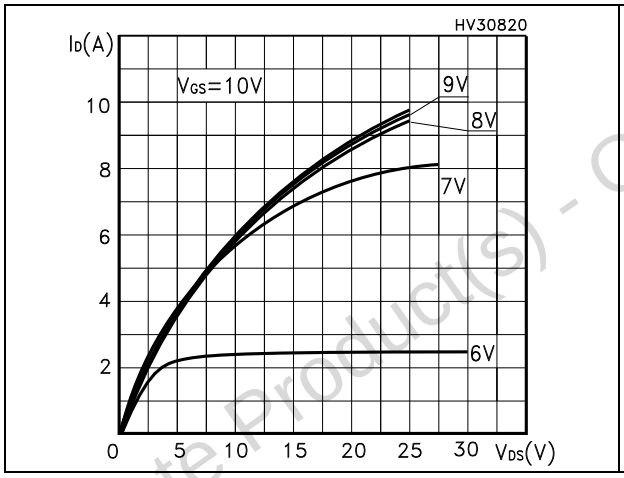


Figure 5. Transfer characteristics

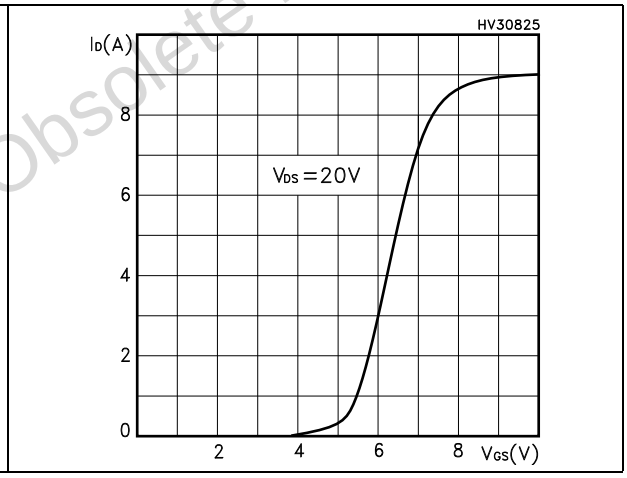


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

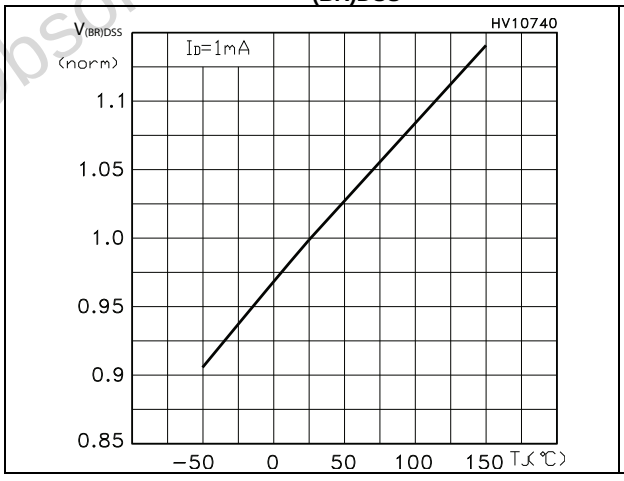


Figure 7. Static drain-source on resistance

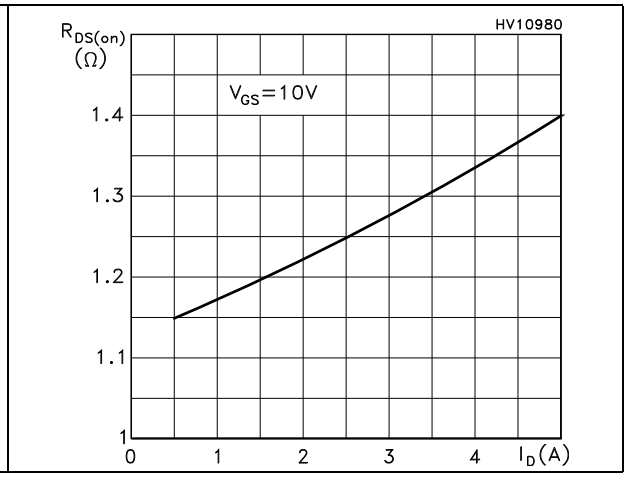


Figure 8. Gate charge vs gate-source voltage

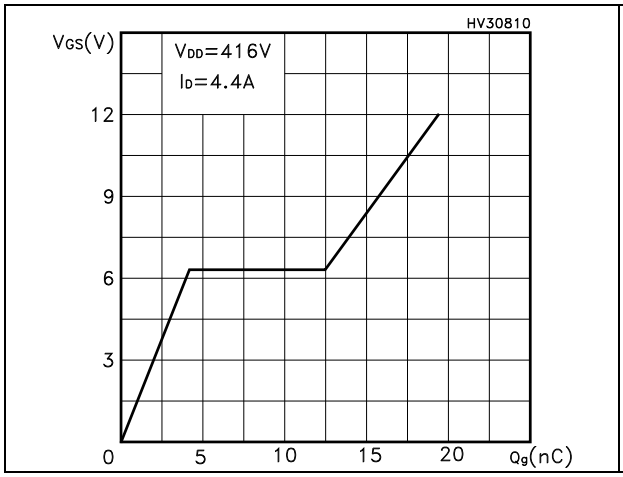


Figure 9. Capacitance variations

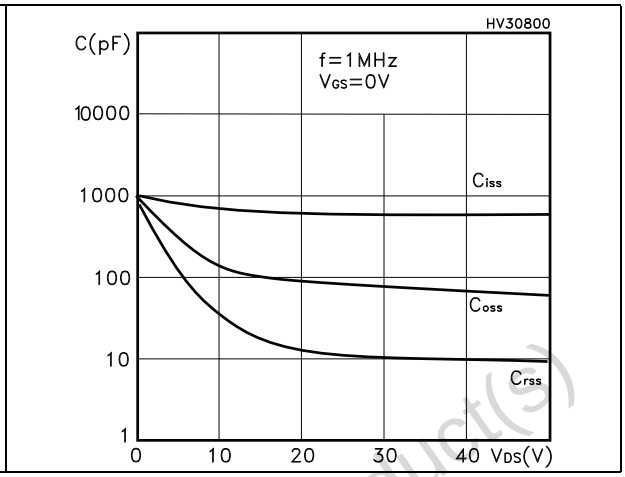


Figure 10. Normalized gate threshold voltage vs temperature

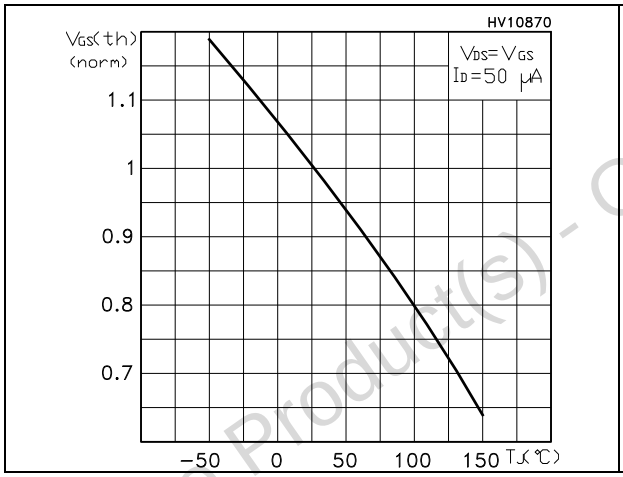


Figure 11. Normalized on-resistance vs temperature

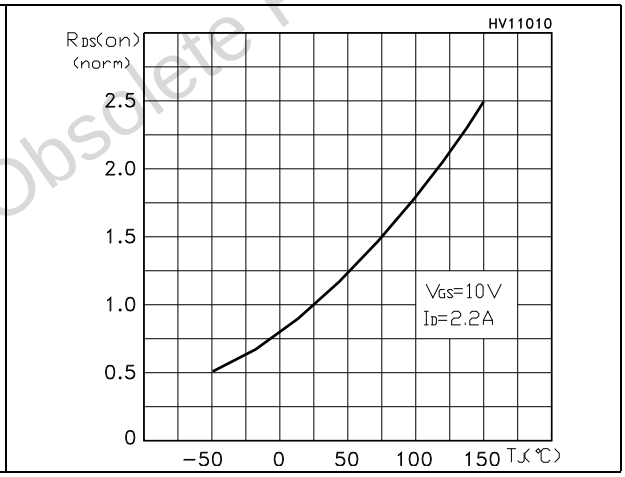


Figure 12. Source-drain diode forward characteristics

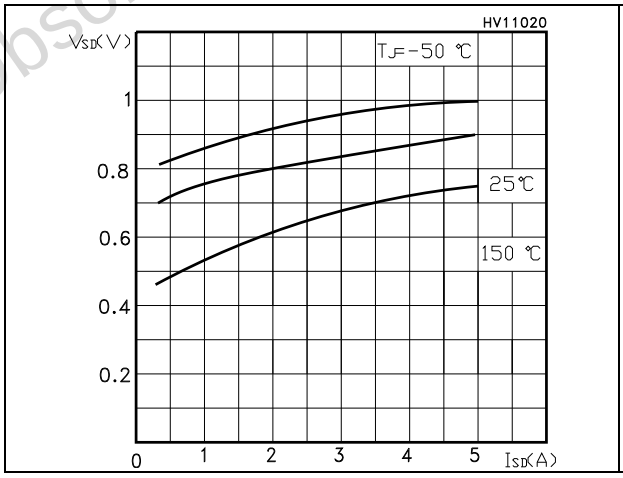
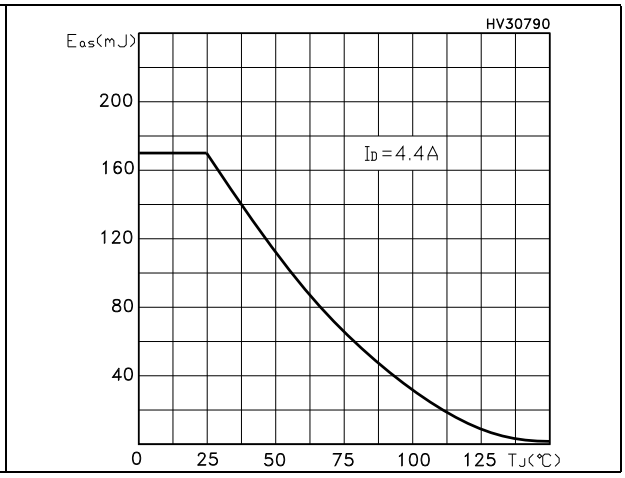


Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

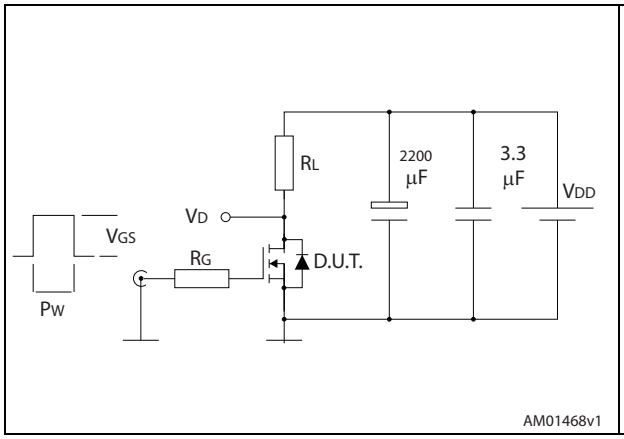


Figure 15. Gate charge test circuit

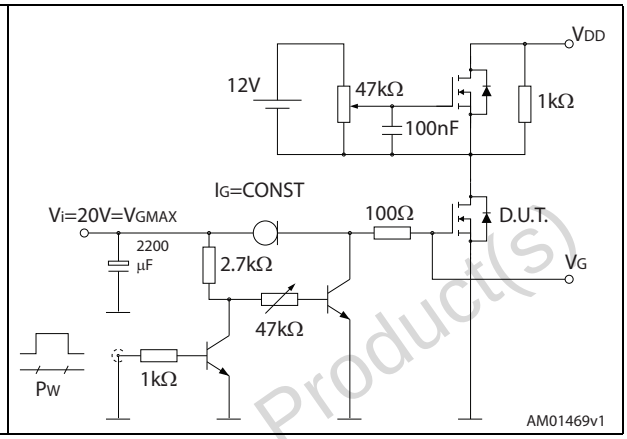


Figure 16. Test circuit for inductive load switching and diode recovery times

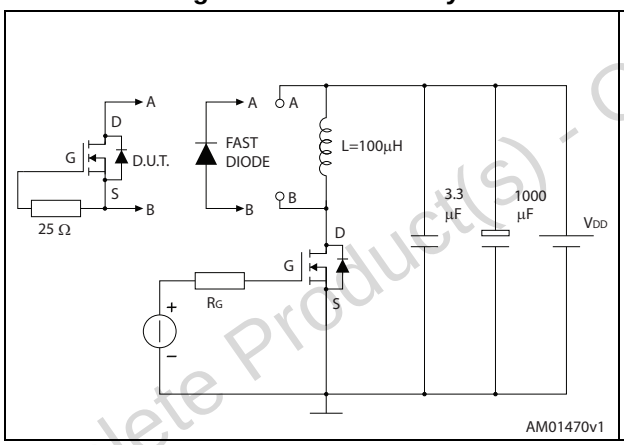


Figure 17. Unclamped inductive load test circuit

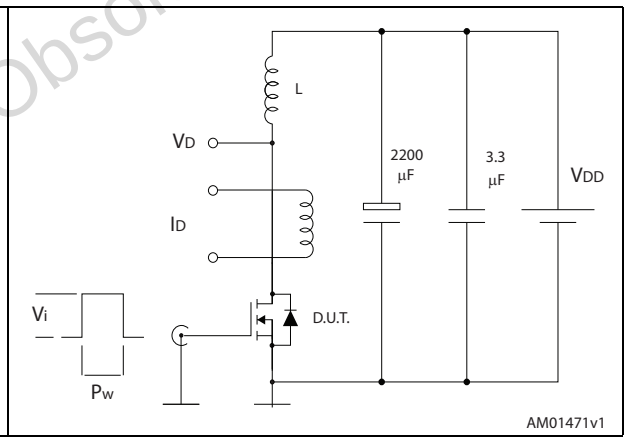


Figure 18. Unclamped inductive waveform

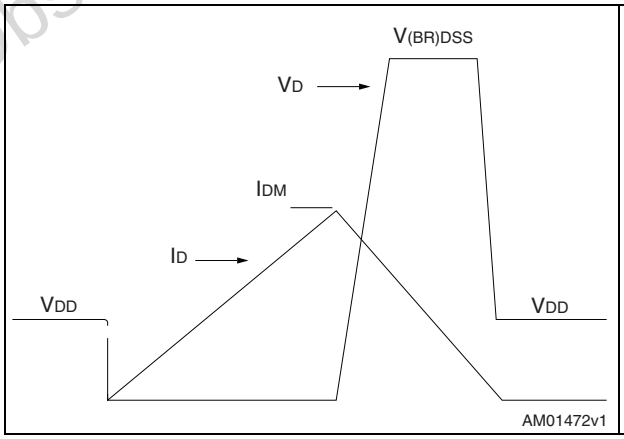
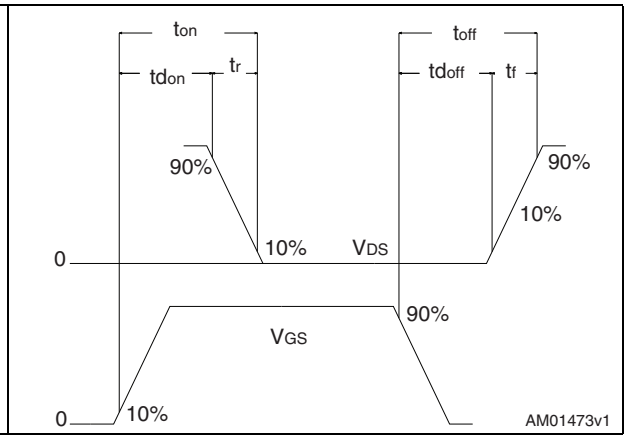


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 20. I²PAK (TO-262) drawing

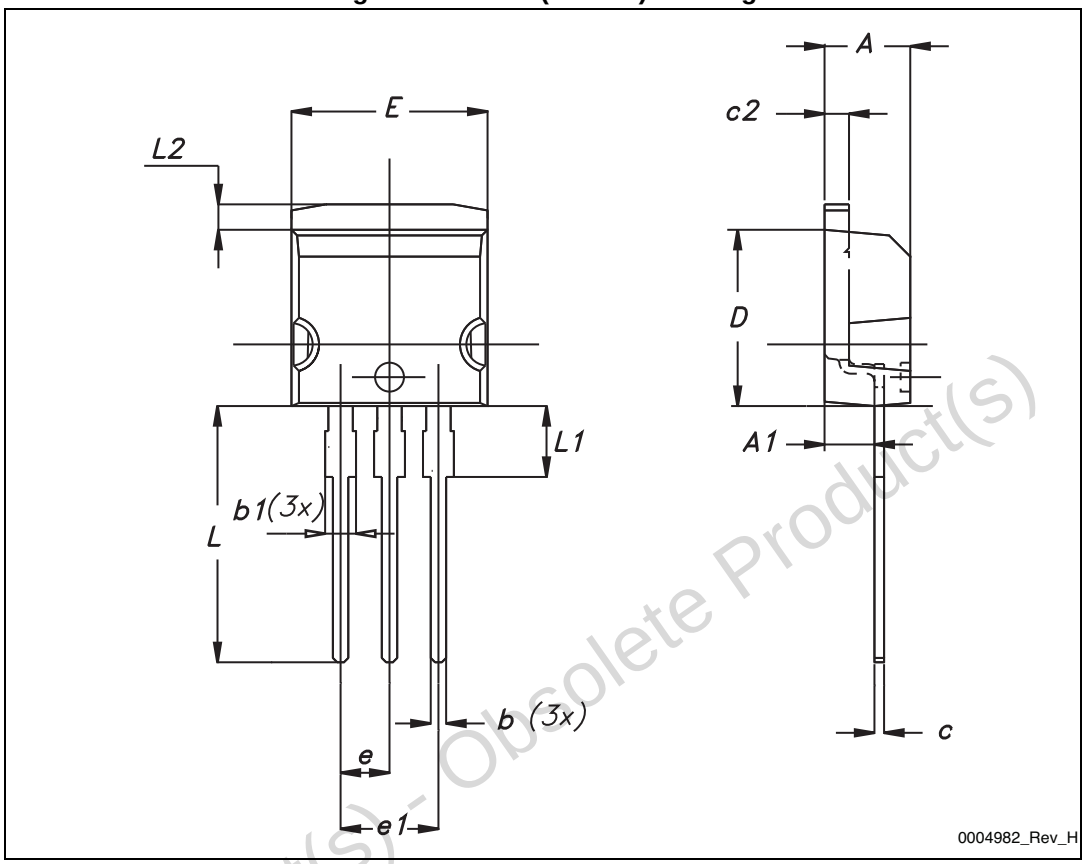


Table 9. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
23-Jul-2014	1	First release. Part number previously included in datasheet DocID15684

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