

## N-channel 600 V, 0.135 $\Omega$ typ., 20 A MDmesh™ II Power MOSFETs in a I<sup>2</sup>PAK package

Datasheet - obsolete product

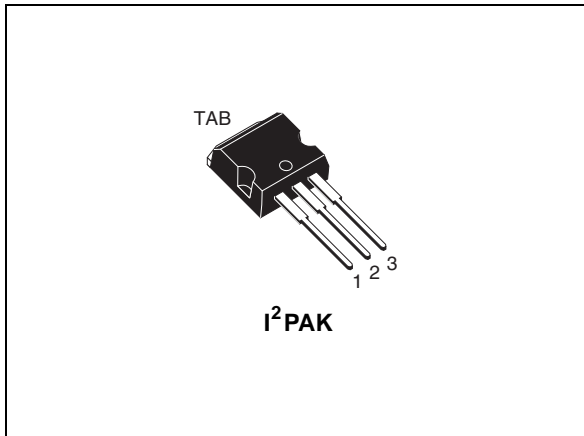
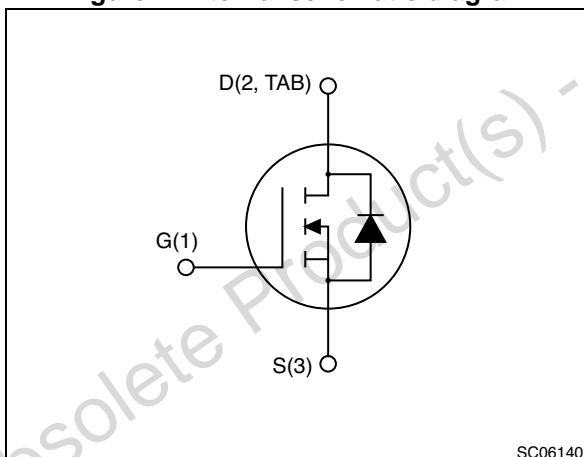


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STI26NM60N	600 V	0.165 $\Omega$	20 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STI26NM60N	26NM60N	I <sup>2</sup> PAK	Tube

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	80	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	140	W
	Derating factor	1.12	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 20\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DSpeak} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.89	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{jmax}$ )	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	610	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 600 V V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C			1 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 25 V			±0.1	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.135	0.165	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	1800	-	pF	
C <sub>oss</sub>	Output capacitance			115	-	pF	
C <sub>rss</sub>	Reverse transfer capacitance			-	1.1	-	pF
C <sub>oss eq.</sub> (1)	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 480 V	-	310	-	pF	
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10 V, (see Figure 15)	-	60	-	nC	
Q <sub>gs</sub>	Gate-source charge			-	8.5	-	nC
Q <sub>gd</sub>	Gate-drain charge			-	30	-	nC
R <sub>g</sub>	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	2.8	-	Ω	

1. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 14)	-	13	-	ns
$t_r$	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
$t_f$	Fall time		-	50	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	370		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 16)	-	5.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	31.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	450		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	7.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	32.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2.Safe operating area

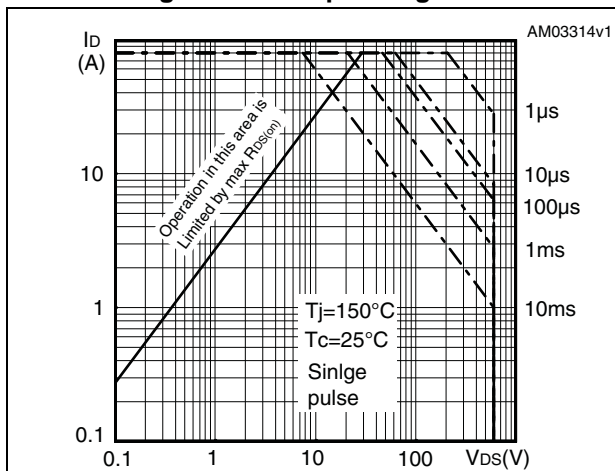


Figure 3.Thermal impedance

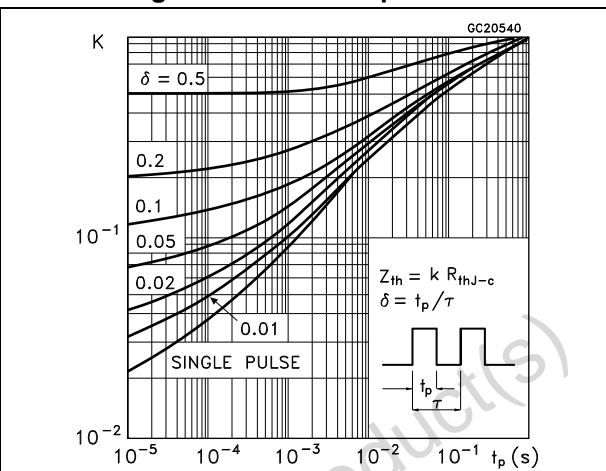


Figure 4.Output characteristics

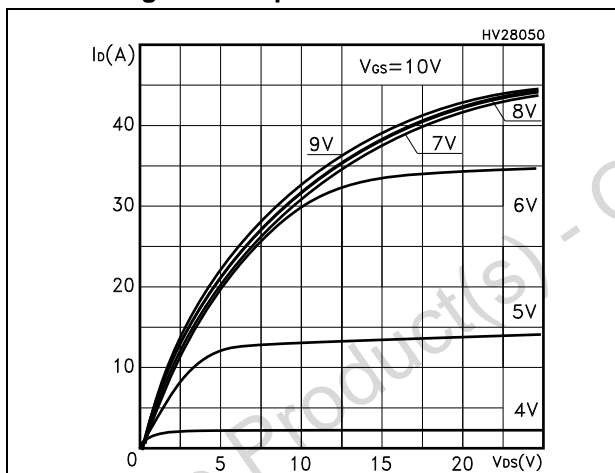


Figure 5.Transfer characteristics

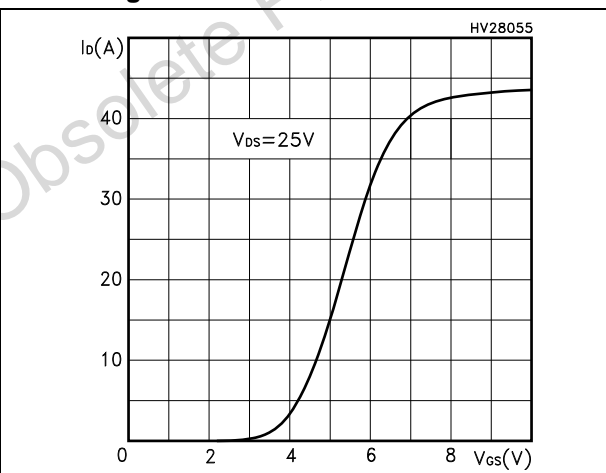


Figure 6.Transconductance

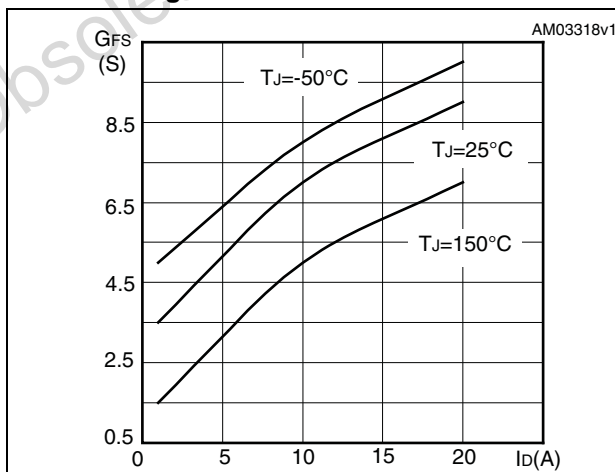


Figure 7.Static drain-source on-resistance

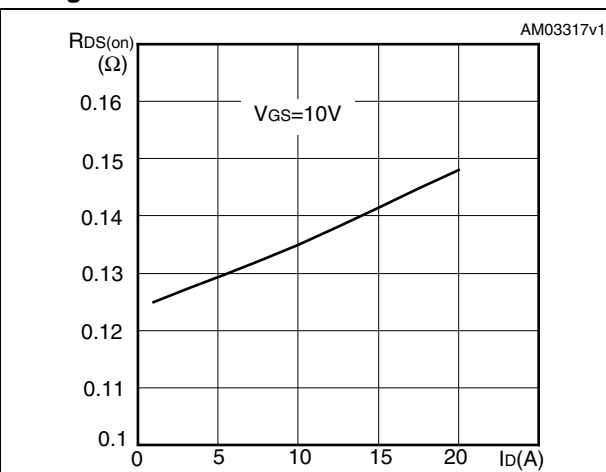


Figure 8. Gate charge vs gate-source voltage

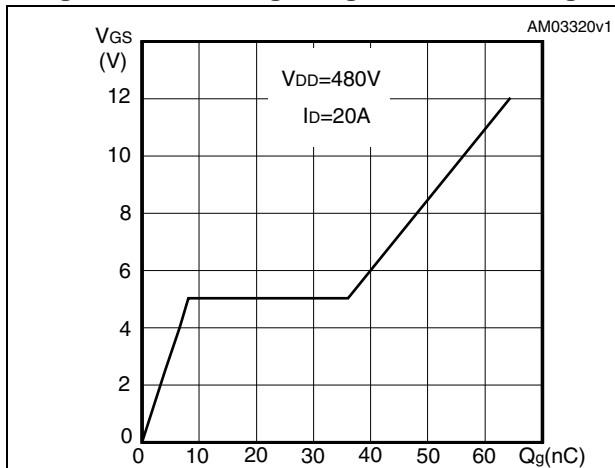


Figure 9. Capacitance variations

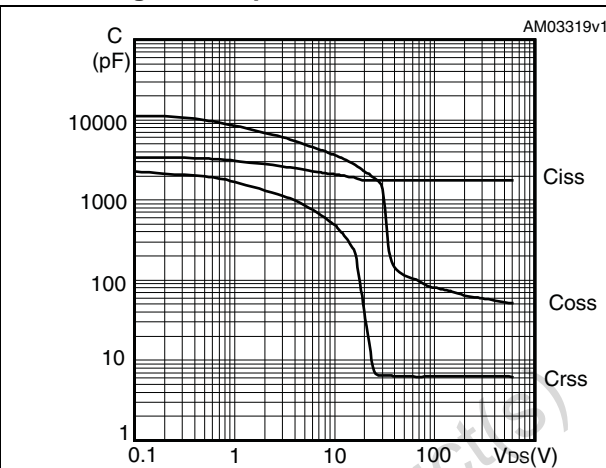


Figure 10. Normalized gate threshold voltage vs temperature

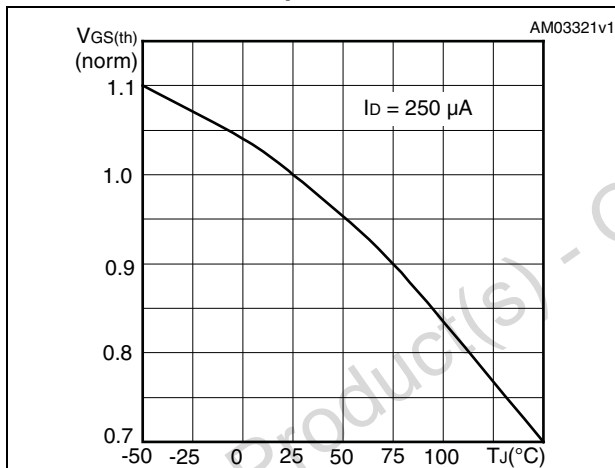


Figure 11. Normalized on resistance vs temperature

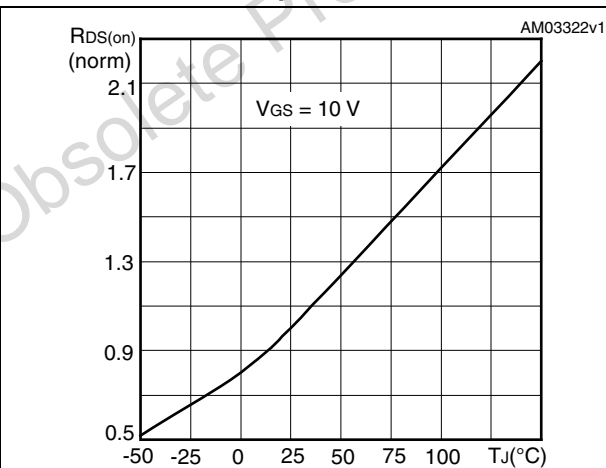


Figure 12. Source-drain diode forward characteristics

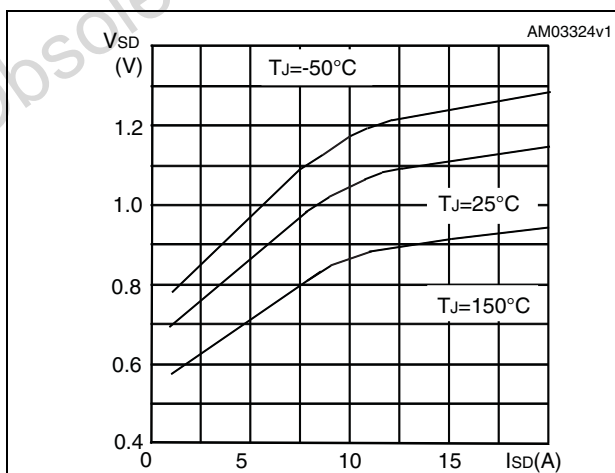
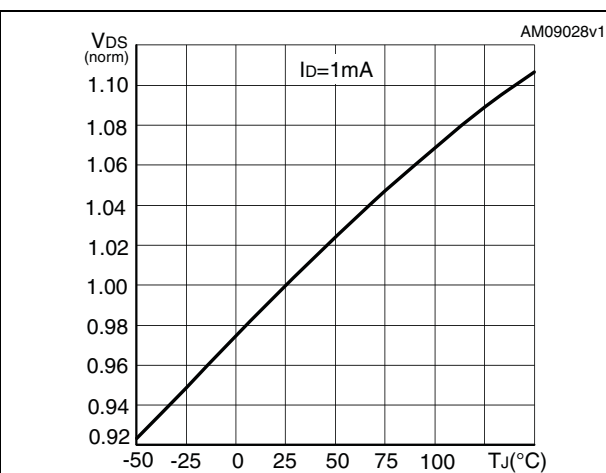


Figure 13. Normalized VDS vs temperature



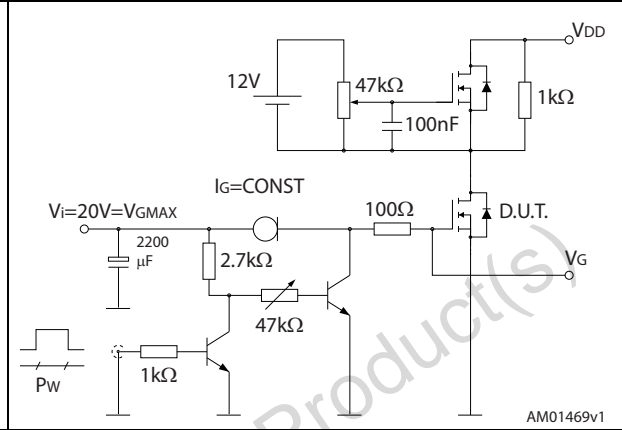
### 3 Test circuits

Figure 14. Switching times test circuit for resistive load



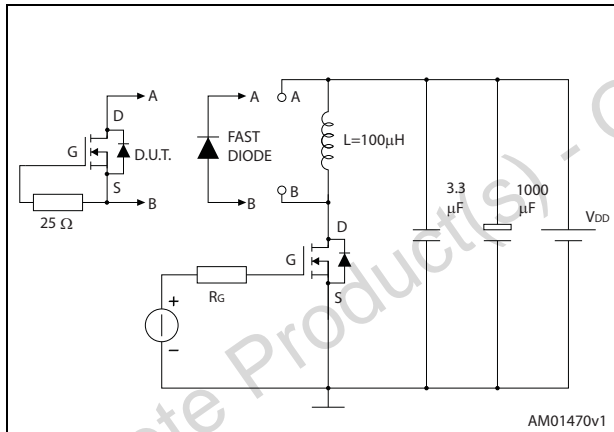
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Figure 15. Gate charge test circuit



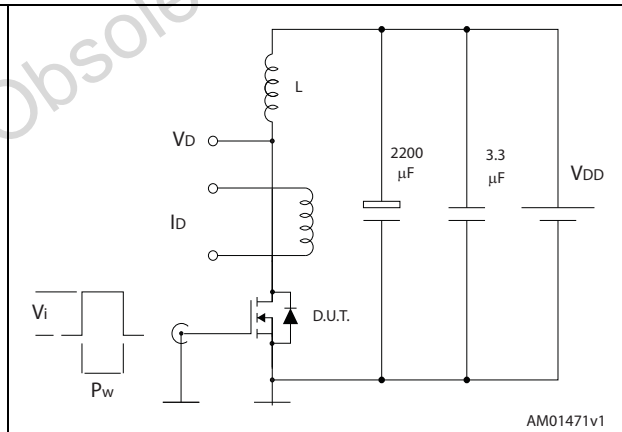
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Figure 16. Test circuit for inductive load switching and diode recovery times



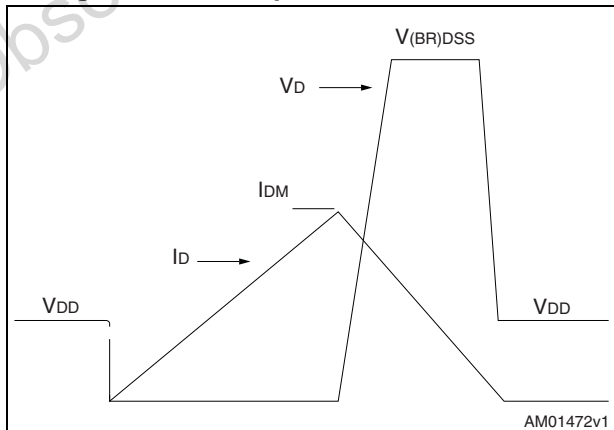
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Figure 17. Unclamped inductive load test circuit



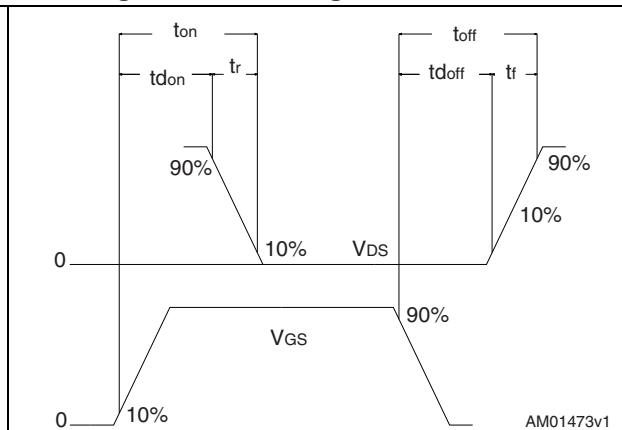
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



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## 4 Package mechanical data

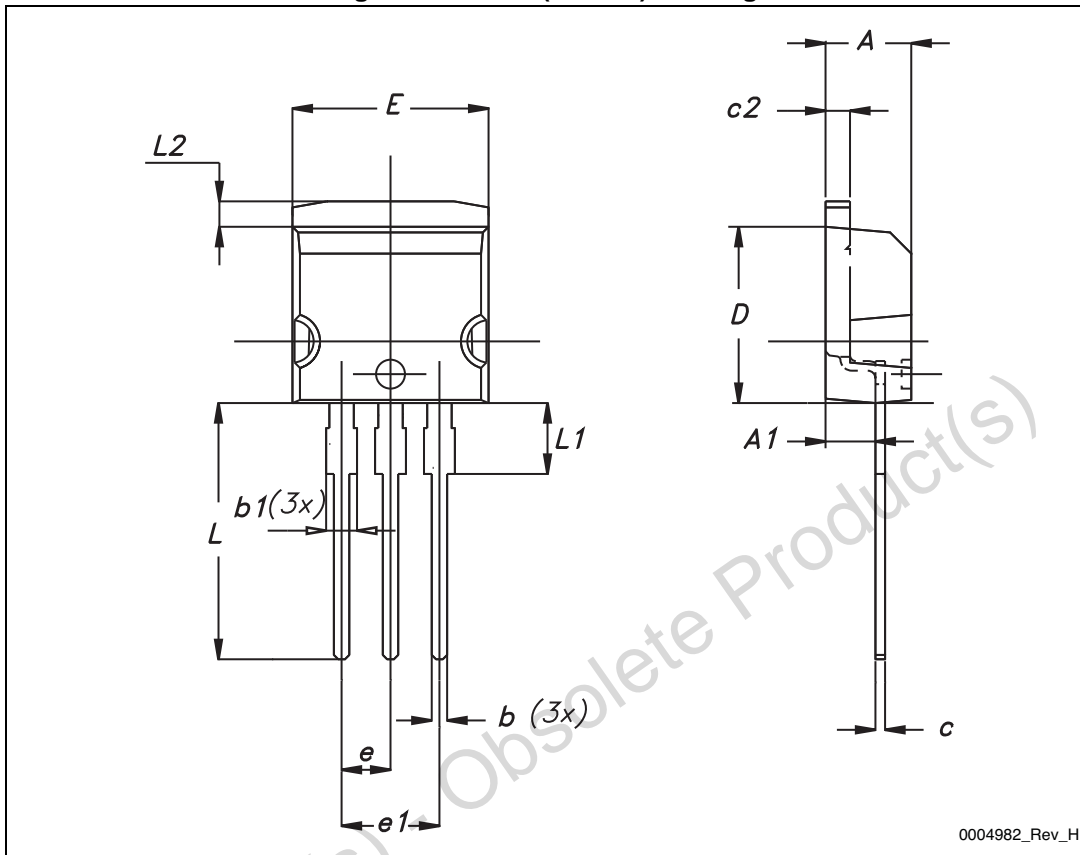
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Table 9. I<sup>2</sup>PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 20. I<sup>2</sup>PAK (TO-262) drawing



0004982\_Rev\_H

## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Sep-2013	1	First release. Part numbers previously included in datasheet DocID15642

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