

N-channel 80 V, 5.6 mΩ typ., 110 A STripFET™ F7 Power MOSFET in a H²PAK-2 package

Datasheet - target specification

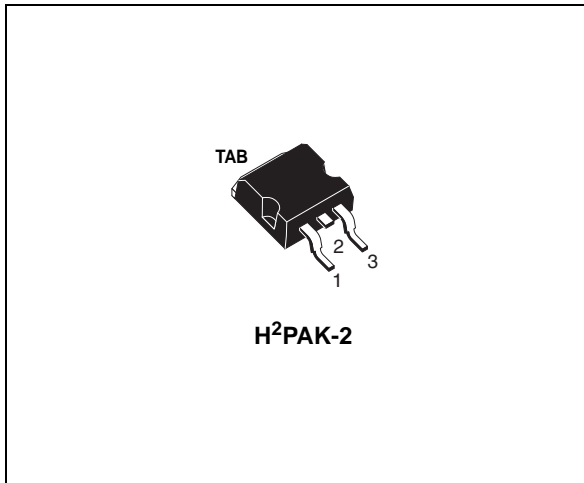
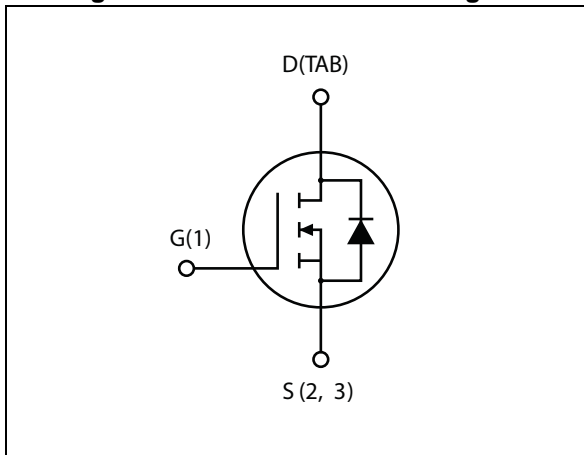


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STH110N8F7-2	80 V	6.6 mΩ	110 A	170 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STH110N8F7-2	110N8F7	H ² PAK-2	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	110	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(1)}$	Drain current (pulsed)	440	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	170	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	TBD	mJ
T_j	Operating junction temperature	- 55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. Pulse width is limited by safe operating area

2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_d = 18.5\text{ A}$, $V_{dd} = 50\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case	0.88	$^\circ\text{C/W}$

1. When mounted on a 1 inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu A$	80			V
I_{DSS}	Zero gate voltage Drain current	$V_{GS} = 0, V_{DS} = 80\ V$			1	μA
		$V_{GS} = 0, V_{DS} = 80\ V,$ $T_J = 125\text{ °C}$			10	μA
I_{GSS}	Gate-source leakage current	$V_{DS} = 0, V_{GS} = \pm 20\ V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ V, I_D = 55\ A$		5.6	6.6	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 25\ V,$ $f = 1\ MHz$	-	3200	-	pF
C_{oss}	Output capacitance		-	800	-	pF
C_{riss}	Reverse transfer capacitance		-	55	-	pF
Q_g	Total gate charge	$V_{DD} = 40\ V, I_D = 110\ A,$ $V_{GS} = 10\ V$	-	45	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 40\ V, I_D = 55\ A$ $R_G = 4.7\ \Omega, V_{GS} = 10\ V$	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off-delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 110 \text{ A}$	-		TBD	V
t_{rr}	Reverse recovery time	$I_{SD} = 110 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 60 \text{ V}$ $T_j = 25 \text{ }^\circ\text{C}$	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

1. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

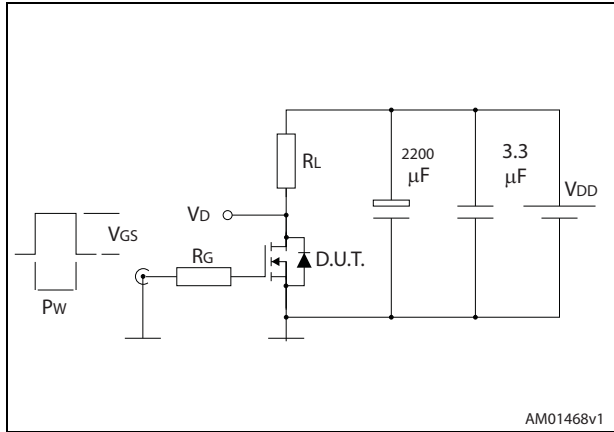


Figure 3. Gate charge test circuit

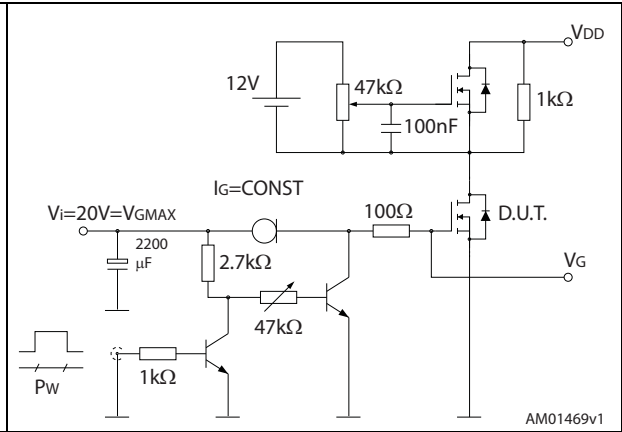


Figure 4. Test circuit for inductive load switching and diode recovery times

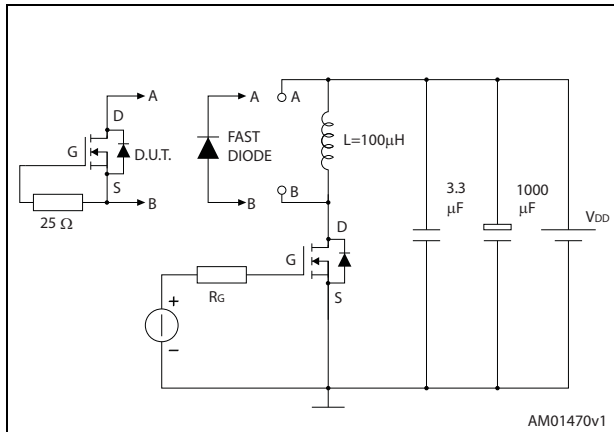


Figure 5. Unclamped inductive load test circuit

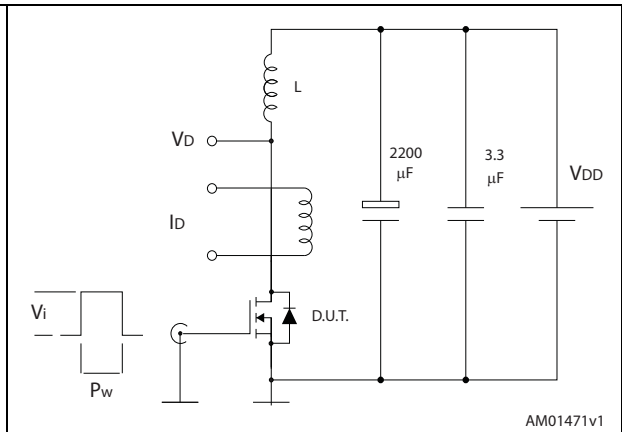


Figure 6. Unclamped inductive waveform

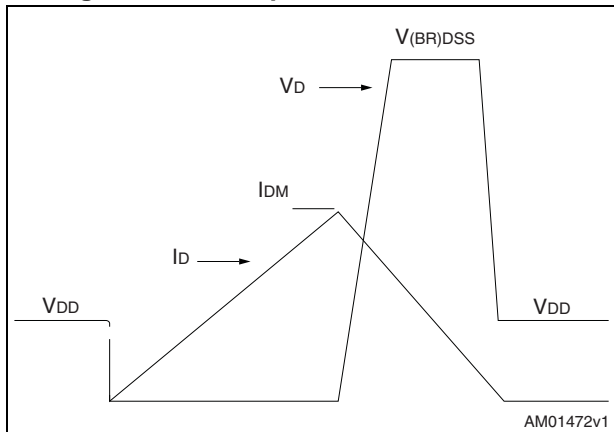
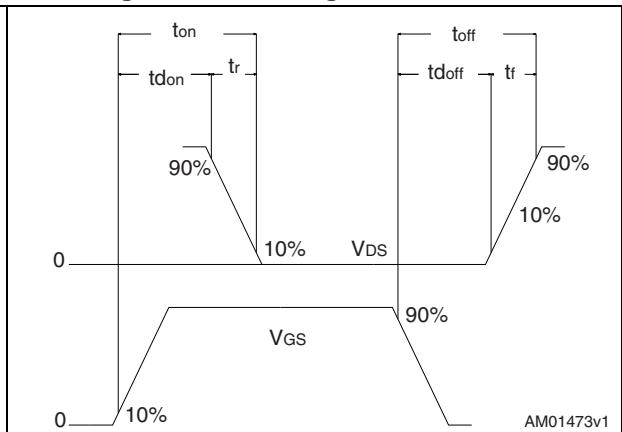


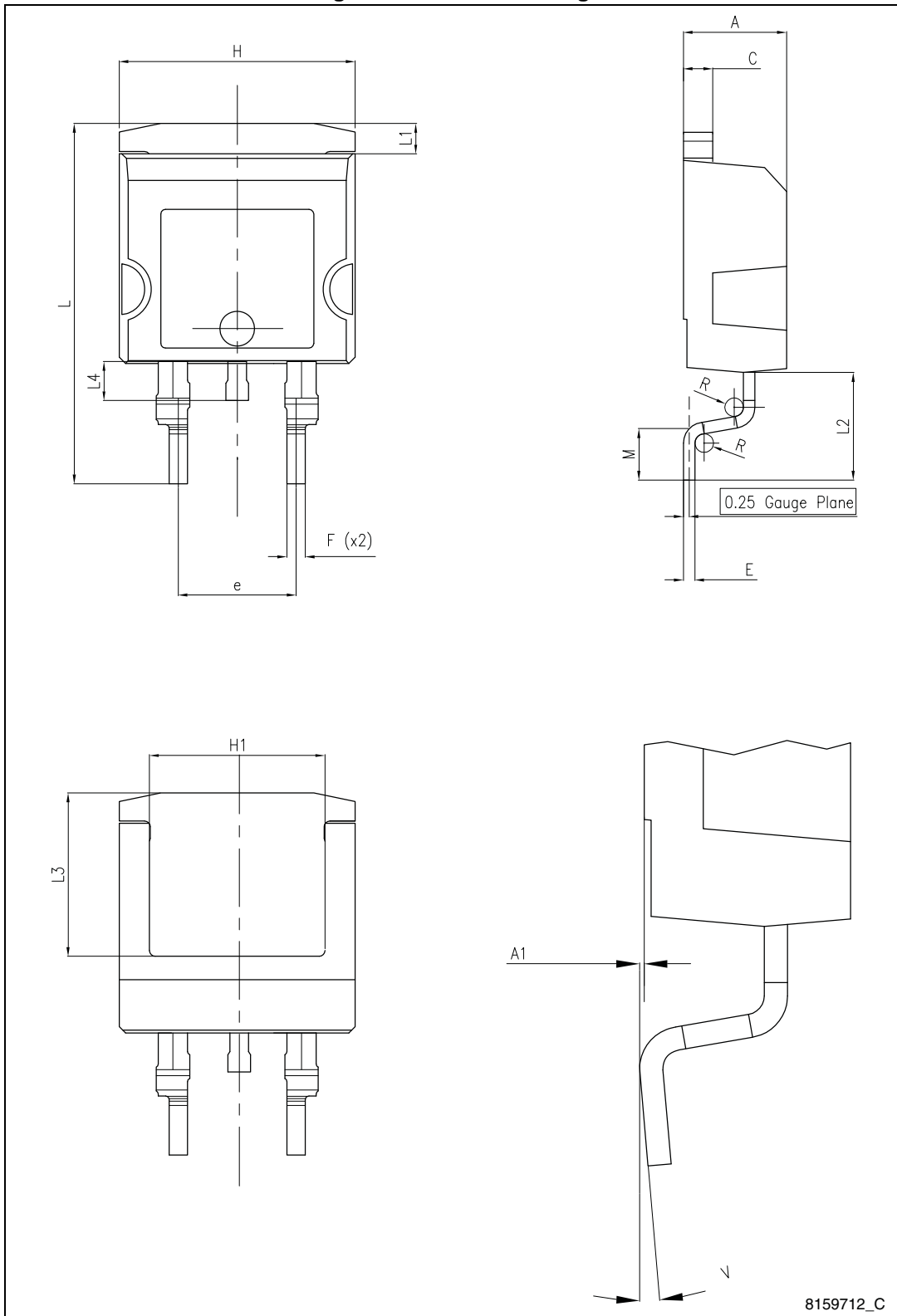
Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 8. H²PAK-2 drawing

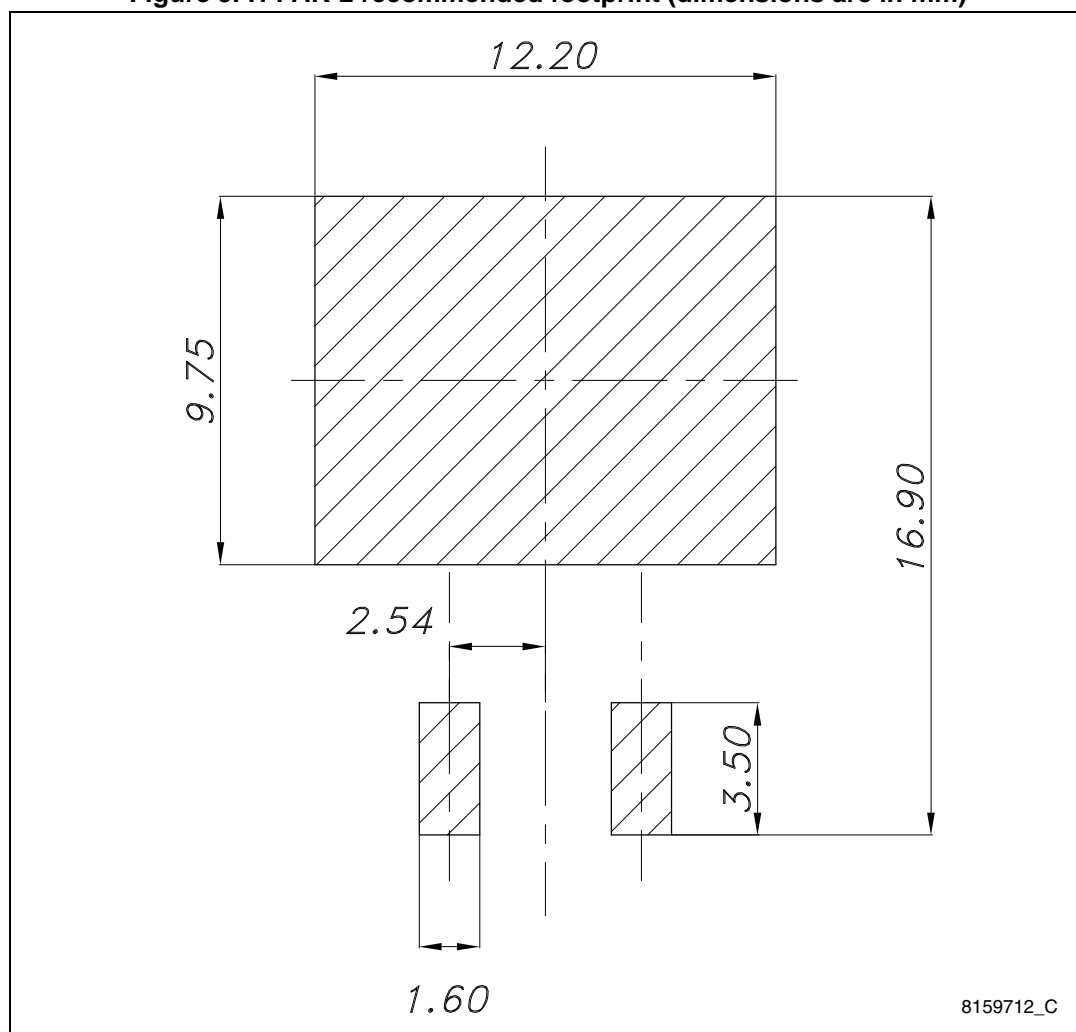


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Table 8. H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 9. H²PAK-2 recommended footprint (dimensions are in mm)



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5 Packaging mechanical data

Figure 10. Tape dimension

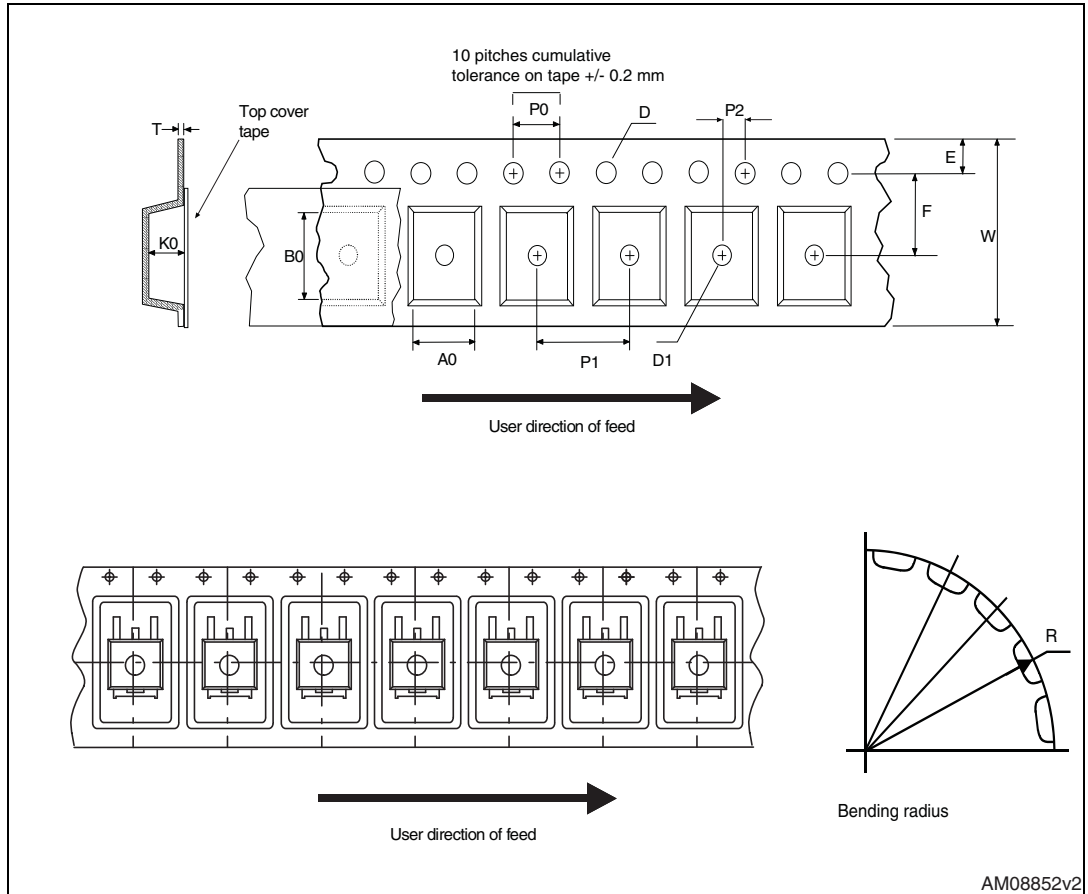
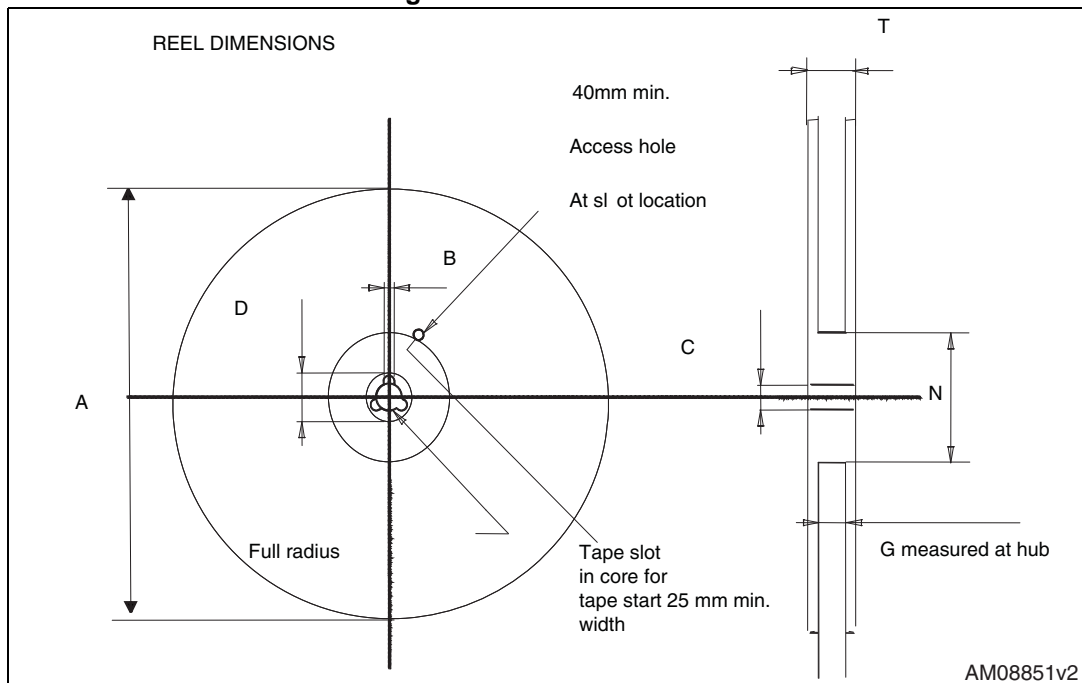


Table 9. H²PAK-2 tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 11. Reel dimension



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Nov-2014	1	First release.

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