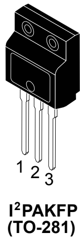
life.augmented

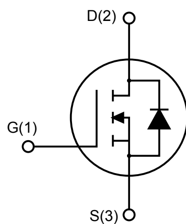
STFI31N65M5

Datasheet

N-channel 650 V, 0.124 Ω, 22 A, MDmesh M5 Power MOSFET in an I²PAKFP package



I²PAKFP (TO-281)



Product status link
STFI32N65M5

Product summary	
Order code	STFI31N65M5
Marking	31N65M5
Package	I^2PAKFP
Packing	Tube

Features

Order code	V_{DS} @ T_{JMAX}	$R_{DS(on)}$ max	I_D
STFI31N65M5	710 V	0.148 Ω	22 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	22 [1]	A
I_D	Drain current (continuous) at T_C = 100 °C	13.9 [1]	A
I_{DM} [2]	Drain current (pulsed)	88 [1]	A
P_{TOT}	Total power dissipation at T_C = 25 °C	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T_C = 25 °C)	2500	V
dv/dt [3]	Peak diode recovery voltage slope	15	V/ns
dv/dt [4]	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Limited by package.*
2. *Limited by maximum junction temperature.*
3. *I_{SD} ≤ 22 A, di/dt ≤ 400 A/µs; V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} ≤ 480 V.*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	4.17	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	410	mJ

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C [(1)]			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 11 A		0.124	0.148	Ω

1. *Defined by design, not subject to production test.*

Obsolete Product(s) - Obsolete Product(s)

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1865	-	pF
C_{oss}	Output capacitance		-	45	-	pF
C_{rss}	Reverse transfer capacitance		-	4.2	-	pF
$C_{o(tr)}$ [(1)]	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	146	-	pF
$C_{o(er)}$ [(2)]	Equivalent capacitance energy related		-	43	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz	-	2.8	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 11 A V_{GS}= 0 to 10 V (see Figure 16. Test circuit for gate charge behavior)	-	45	-	nC
Q_{gs}	Gate-source charge		-	11.5	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC

1. *$C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD}= 400 V, I_D = 14 A, R_G = 4.7 Ω V_{GS} = 10 V (see Figure 17. Test circuit for inductive load switching and diode recovery times and Figure 20. Switching time waveform)	-	46	-	ns
$t_{r(v)}$	Voltage rise time		-	8	-	ns
$t_{f(i)}$	Current fall time		-	8.5	-	ns
$t_{c(off)}$	Crossing time		-	11	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
I_{SDM} (1)	Source-drain current (pulsed)		-		88	A
V_{SD} (2)	Forward on voltage	I_{SD} = 22 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 22 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	336		ns
Q_{rr}	Reverse recovery charge		-	5		µC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 22 A, di/dt = 100 A/µs, V_{DD}= 100 V, T_j= 150 °C (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	406		ns
Q_{rr}	Reverse recovery charge		-	6		µC
I_{RRM}	Reverse recovery current		-	31		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

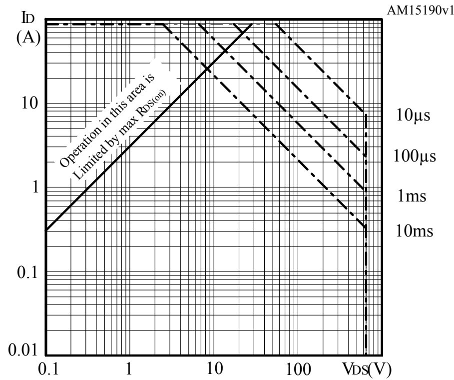


Figure 2. Thermal impedance

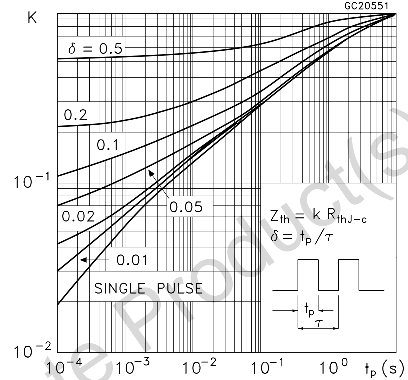


Figure 3. Output characteristics

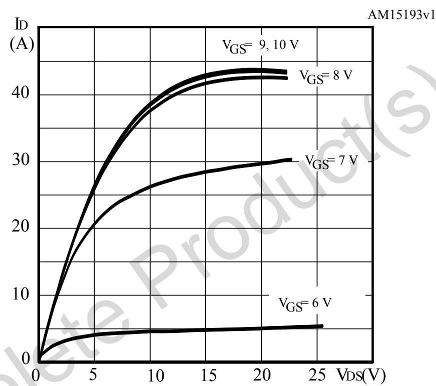


Figure 4. Transfer characteristics

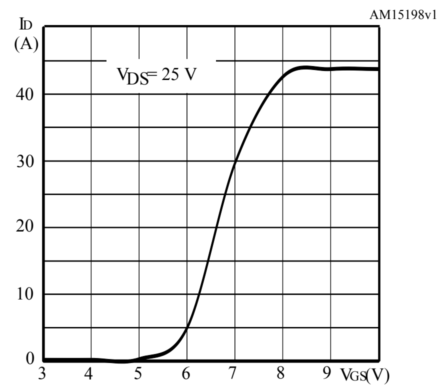


Figure 5. Gate charge vs gate-source voltage

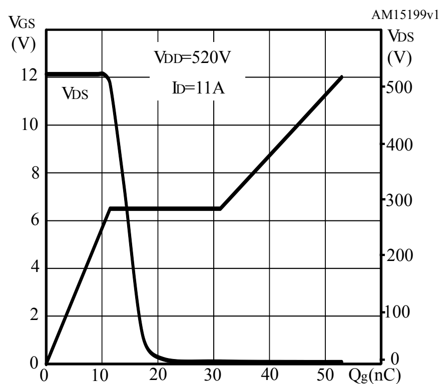
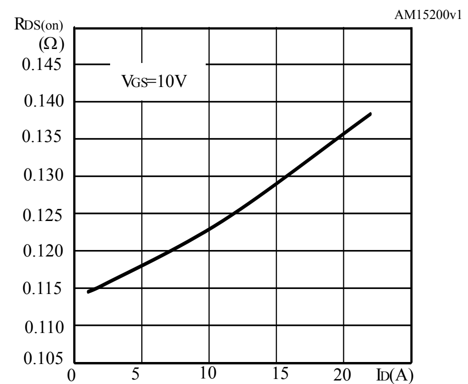


Figure 6. Static drain-source on-resistance



Obsolete Product(s) - Obsolete Product(s)

Figure 7. Capacitance variations

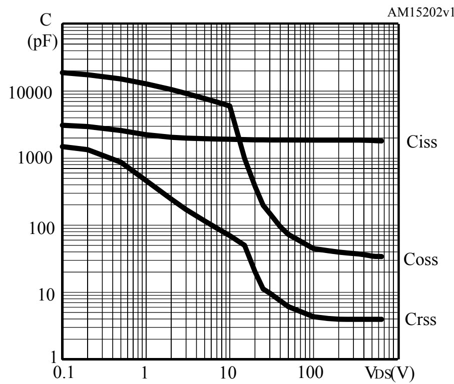


Figure 8. Output capacitance stored energy

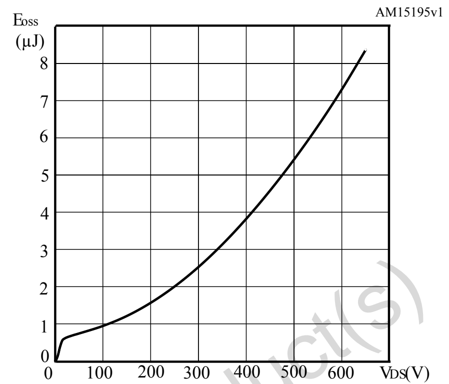


Figure 9. Normalized gate threshold voltage vs temperature

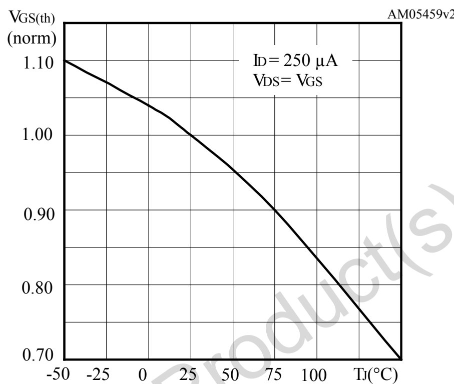


Figure 10. Normalized on-resistance vs temperature

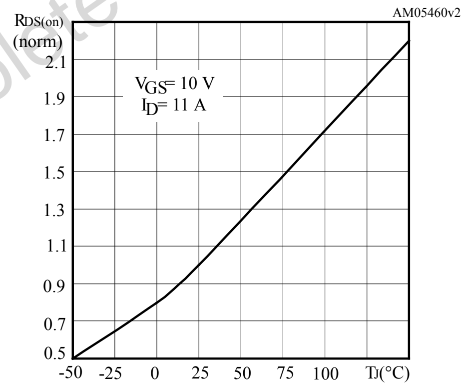


Figure 11. Source-drain diode forward characteristics

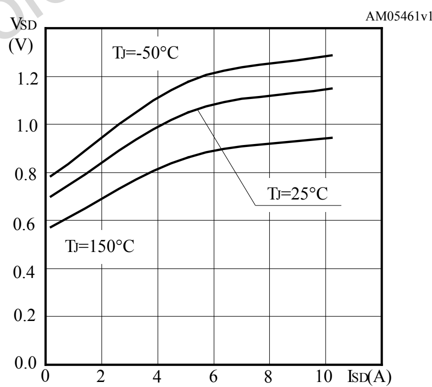
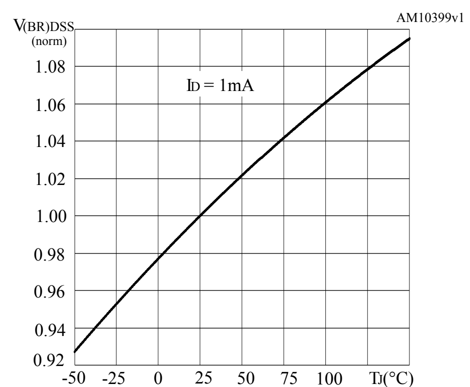
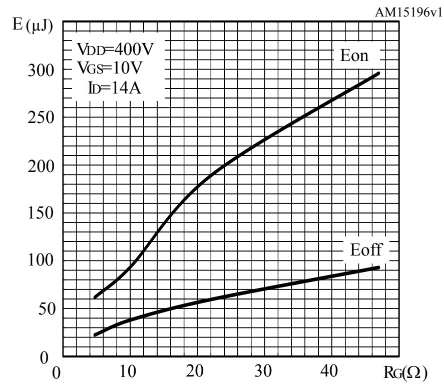


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



Obsolete Product(s) - Obsolete Product(s)

Figure 13. Switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

Obsolete Product(s) - Obsolete Product(s)

3 Test circuits

Figure 15. Test circuit for resistive load switching times

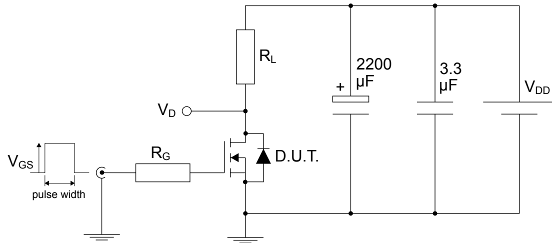
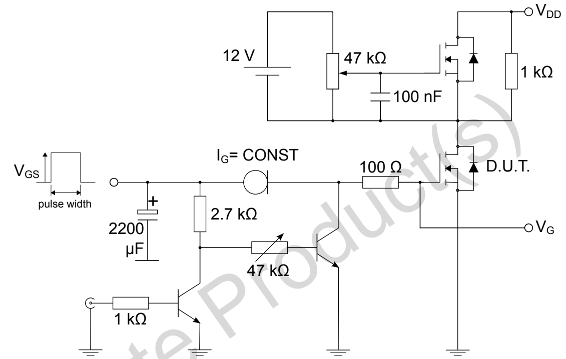


Figure 16. Test circuit for gate charge behavior



Obsolete Product(s) - Obsolete Product(s)

Figure 17. Test circuit for inductive load switching and diode recovery times

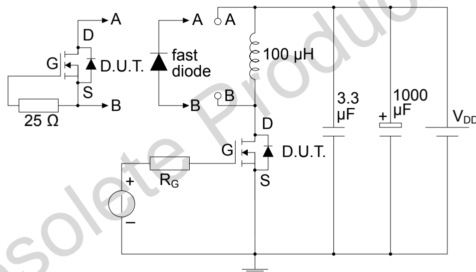


Figure 18. Unclamped inductive load test circuit

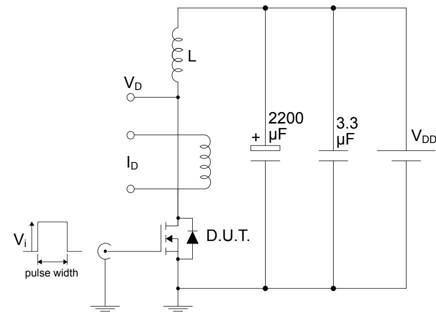


Figure 19. Unclamped inductive waveform

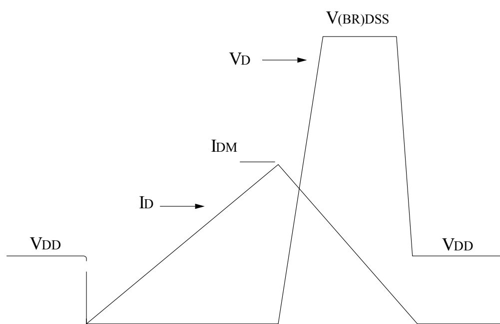
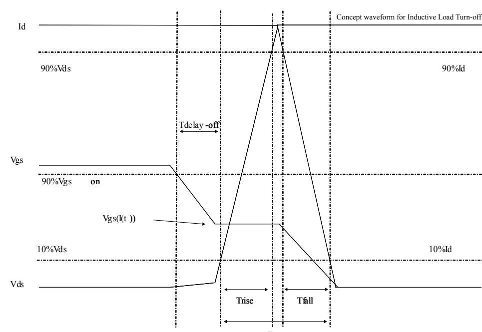


Figure 20. Switching time waveform

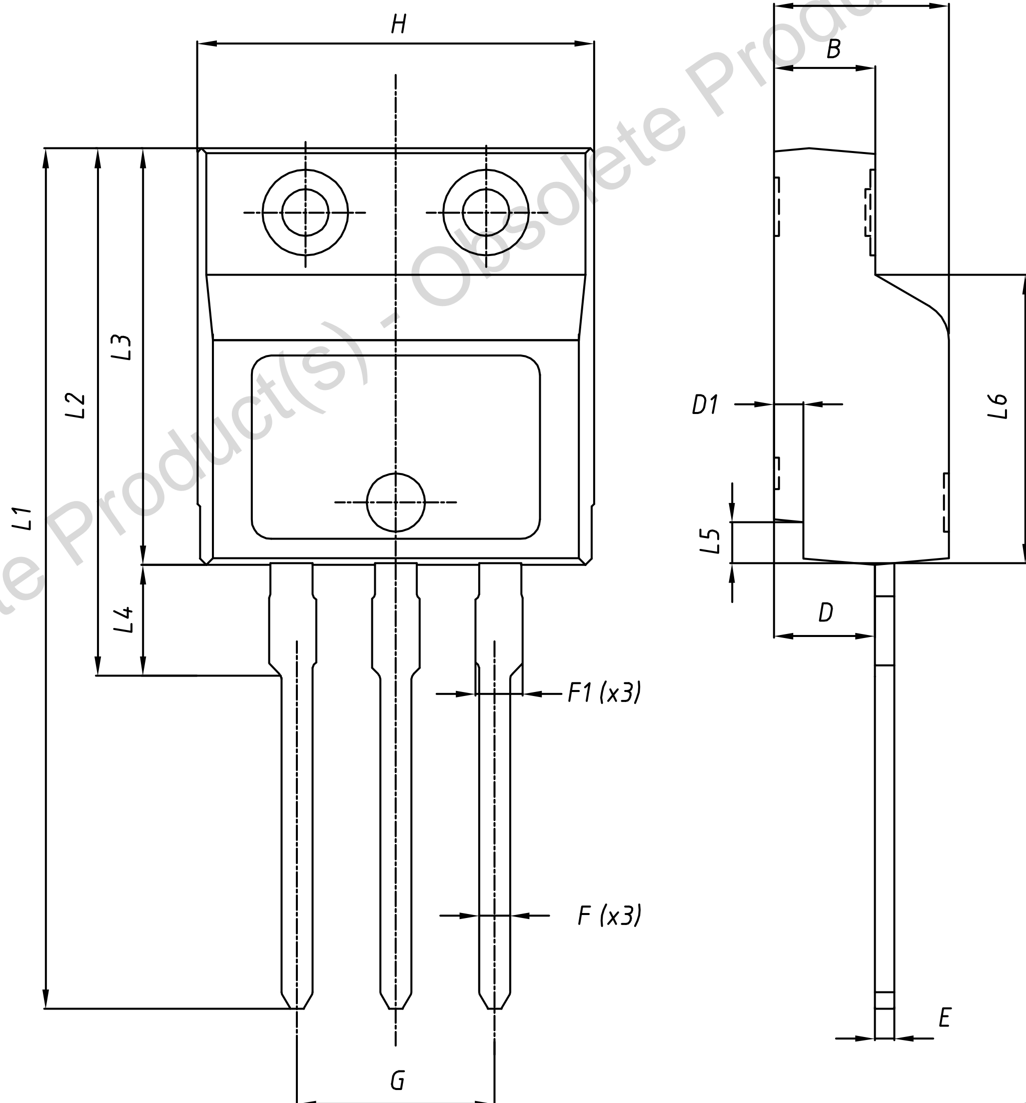


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 I²PAKFP (TO-281) package information

Figure 21. I²PAKFP (TO-281) package outline



Obsolete Product(s) - Obsolete Product(s)

Table 8. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

Obsolete Product(s) - Obsolete Product(s)

Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Apr-2019	1	First release. Part number previously included in datasheet DocID022848.

Obsolete Product(s) - Obsolete Product(s)

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved

Obsolete Product(s) - Obsolete Product(s)