# STB140N4F6

## N-channel 40 V, 3.5 mΩ typ., 80 A STripFET™ F6 Power MOSFET in a D²PAK package

Datasheet - preliminary data

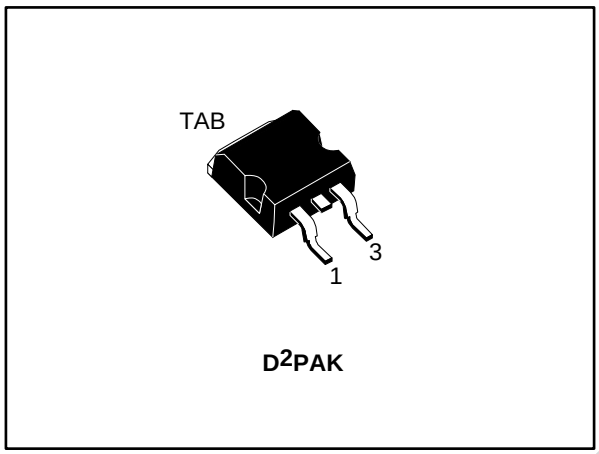
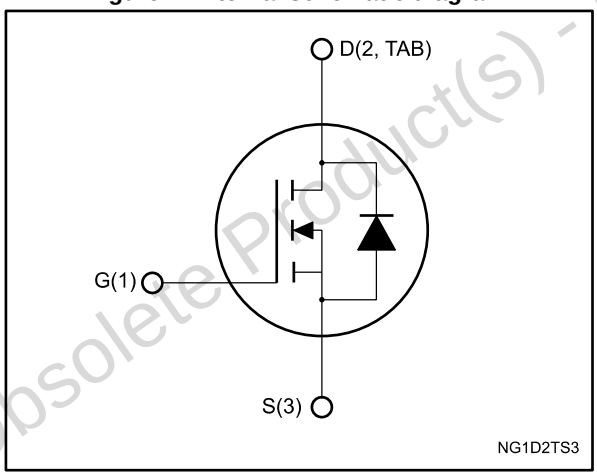



**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STB140N4F6 | 40 V | 4.0 mΩ | 80 A | 168 W |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

## Applications

- Switching applications
- Power tools

## Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.



**Table 1: Device summary**

| Order code | Marking | Package | Packing |
|---|---|---|---|
| STB140N4F6 | 140N4F6 | D²PAK | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 40 | V |
| $V_{GS}$ | Gate-source voltage | ±20 | V |
| $I_D$ (1) | Drain current (continuous) at $T_{case}$ = 25 °C | 80 | A |
| | Drain current (continuous) at $T_{case}$ = 100 °C | 80 | |
| $I_{DM}$ (2) | Drain current (pulsed) | 320 | A |
| $P_{TOT}$ | Total dissipation at $T_{case}$ = 25 °C | 168 | W |
| $T_{stg}$ | Storage temperature | -55 to 175 | °C |
| $T_j$ | Operating junction temperature | | |

**Notes:**

(1) Limited by package

(2) Pulse width is limited by safe operating area.

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.89 | °C/W |
| $R_{thj\text{-}pcb}$ | Thermal resistance junction-pcb | 35 | |

**Table 4: Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ (1) | Avalanche current, repetitive or not repetitive | 40 | A |
| $E_{AS}$ (2) | Single pulse avalanche energy | 240 | mJ |

**Notes:**

(1) Pulse width limited by $T_{jmax}$.

(2) starting $T_j$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 25 V.

# 2 Electrical characteristics

($T_{case}$ = 25 °C unless otherwise specified)

**Table 5: Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 40 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V, $T_{case}$ = 125 °C | | | 10 | |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 40 A | | 3.5 | 4.0 | mΩ |

**Table 6: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 4260 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 635 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 310 | - | |
| $Q_g$ | Total gate charge | $V_{DD}$ = 20 V, $I_D$ = 80 A, $V_{GS}$ = 10 V (see *Figure 14: "Gate charge test circuit"*) | - | 70 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 20 | - | |
| $Q_{gd}$ | Gate-drain charge | | - | 18 | - | |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 1.3 | - | Ω |

**Table 7: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 20 V, $I_D$ = 40 A $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 13: "Switching times test circuit for resistive load"* and *Figure 18: "Switching time waveform"*) | - | 20 | - | ns |
| $t_r$ | Rise time | | - | 63 | - | |
| $t_{d(off)}$ | Turn-off delay time | | - | 58 | - | |
| $t_f$ | Fall time | | - | 20 | - | |

**Table 8: Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 80 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 320 | A |
| $V_{SD}$ (2) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 40 A | - | | 1.3 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 80 A, di/dt = 100 A/µs, $V_{DD}$ = 30 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*) | - | 41 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 58 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 2.8 | | A |

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

**Figure 2: Safe operating area**

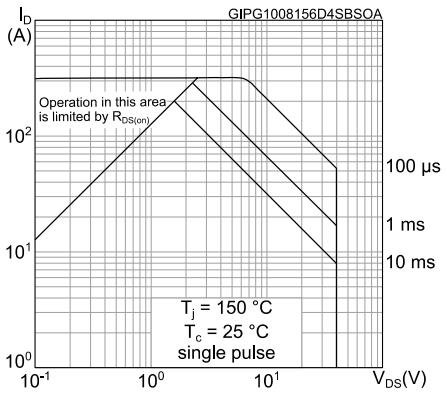



**Figure 3: Thermal impedance**

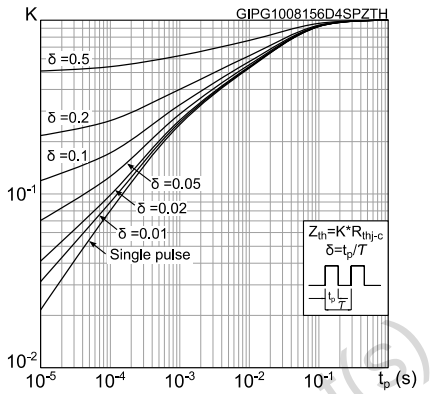



**Figure 4: Output characteristics**

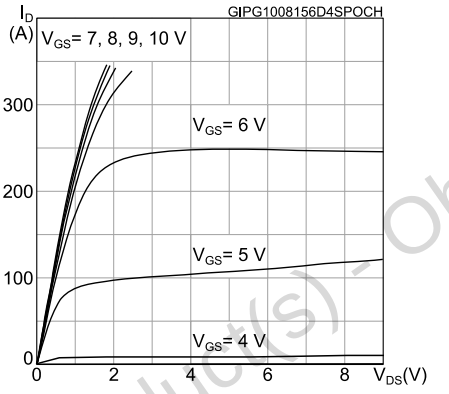



**Figure 5: Transfer characteristics**

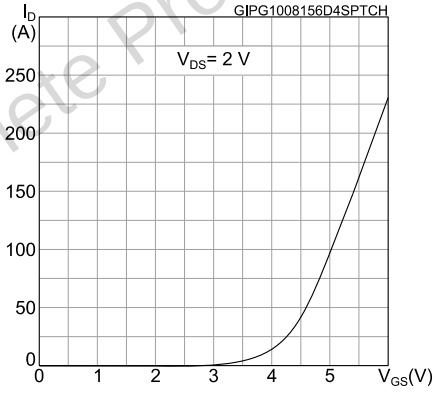



**Figure 6: Gate charge vs gate-source voltage**

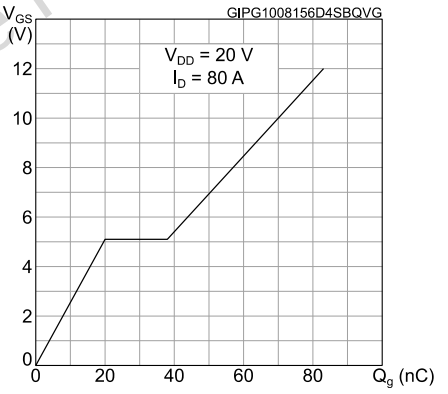



**Figure 7: Static drain-source on-resistance**

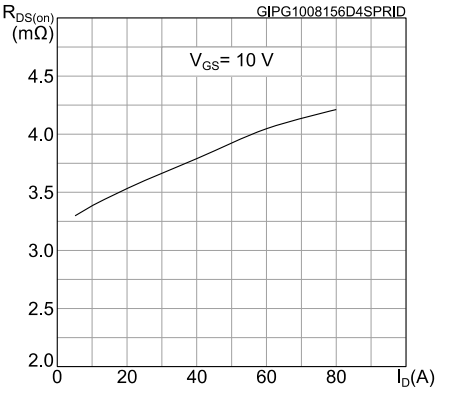


**Figure 8: Capacitance variations**

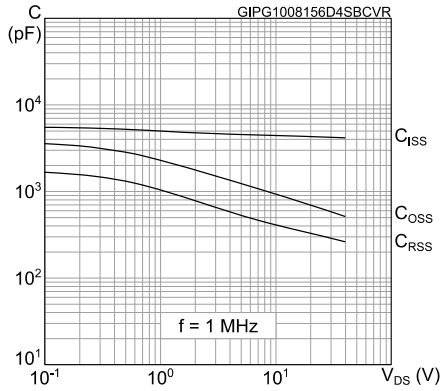



**Figure 9: Normalized gate threshold voltage vs temperature**

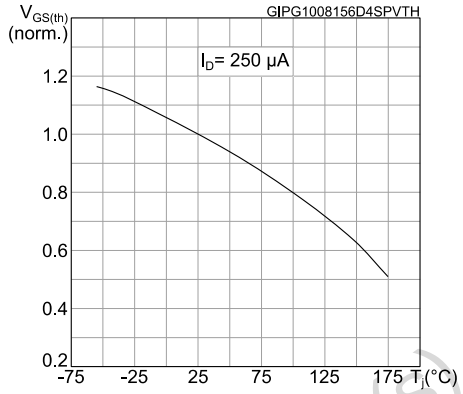



**Figure 10: Normalized on-resistance vs temperature**

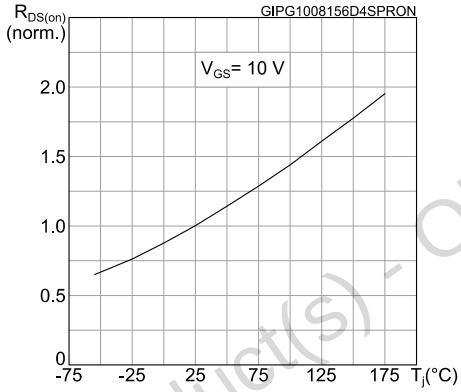



**Figure 11: Normalized V(BR)DSS vs temperature**

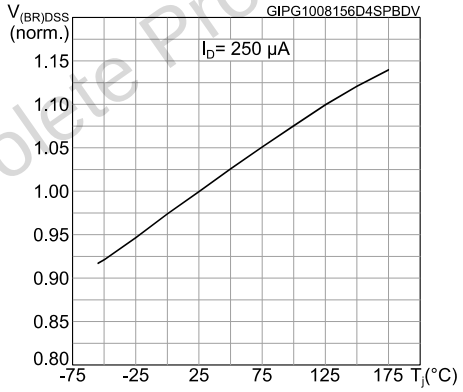
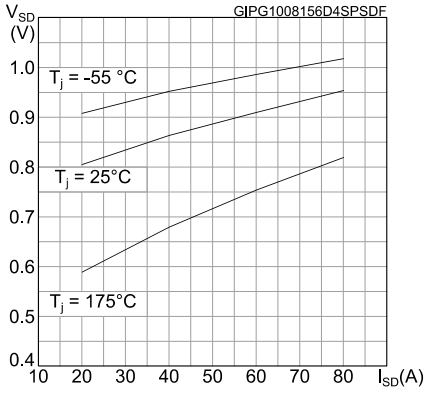



**Figure 12: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13: Switching times test circuit for resistive load**

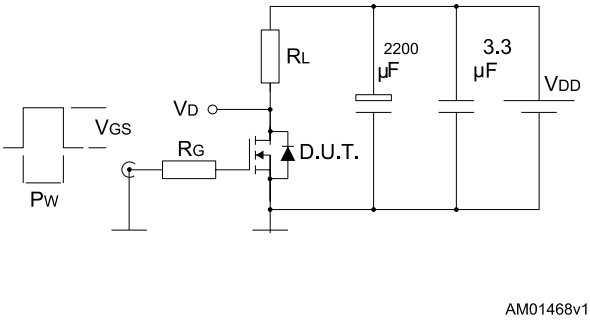



**Figure 14: Gate charge test circuit**

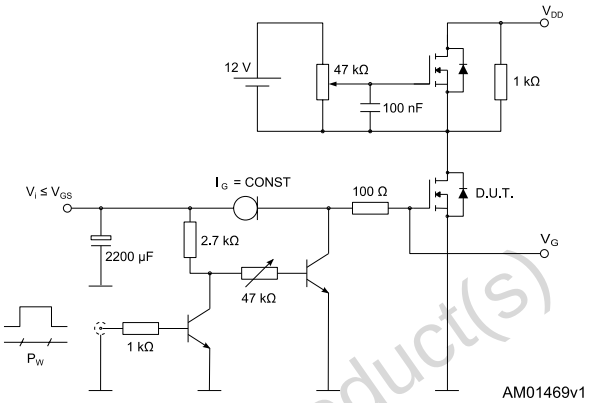



**Figure 15: Test circuit for inductive load switching and diode recovery times**

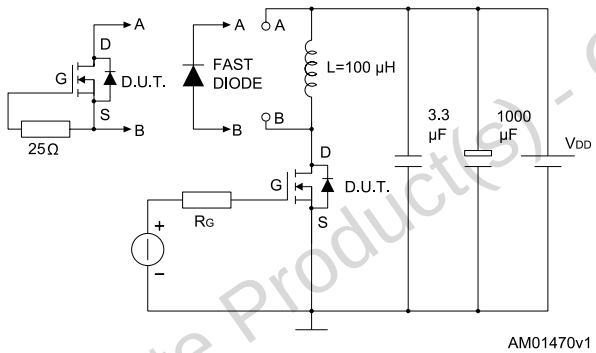



**Figure 16: Unclamped inductive load test circuit**

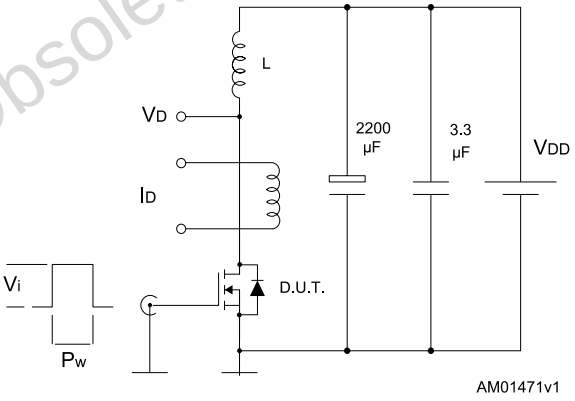



**Figure 17: Unclamped inductive waveform**

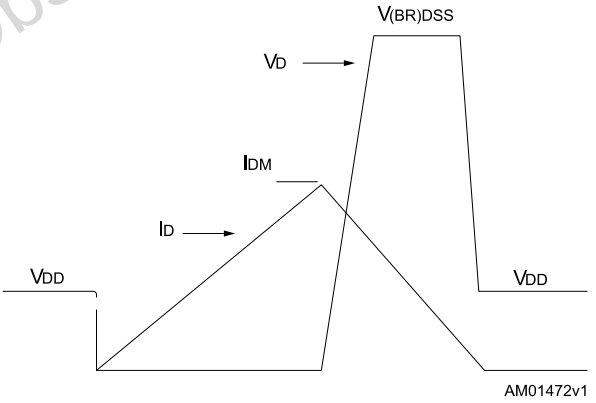
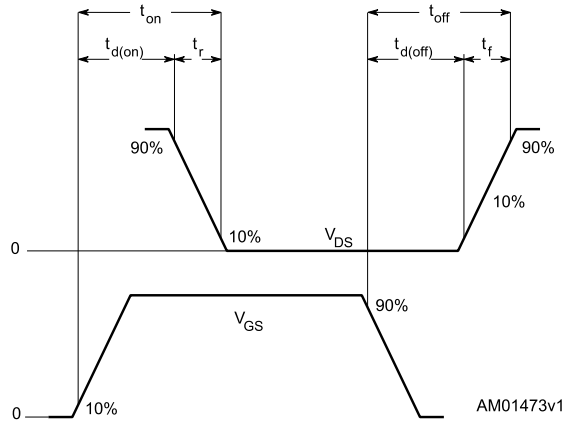



**Figure 18: Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 D²PAK (TO-263) type A package information

**Figure 19: D²PAK (TO-263) type A package outline**

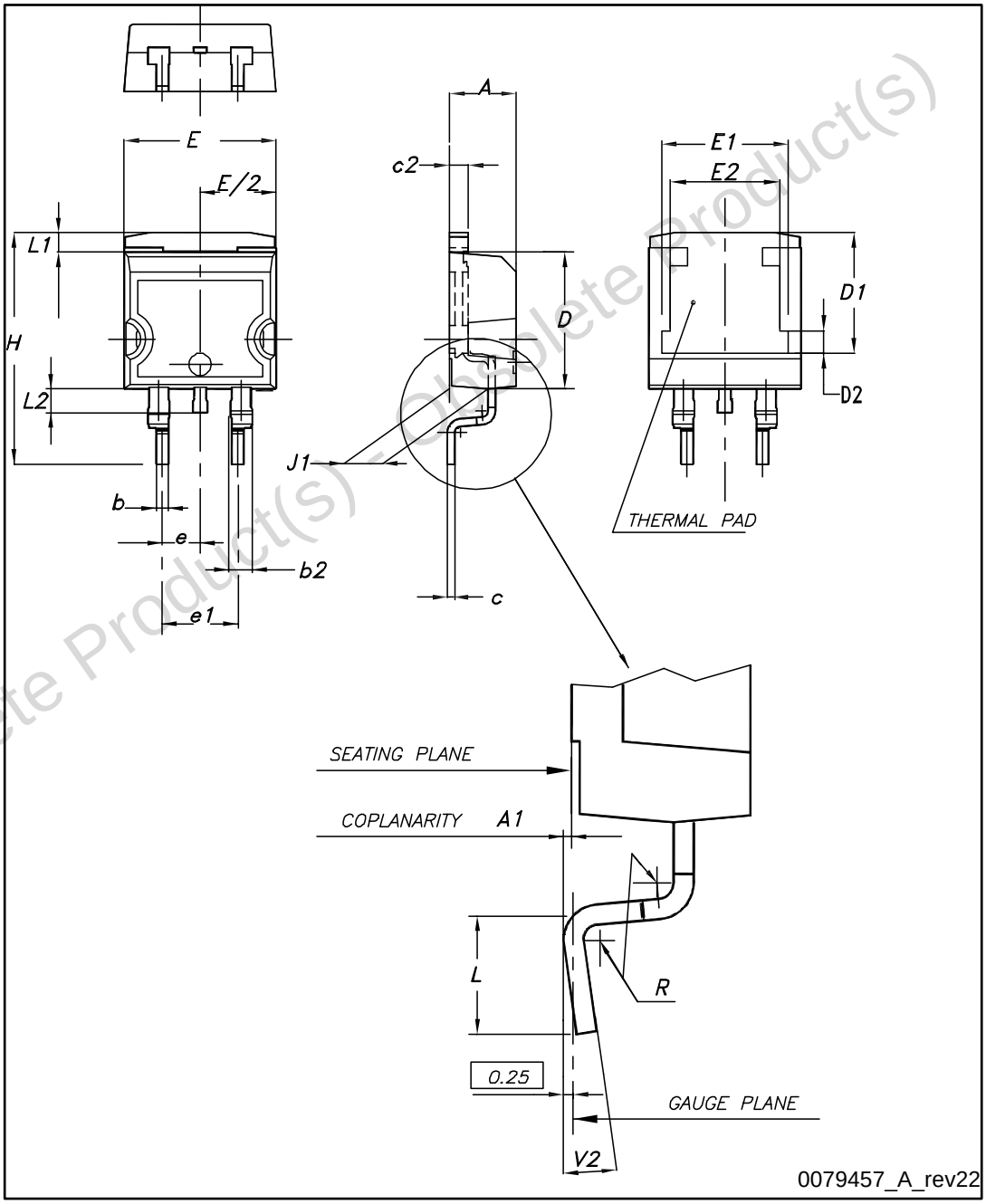
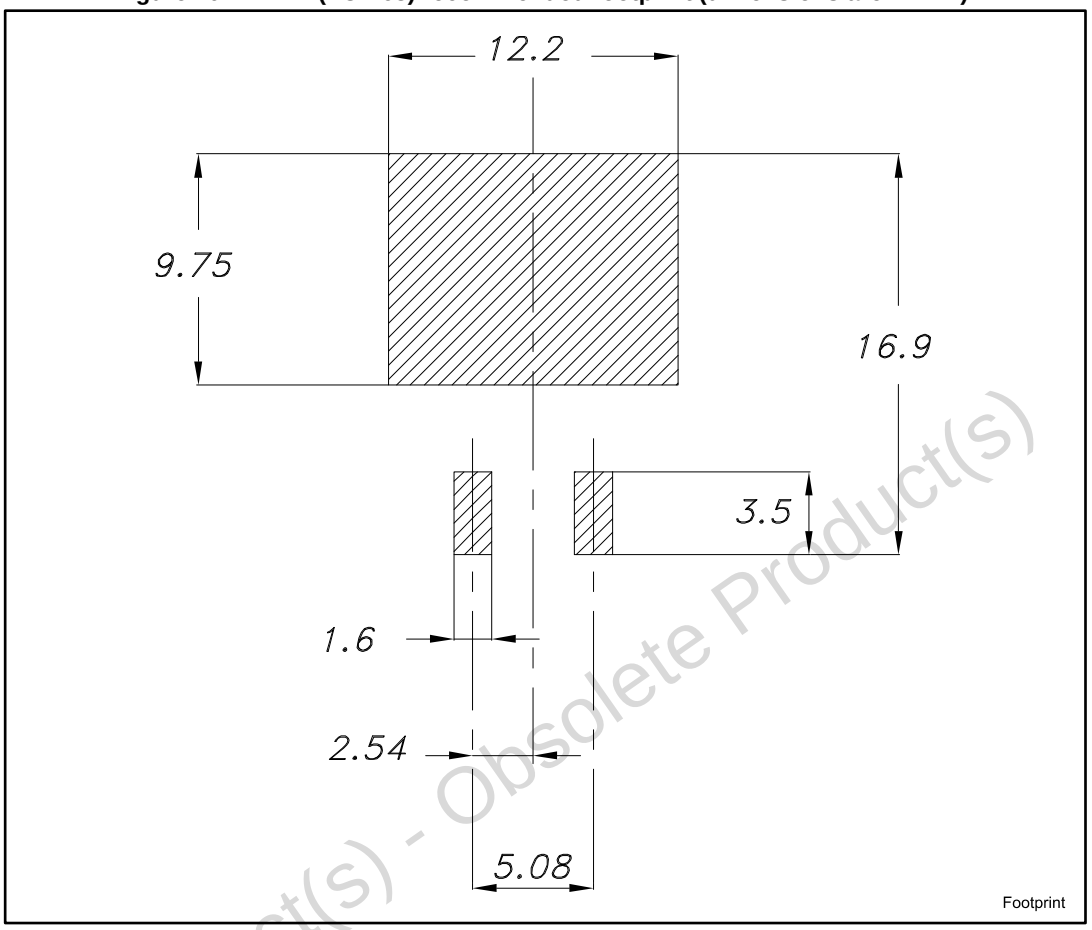


Table 9: D²PAK (TO-263) type A package mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10 | | 10.40 |
| E1 | 8.50 | 8.70 | 8.90 |
| E2 | 6.85 | 7.05 | 7.25 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.4 | |
| V2 | 0° | | 8° |

Figure 20: D²PAK (TO-263) recommended footprint (dimensions are in mm)



## 4.2 D²PAK packing information

**Figure 21: Tape**

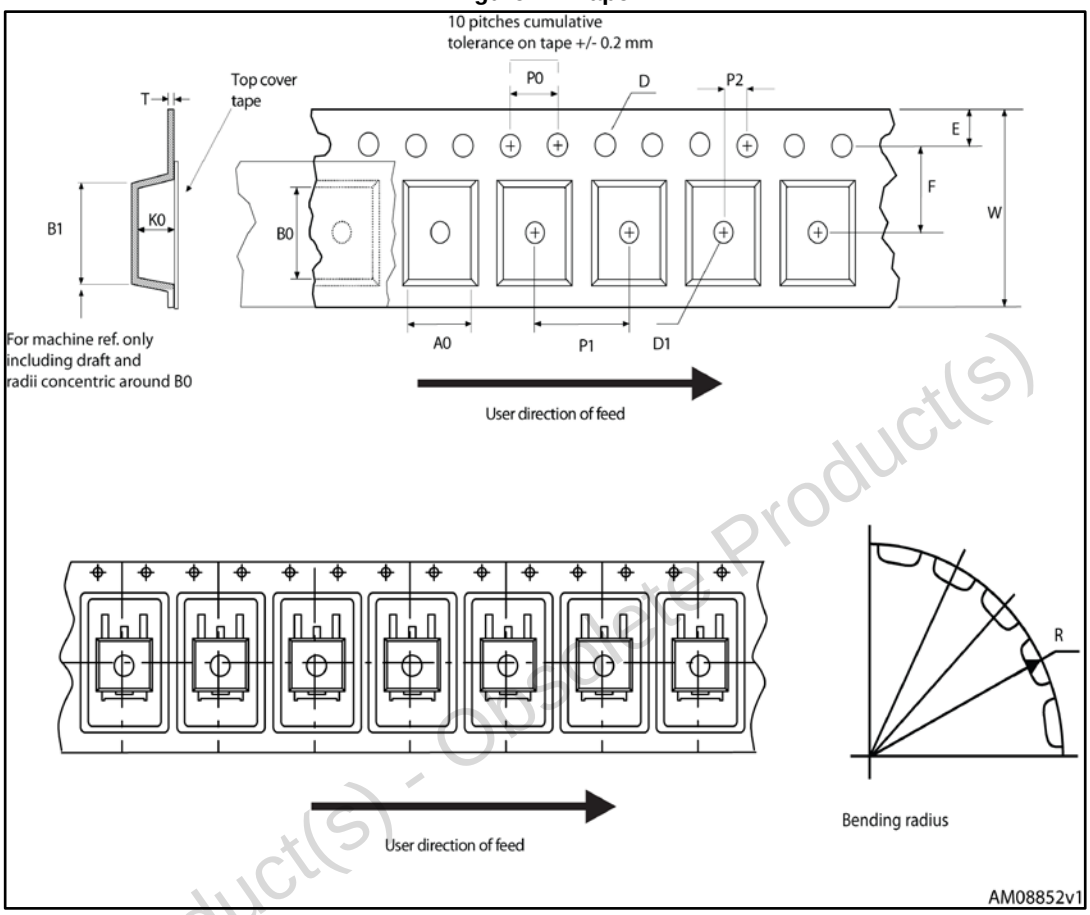


**Figure 22: Reel**

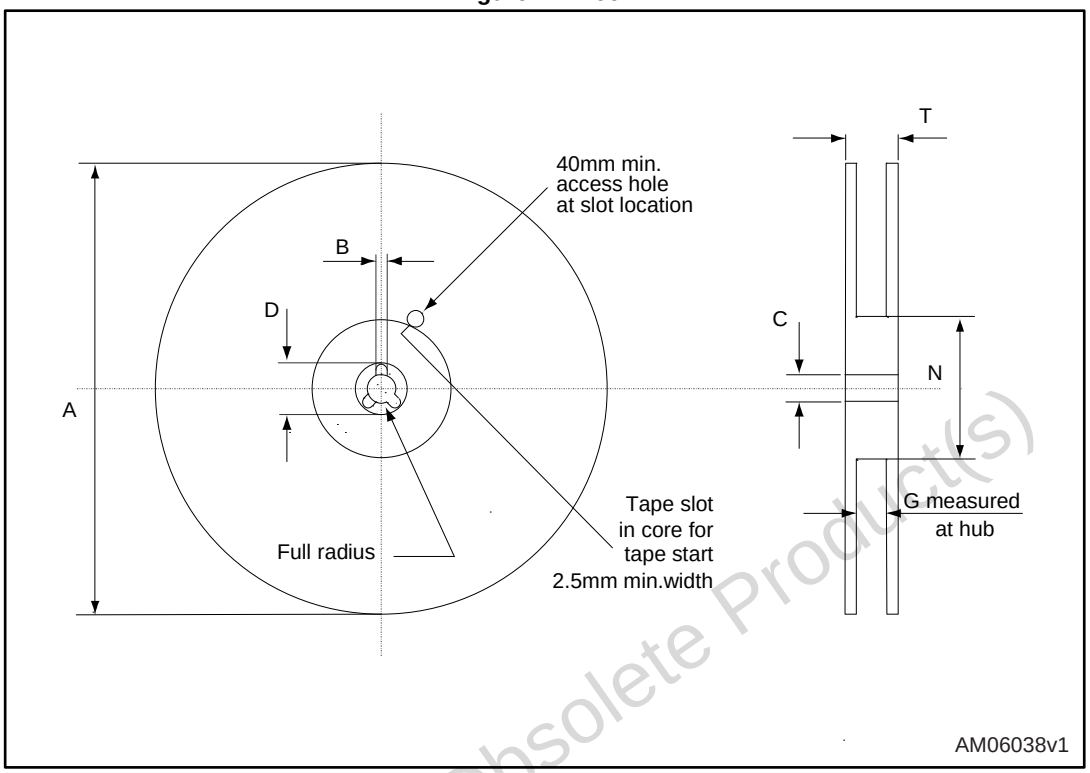



**Table 10: D²PAK tape and reel mechanical data**

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base qty | | 1000 |
| P2 | 1.9 | 2.1 | Bulk qty | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

# 5 Revision history

Table 11: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 10-Aug-2015 | 1 | First release. |

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