

Automotive-grade N-channel 40 V, 1.3 mΩ typ., 180 A STripFET™ F6 Power MOSFETs in H<sup>2</sup>PAK-2 and H<sup>2</sup>PAK-6 packages

Datasheet - production data

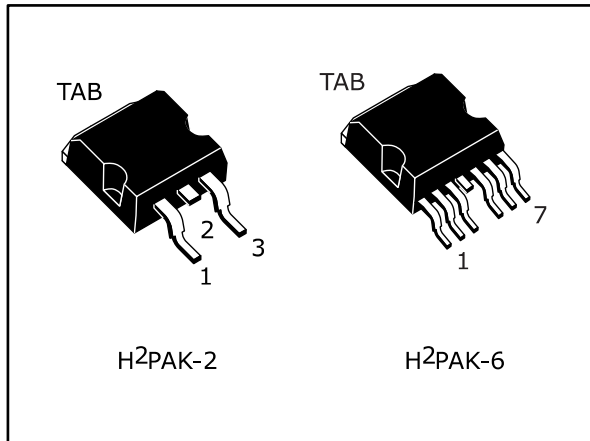
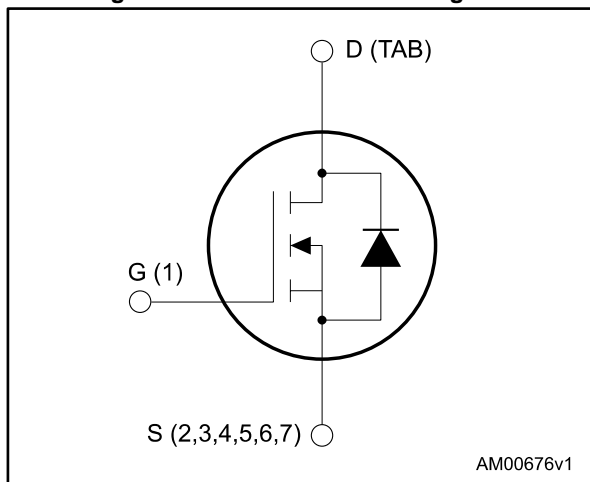


Figure 1: Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STH290N4F6-2AG	40 V	1.7 mΩ	180 A	300 W
STH290N4F6-6AG				

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STH290N4F6-2AG	290N4F6	H <sup>2</sup> PAK-2	Tape and Reel
STH290N4F6-6AG		H <sup>2</sup> PAK-6	

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	180	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	180	
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	300	W
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature		

**Notes:**

<sup>(1)</sup> Limited by package, current allowed by silicon is 295 A.

<sup>(2)</sup> Pulse width is limited by safe operating area.

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	

**Notes:**

<sup>(1)</sup> When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_{\text{casePCB}} = 25\text{ °C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 45\text{ A}$		1.3	1.7	m $\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	7380	-	$\mu\text{F}$
$C_{oss}$	Output capacitance		-	1080	-	
$C_{rss}$	Reverse transfer capacitance		-	590	-	
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 180\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Gate charge test circuit"</a> )	-	115	-	nC
$Q_{gs}$	Gate-source charge		-	33	-	
$Q_{gd}$	Gate-drain charge		-	32	-	

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 90\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	20	-	ns
$t_r$	Rise time		-	116	-	
$t_{d(off)}$	Turn-off delay time		-	105	-	
$t_f$	Fall time		-	48	-	

Table 7: Source-drain diode

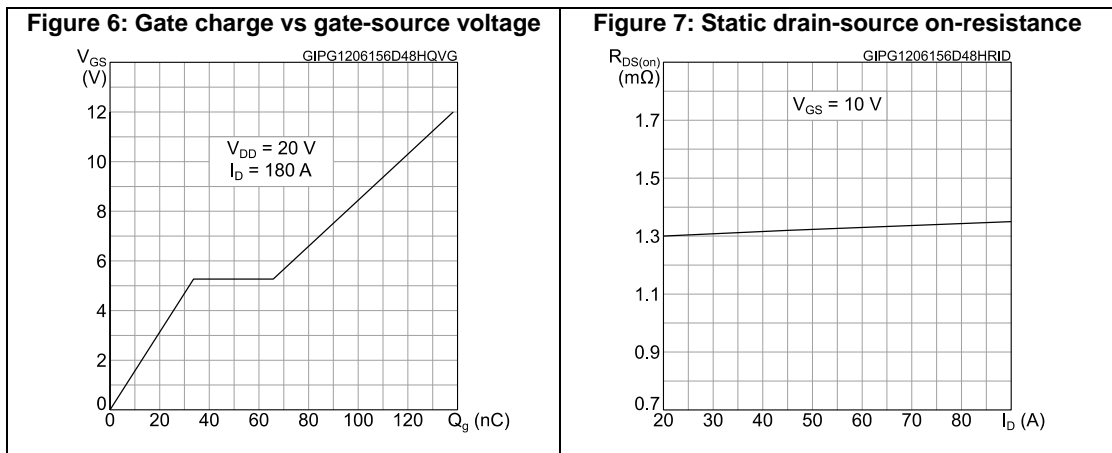
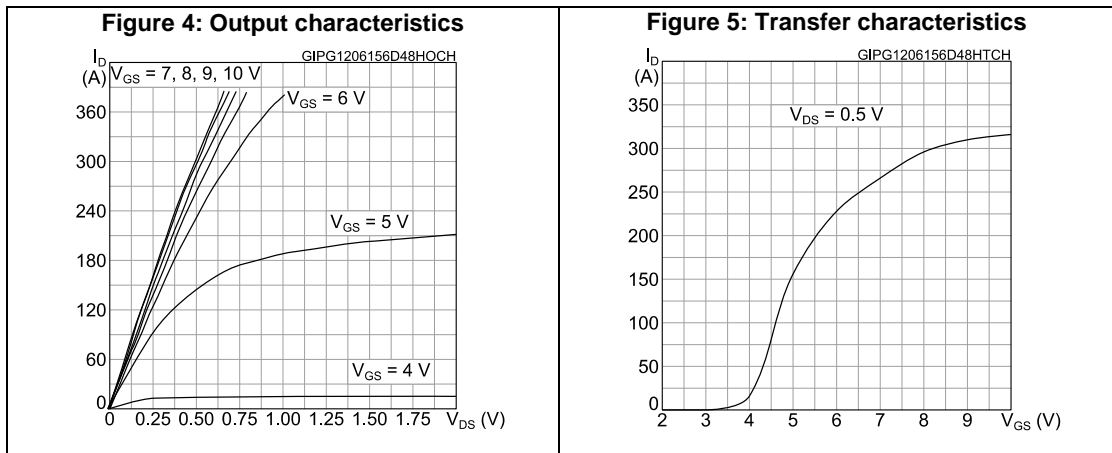
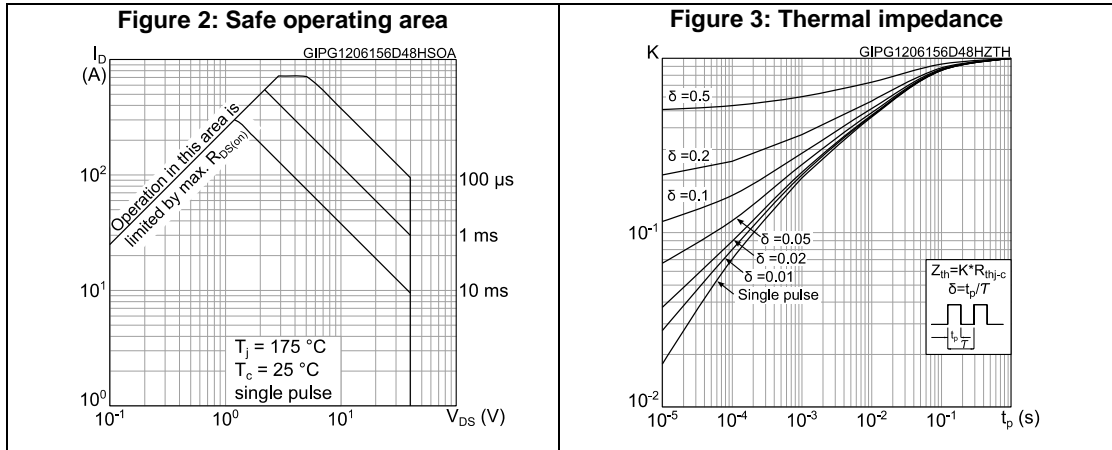
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		180	A
$I_{SDM}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 90\text{ A}$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 180\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 32\text{ V}$ (see <a href="#">Figure 15</a> : "Test circuit for inductive load switching and diode recovery times")	-	36		ns
$Q_{rr}$	Reverse recovery charge		-	42		nC
$I_{RRM}$	Reverse recovery current		-	2.3		A

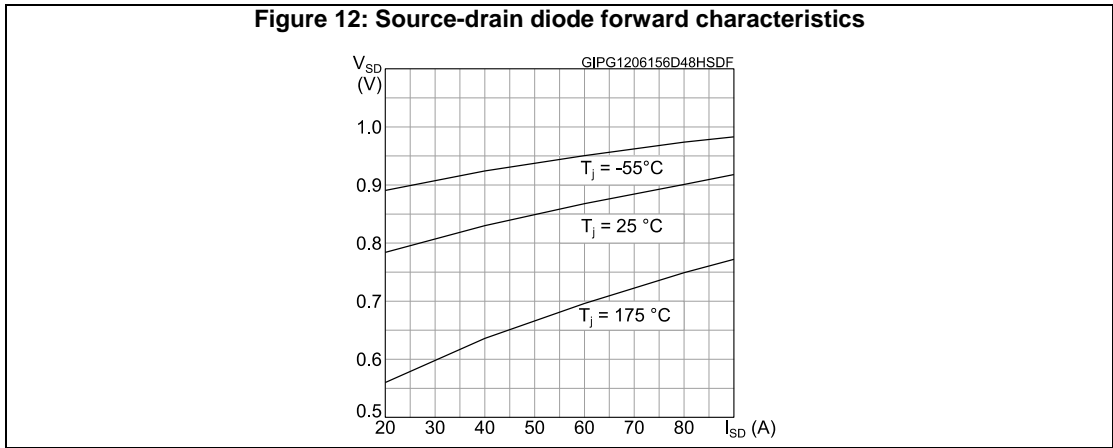
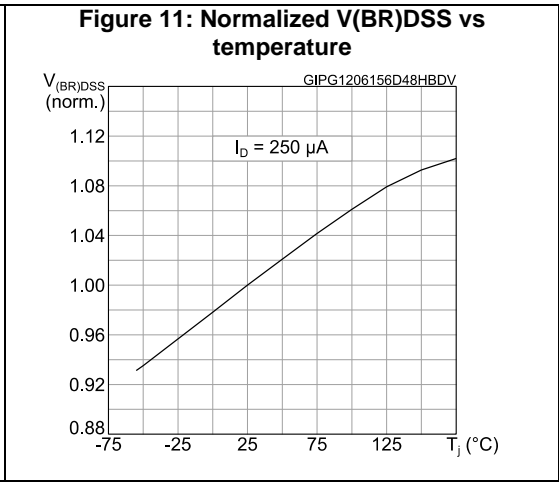
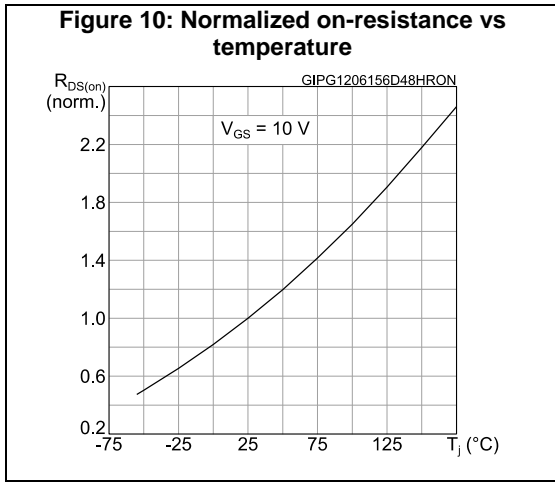
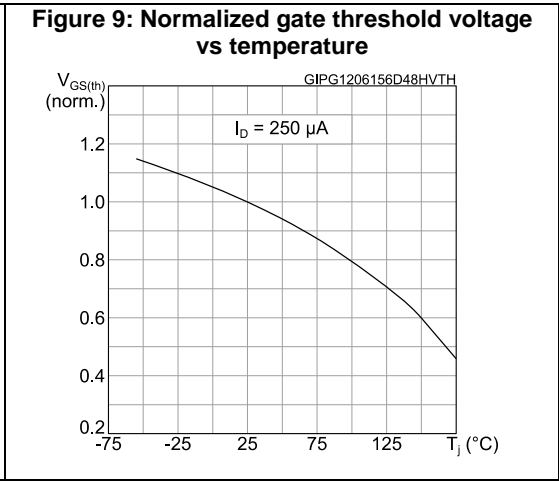
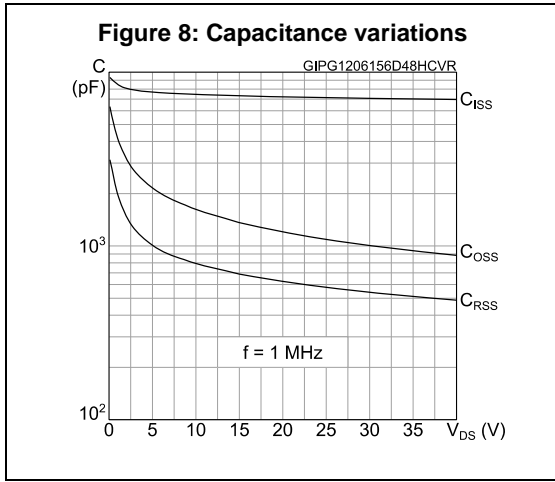
**Notes:**

(1) Limited by package, current allowed by silicon is 295 A.

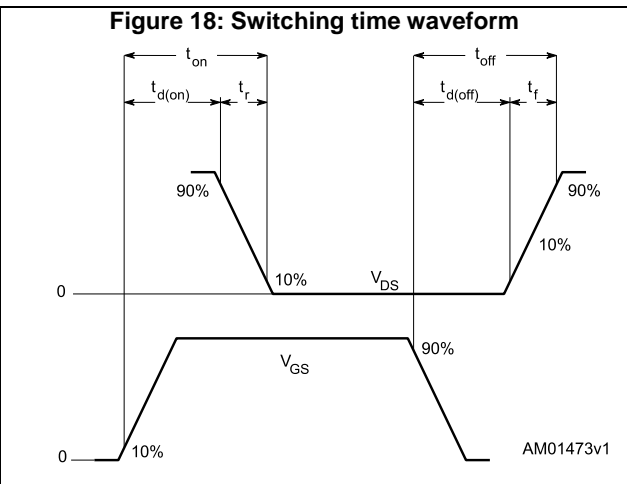
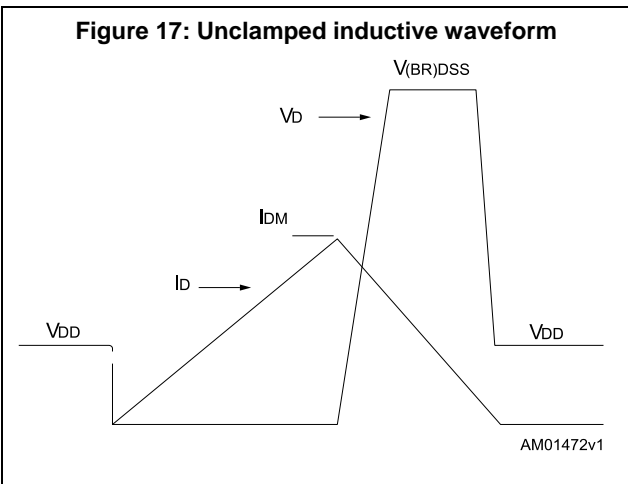
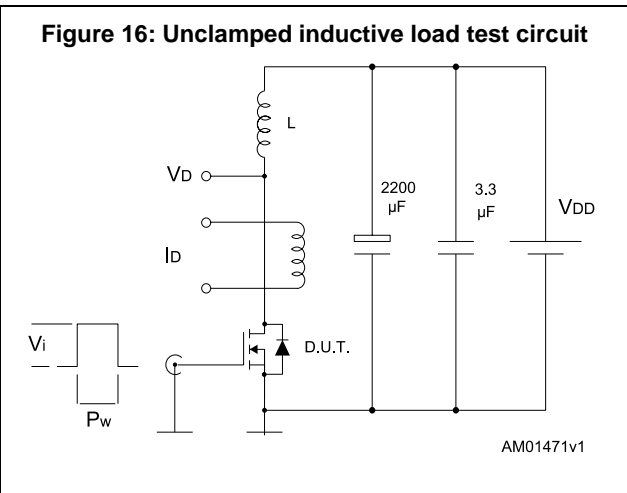
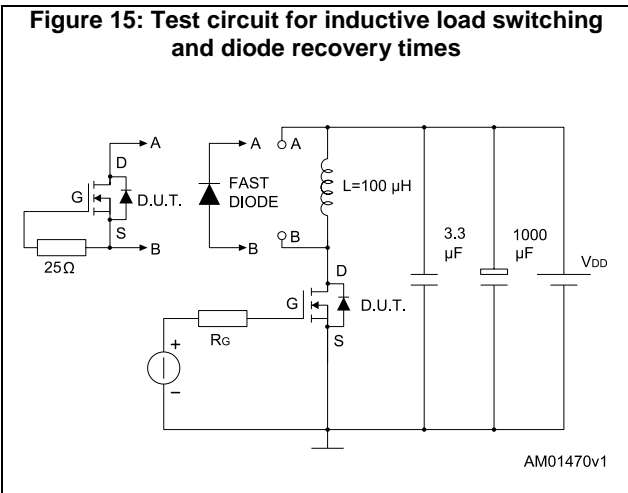
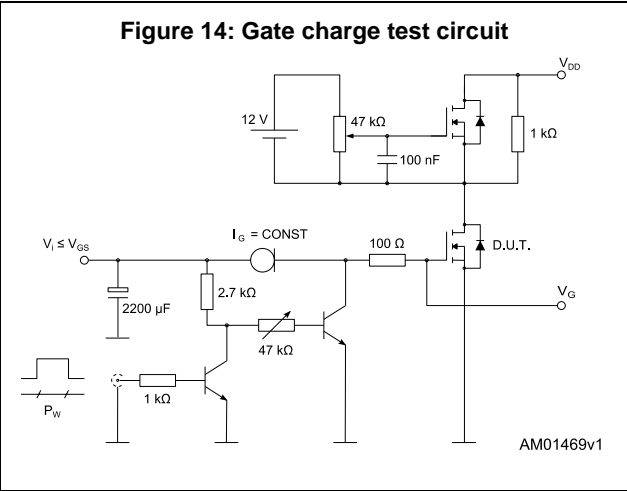
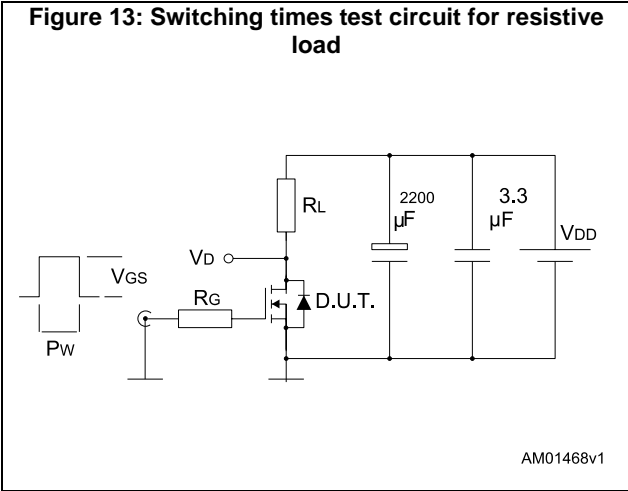
(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)





### 3 Test circuits





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

Figure 19: H<sup>2</sup>PAK-2 package outline

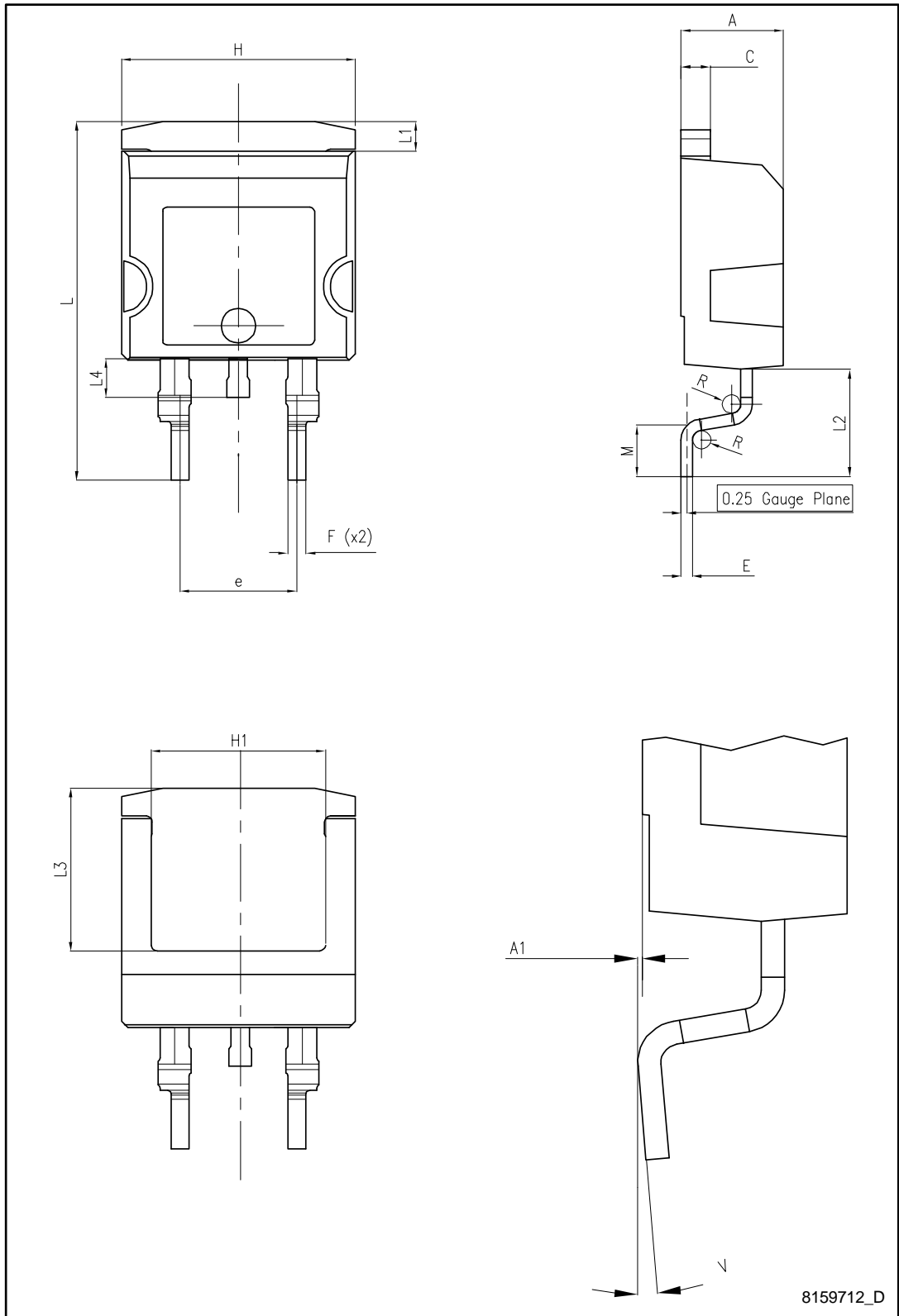
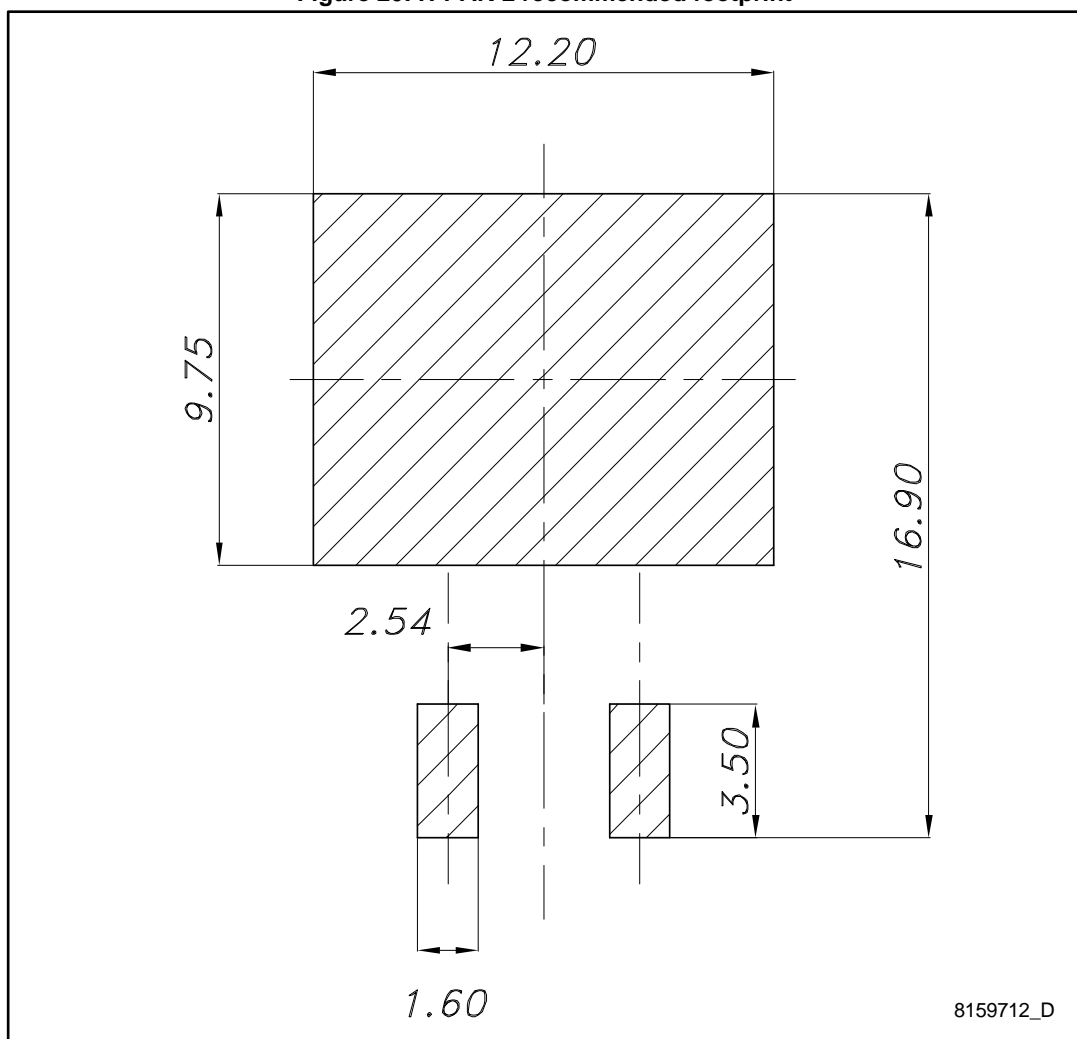


Table 8: H<sup>2</sup>PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H<sup>2</sup>PAK-2 recommended footprint



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### 4.2 H<sup>2</sup>PAK-6 package information

Figure 21: H<sup>2</sup>PAK-6 package outline

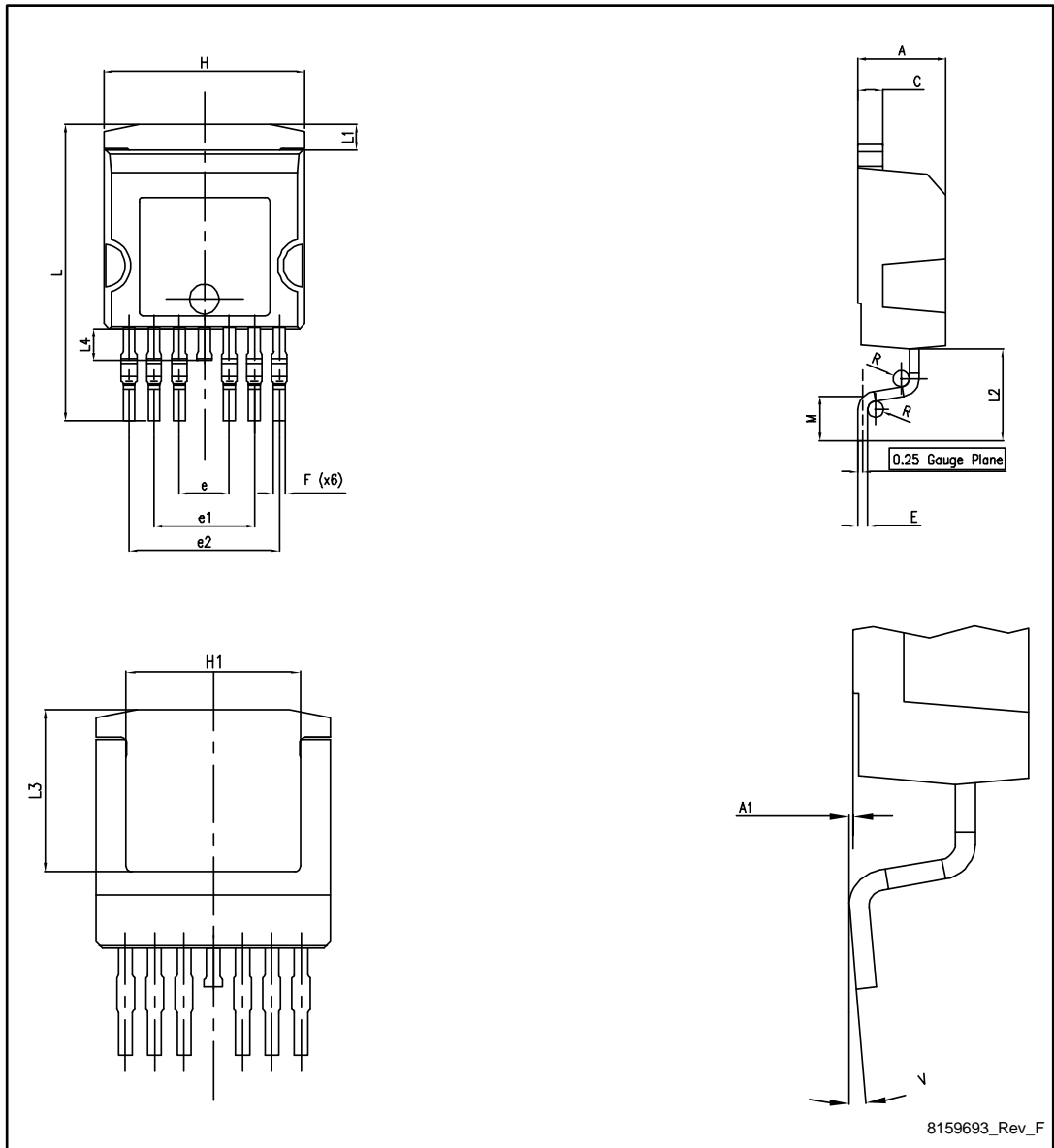
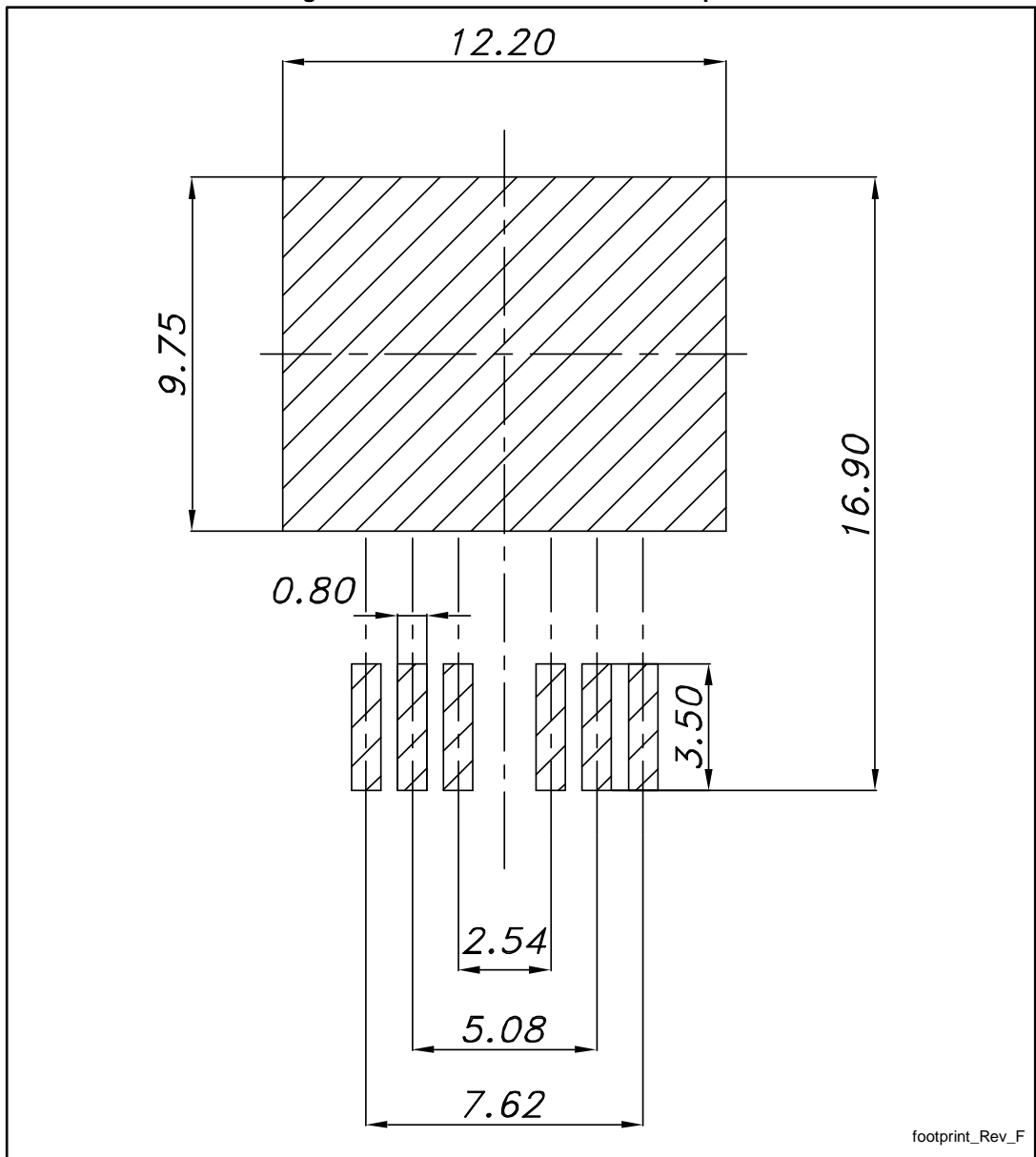


Table 9: H<sup>2</sup>PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22: H<sup>2</sup>PAK-6 recommended footprint



Dimensions are in mm.

### 4.3 H<sup>2</sup>PAK packing information

Figure 23: Tape outline

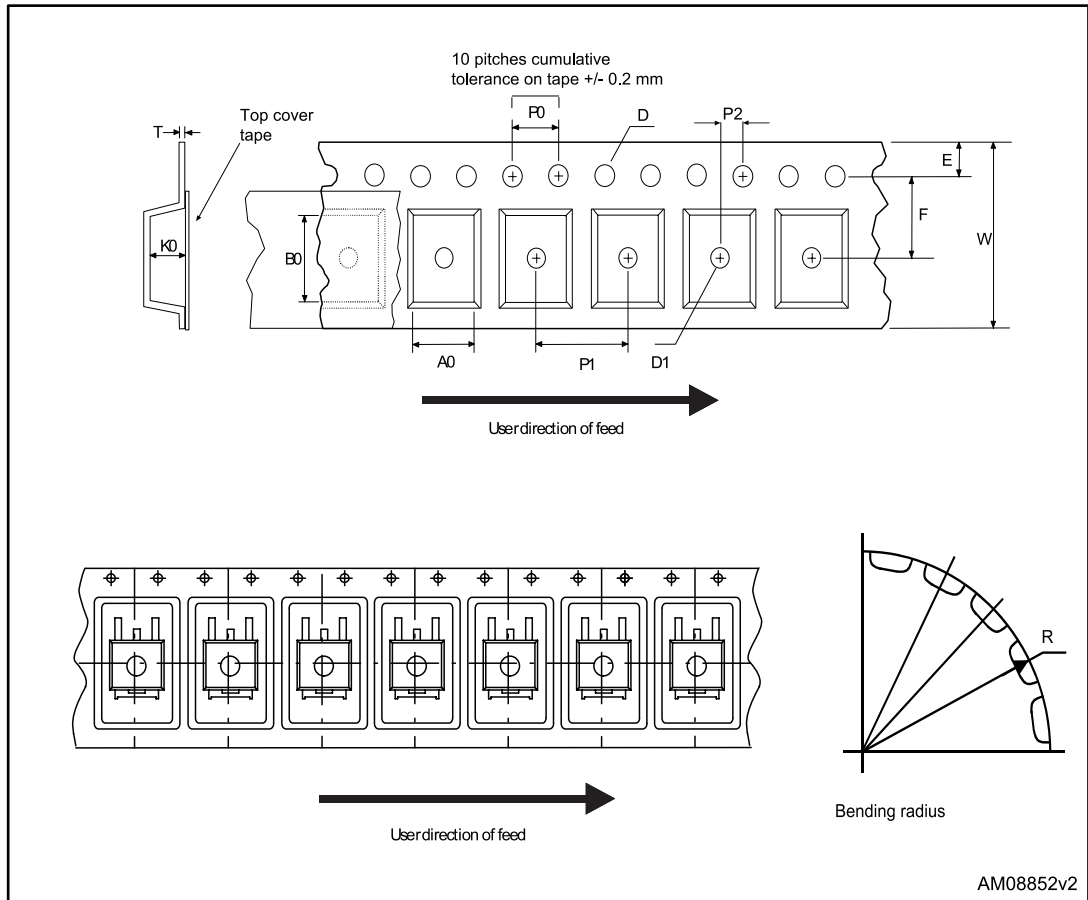


Figure 24: Reel outline

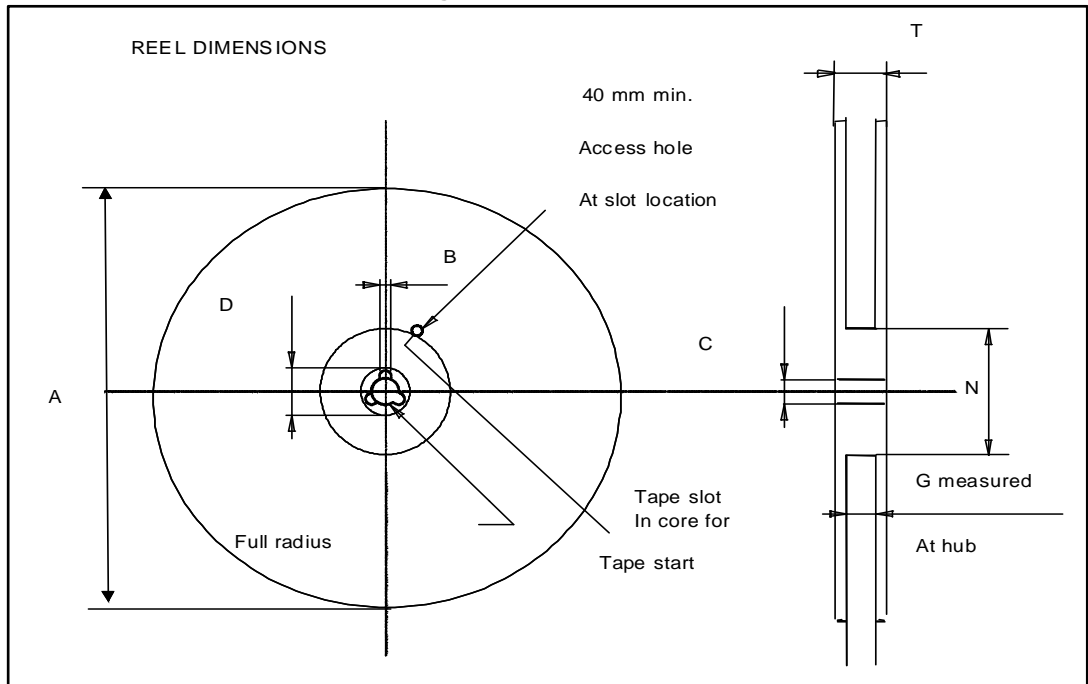




Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
03-Jul-2015	1	First release.

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