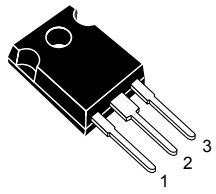
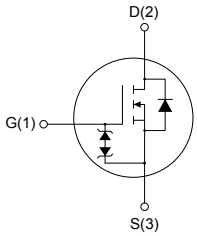
# STW58N65DM2AG

Datasheet

## Automotive-grade N-channel 650 V, 0.058 Ω typ., 48 A, MDmesh™ DM2 Power MOSFET in a TO-247 package




TO-247




NG1D2S3Z

| Product status link |
|---|
| STW58N65DM2AG |

| Product summary | |
|---|---|
| **Order code** | STW58N65DM2AG |
| **Marking** | 58N65DM2 |
| **Package** | TO-247 |
| **Packing** | Tube |

## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STW58N65DM2AG | 650 V | 0.065 Ω | 48 A | 360 W |

- AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

## Applications

- Switching applications

## Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge ($Q_{rr}$) and time ($t_{rr}$) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_{case}$ = 25 °C | 48 | A |
| | Drain current (continuous) at $T_{case}$ = 100 °C | 30 | |
| $I_{DM}$(1) | Drain current (pulsed) | 150 | A |
| $P_{TOT}$ | Total dissipation at $T_{case}$ = 25 °C | 360 | W |
| dv/dt(2) | Peak diode recovery voltage slope | 50 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | |
| $T_{stg}$ | Storage temperature range | -55 to 150 | °C |
| $T_J$ | Operating junction temperature range | | |

1. *Pulse width is limited by safe operating area.*
2. *$I_{SD}$ ≤ 48 A, di/dt=800 A/µs, $V_{DS}$ peak < $V_{(BR)DSS}$, $V_{DD}$ = 80% $V_{(BR)DSS}$*
3. *$V_{DS}$ ≤ 520 V*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.35 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient | 50 | |

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$(1) | Avalanche current, repetitive or not repetitive | 7 | A |
| $E_{AS}$(2) | Single pulse avalanche energy | 1300 | mJ |

1. *Pulse width is limited by $T_{Jmax}$.*
2. *Starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V*

# 2 Electrical characteristics

($T_{case}$ = 25 °C unless otherwise specified)

**Table 4. Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | | 10 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V, $T_{case}$ = 125 °C(1) | | | 100 | |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±25 V | | | ±5 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 24 A | | 0.058 | 0.065 | Ω |

1. *Defined by design, not subject to production test.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 4100 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 160 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.5 | - | |
| $C_{oss\ eq.}$(1) | Equivalent output capacitance | $V_{DS}$ = 0 to 520 V, $V_{GS}$ = 0 V | - | 375 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 A | - | 4.1 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 48 A, $V_{GS}$ = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 88 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 22 | - | |
| $Q_{gd}$ | Gate-drain charge | | - | 37 | - | |

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 325 V, $I_D$ = 24 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 28 | - | ns |
| $t_r$ | Rise time | | - | 31 | - | |
| $t_{d(off)}$ | Turn-off delay time | | - | 157 | - | |
| $t_f$ | Fall time | | - | 7.7 | - | |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 48 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 150 | A |
| $V_{SD}$(2) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 48 A | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 48 A, di/dt = 100 A/µs, $V_{DD}$ = 100 V (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 135 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 0.68 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 10 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 48 A, di/dt = 100 A/µs, $V_{DD}$ = 100 V, $T_J$ = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 260 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.75 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 21 | | A |

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

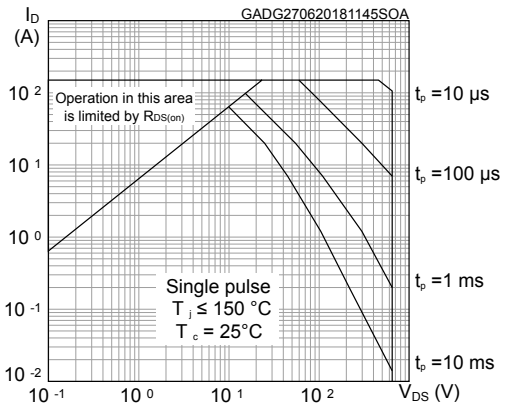



**Figure 2. Thermal impedance**

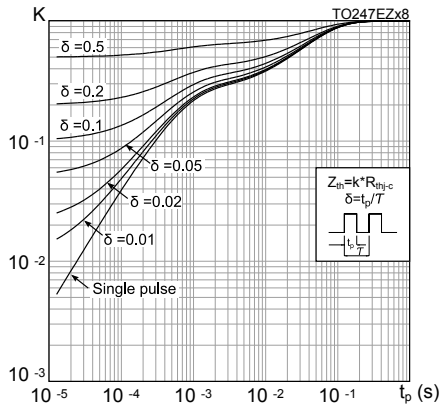



**Figure 3. Output characteristics**

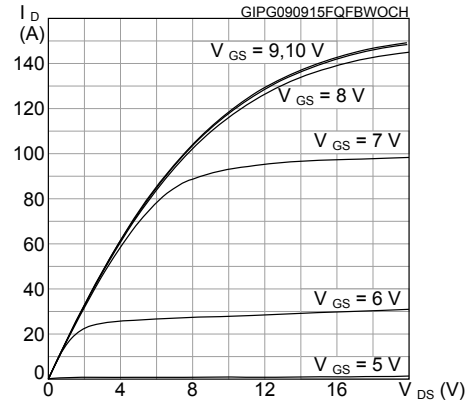



**Figure 4. Transfer characteristics**

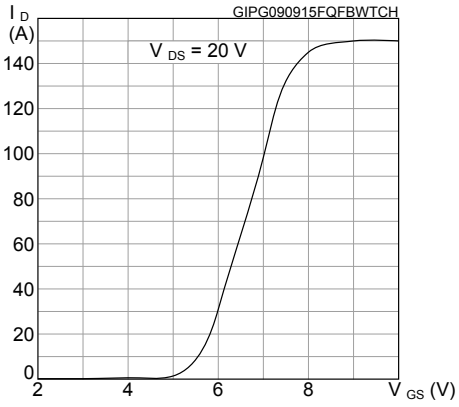



**Figure 5. Gate charge vs gate-source voltage**

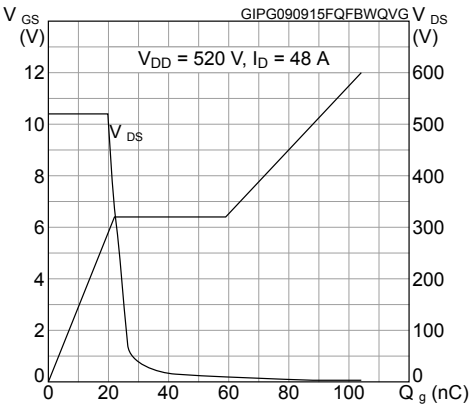



**Figure 6. Static drain-source on-resistance**

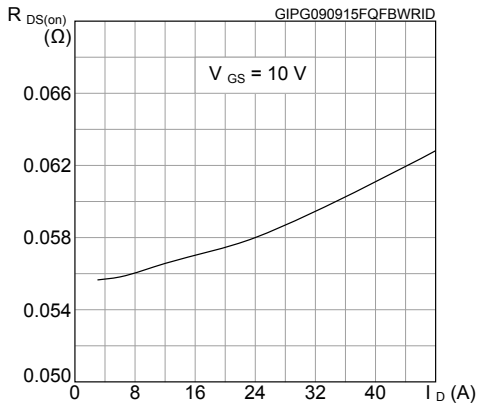


**Figure 7. Capacitance variations**

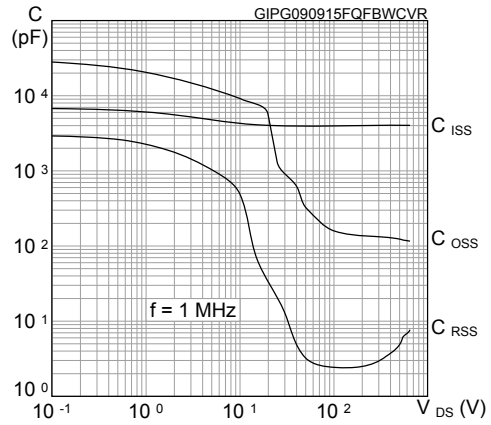



**Figure 8. Normalized gate threshold voltage vs temperature**

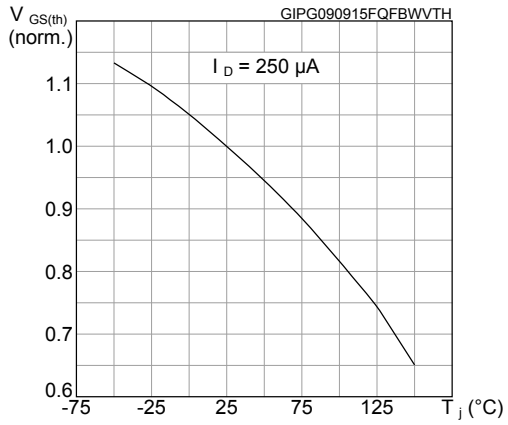



**Figure 9. Normalized on-resistance vs temperature**

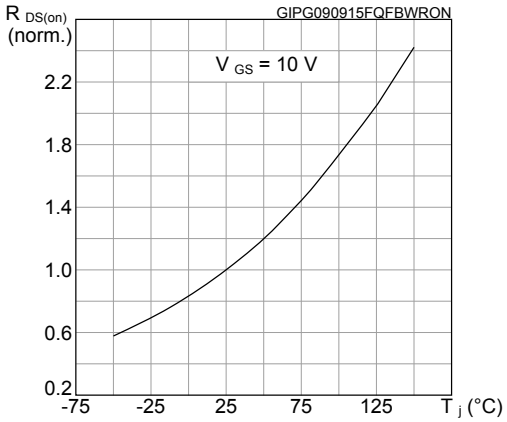



**Figure 10. Normalized $V_{(BR)DSS}$ vs temperature**

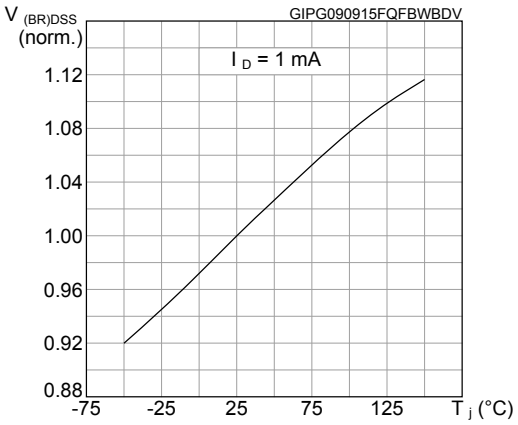



**Figure 11. Output capacitance stored energy**

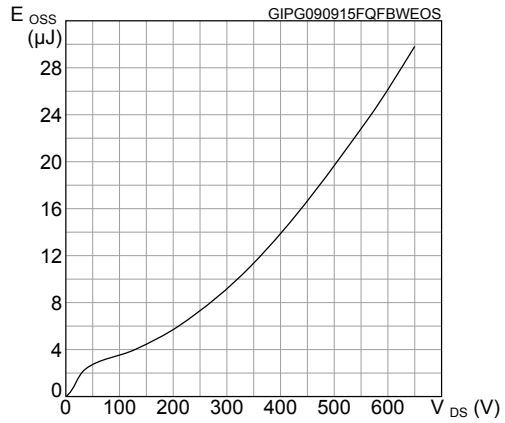
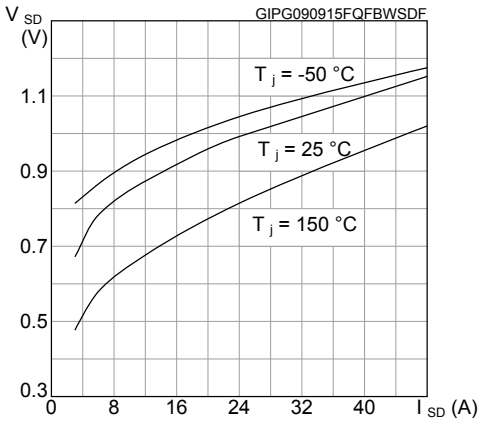



**Figure 12. Source- drain diode forward characteristics**



# 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

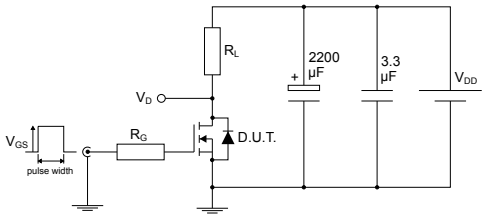



**Figure 14. Test circuit for gate charge behavior**

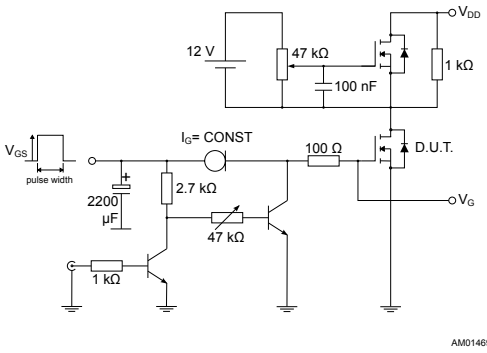



**Figure 15. Test circuit for inductive load switching and diode recovery times**

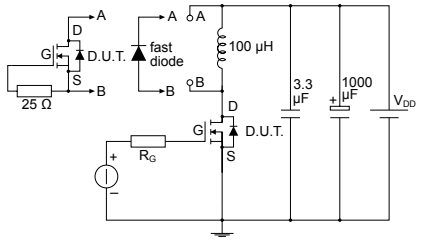



**Figure 16. Unclamped inductive load test circuit**

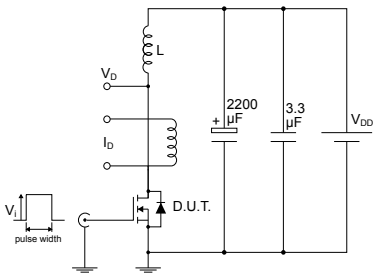



**Figure 17. Unclamped inductive waveform**

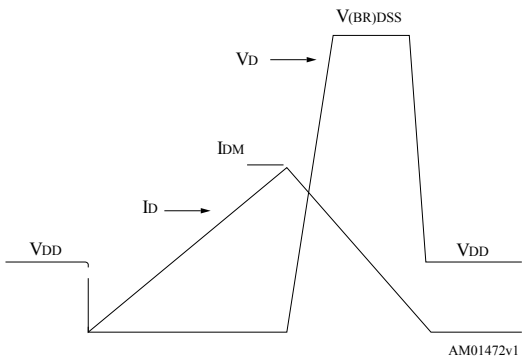
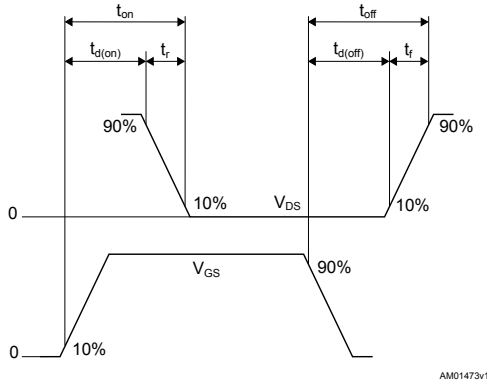



**Figure 18. Switching time waveform**

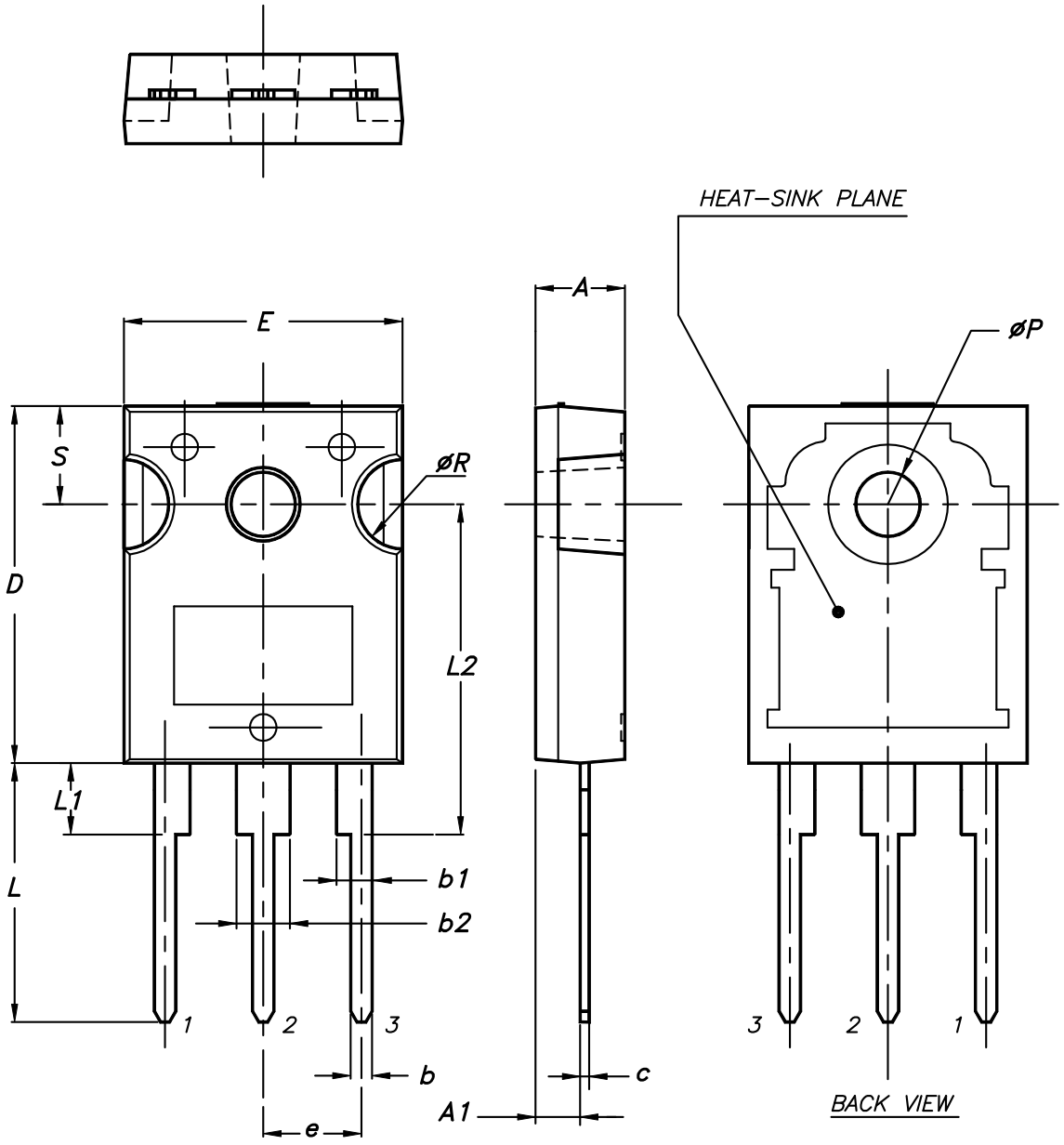


# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 4.1 TO-247 package information

Figure 19. TO-247 package outline




0075325_9

Table 8. **TO-247 package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.85 | | 5.15 |
| A1 | 2.20 | | 2.60 |
| b | 1.0 | | 1.40 |
| b1 | 2.0 | | 2.40 |
| b2 | 3.0 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.85 | | 20.15 |
| E | 15.45 | | 15.75 |
| e | 5.30 | 5.45 | 5.60 |
| L | 14.20 | | 14.80 |
| L1 | 3.70 | | 4.30 |
| L2 | | 18.50 | |
| ØP | 3.55 | | 3.65 |
| ØR | 4.50 | | 5.50 |
| S | 5.30 | 5.50 | 5.70 |

## Revision history

Table 9. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 09-Sep-2015 | 1 | Initial release. |
| 15-Sep-2015 | 2 | In section *Electrical characteristics (curves)*:<br>- updated figure *Safe operating area* |
| 02-Jul-2018 | 3 | Removed maturity status indication from cover page. The document status is production data.<br>Updated Table 1. Absolute maximum ratings and Table 7. Source-drain diode.<br>Updated Figure 1. Safe operating area.<br>Minor text changes |

# Contents

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